

54/74165
54LS/74LS165

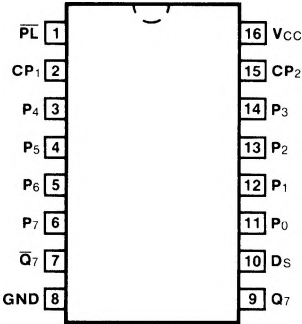
8-BIT PARALLEL-TO-SERIAL CONVERTER

DESCRIPTION — The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (Ds) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74165PC, 74LS165PC		9B
Ceramic DIP (D)	A	74165DC, 74LS165DC	54165DM, 54LS165DM	6B
Flatpak (F)	A	74165FC, 74LS165FC	54165FM, 54LS165FM	4L

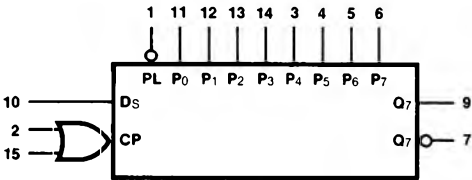
CONNECTION DIAGRAM
PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP ₁ , CP ₂	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	0.5/0.25
D _S	Serial Data Input	1.0/1.0	0.5/0.25
PL	Asynchronous Parallel Load Input (Active LOW)	2.0/2.0	1.5/0.75
P ₀ — P ₇	Parallel Data Inputs	1.0/1.0	0.5/0.25
Q ₇	Serial Output From Last Stage	20/10	10/5.0 (2.5)
$\overline{Q}_7$	Complementary Output	20/10	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the PL signal is LOW. The parallel data can change while PL is LOW provided that the recommended setup and hold times are observed.

For clocked operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

TRUTH TABLE

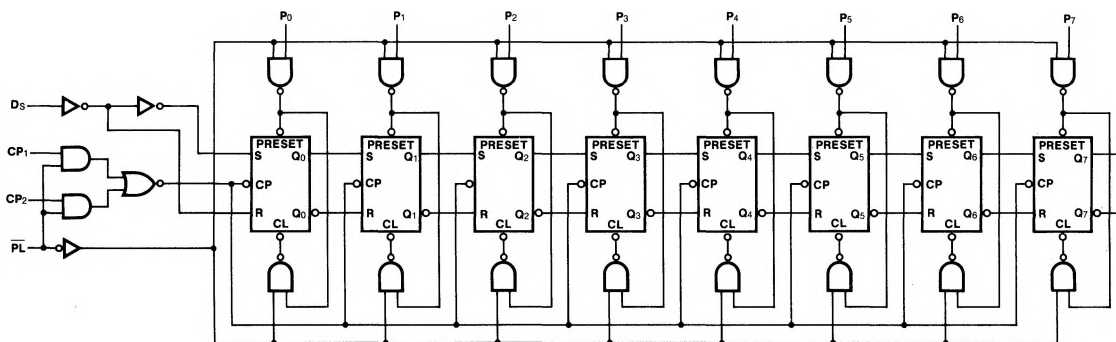
PL	CP		CONTENTS								RESPONSE
	1	2	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	P ₀	P ₁	P ₂	P ₃	P ₄	P ₅	P ₆	P ₇	Parallel Entry
H	L		D _S	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H	H		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change
H		L	D _S	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H		H	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max		
I _{OS}	Output Short Circuit Current	XM	-20	-55			mA	V _{CC} = Max
		XC	-18	-55				
I _{CC}	Power Supply Current		63		36		mA	V _{CC} = Max, $\overline{PL} = \square$ P _n = $\square$ CP ₁ , CP ₂ = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	20		30		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay P _L to Q ₇ or $\overline{Q}_7$	31 40		30 30		ns	Figs. 3-1, 3-16
t _{PLH} t _{PHL}	Propagation Delay CP ₁ to Q ₇ or $\overline{Q}_7$	24 31		30 30		ns	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay P ₇ to Q ₇	17 36		25 30		ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay P ₇ to $\overline{Q}_7$	27 27		30 25		ns	Figs. 3-1, 3-4

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW P _n to PL	10		10		ns	Fig. 3-13
t _h (H) t _h (L)	Hold Time HIGH or LOW P _n to PL	0		5.0		ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW Ds to CP _n	20		10		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW Ds to CP _n	0		5.0		ns	
t _s (H)	Setup Time HIGH CP ₁ to CP ₂ or CP ₂ to CP ₁	30		30		ns	
t _w (H)	CP _n Pulse Width HIGH	25		20		ns	Fig. 3-8
t _w (L)	PL Pulse Width LOW	15		15		ns	Fig. 3-16
t _{rec}	Recovery Time PL to CP _n	45		15		ns	