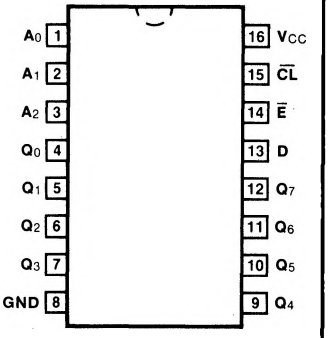
54LS/74LS259

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The '259 is a high speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multi-functional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

- **SERIAL-TO-PARALLEL CONVERSION**
- **EIGHT BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **FULLY TTL AND CMOS COMPATIBLE**

CONNECTION DIAGRAM
PINOUT A



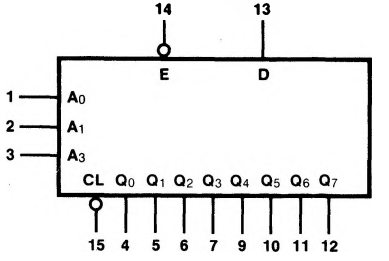
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS259PC		9B
Ceramic DIP (D)	A	74LS259DC	54LS259DM	6B
Flatpak (F)	A	74LS259FC	54LS259FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	0.5/0.25
D	Data Input	0.5/0.25
$\overline{E}$	Enable Input (Active LOW)	1.0/0.5
$\overline{CL}$	Conditional Clear Input (Active LOW)	0.5/0.25
$Q_0 - Q_7$	Latch Outputs	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. in the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the '259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the '259.

MODE SELECT TABLE

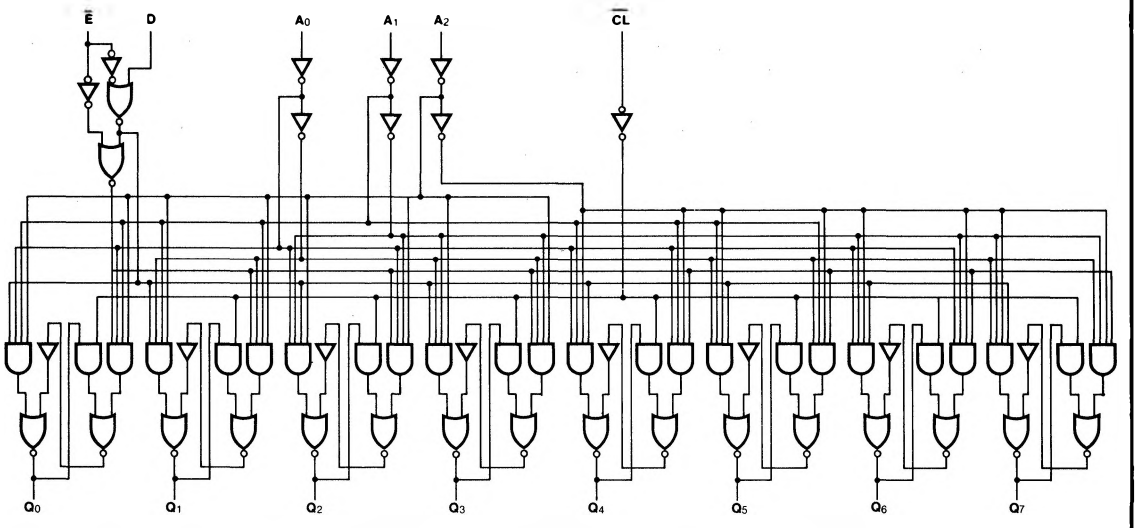
$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

TRUTH TABLE

INPUTS						OUTPUTS								
$\overline{CL}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	I	I	L	L	L	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable
H	L	H	L	L	L	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Latch
H	L	L	H	L	L	Q_{t-1}	L	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
H	L	H	H	L	L	Q_{t-1}	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
H	L	L	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	L	
H	L	H	H	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	H	

Q_{t-1} = Previous Output State
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		36	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C_L = 15 pF			
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		27 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		30 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay, A_n to Q_n		30 20	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay, $\overline{CL}$ to Q_n		18	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH, D to $\overline{E}$	20		ns	Fig. 3-13
t_h (H)	Hold Time HIGH, D to $\overline{E}$	0		ns	
t_s (L)	Setup Time LOW, D to $\overline{E}$	15		ns	
t_h (L)	Hold Time LOW, D to $\overline{E}$	0		ns	
t_s	Setup Time HIGH or LOW, A_n to $\overline{E}$	0		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17			