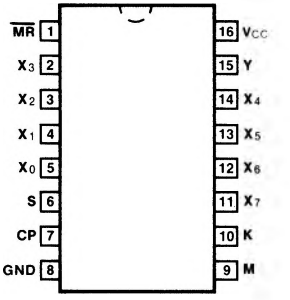
54LS/74LS384

8-BIT SERIAL/PARALLEL TWOS COMPLEMENT MULTIPLIER

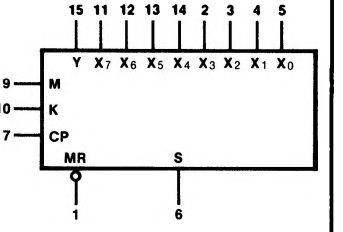
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '384 is an 8-bit by 1-bit sequential logic element that multiplies two numbers represented in twos complement notation. The device implements Booth's algorithm internally to produce a twos complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand (X_0 — X_7). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the S output, least significant bit first.

The K input is used for expansion to longer X words, using two or more '384 packages. The Mode Control (M) input is used to establish the most significant package. An asynchronous Master Reset ($\overline{MR}$) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

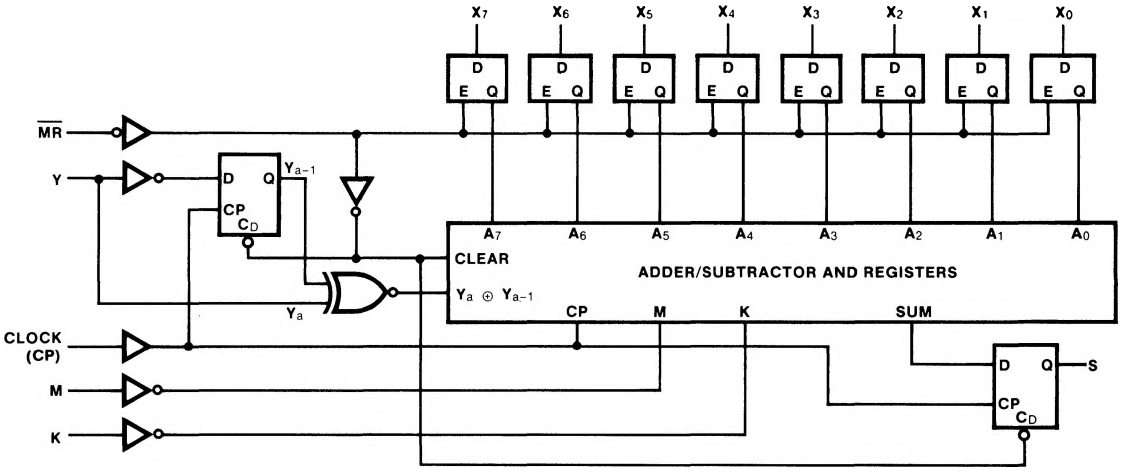
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS384PC		9B
Ceramic DIP (D)	A	74LS384DC	54LS384DM	6B
Flatpak (F)	A	74LS384FC	54LS384FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
K	Serial Expansion Input	0.75/0.75
M	Mode Control Input	0.5/0.3
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.75/0.75
X_0 — X_7	Multiplicand Data Inputs	0.5/0.3
Y	Serial Multiplier Input	2.0/2.0
S	Serial Product Output	25/7.5 (5.0)

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{MR}$	CP	K	M	X_i	Y	Y_{a-1}	S	
-		L	L					Most Significant Multiplier Device
-		CS	H					Devices Cascaded in Multiplier String
L				OP		L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H								Device Enabled
H	⌐¬				L	L	AR	Shift Sum Register
H	⌐¬				L	H	AR	Add Multiplicand to Sum Register and Shift
H	⌐¬				H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	⌐¬				H	H	AR	Shift Sum Register

⌐¬ = LOW-to-HIGH transition
CS = Connected to S output of high order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

FUNCTIONAL DESCRIPTION — Referring to the logic diagram, the multiplicand (X_0 — X_7) latches are enabled to receive new data when $\overline{MR}$ is LOW. Data that meet the setup time requirements is latched and stored when $\overline{MR}$ goes HIGH. The LOW signal on MR also clears the Y_{a-1} flip-flop as well as the carry-save flip-flops and the partial product register in the arithmetic section. *Figure a* is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the carry logic. The cells use the carry-save technique to avoid the complexity and delays inherent in look-ahead carry schemes for longer words.

Figure b is a timing diagram for an 8 x 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that MR goes LOW shortly after the CP rising edge that marks the beginning of T_0 and goes HIGH again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input ($X_0 Y_0$) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the S output of the package. The next-least bit Y_1 of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, thanks to storage in its carry flip-flop and in the sum flip-flop of the next-least cell, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the S output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the S output contains information formed one stage further upstream. For example, the S output during T_9 contains X_7Y_0, which was actually formed during T_1.

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the '322 Shift Register. *Figure c* shows the method of using two '384s to perform a 12 x n bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to X_4 — X_7 of the most significant package. Whereas the 8 x 8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of *Figure c* requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store S_{n+11}.

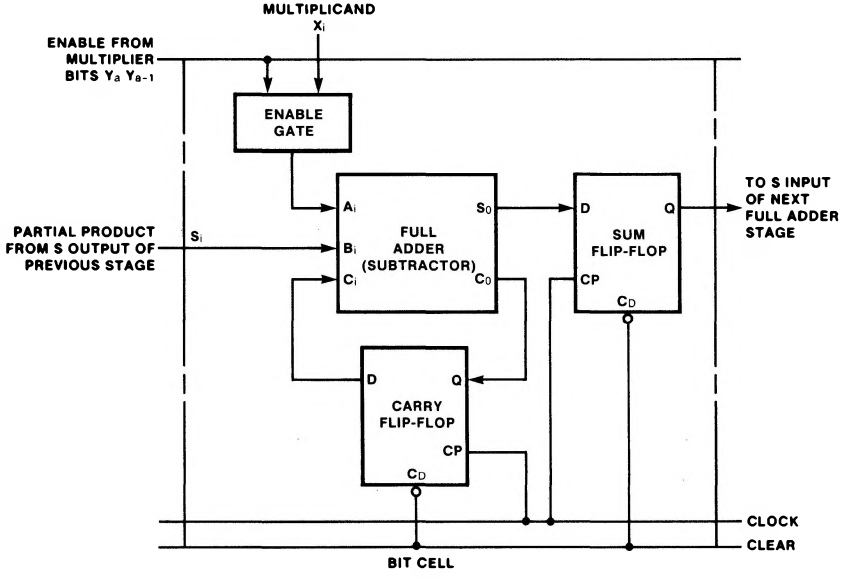


Fig. a Conceptual Carry Save Adder Cell

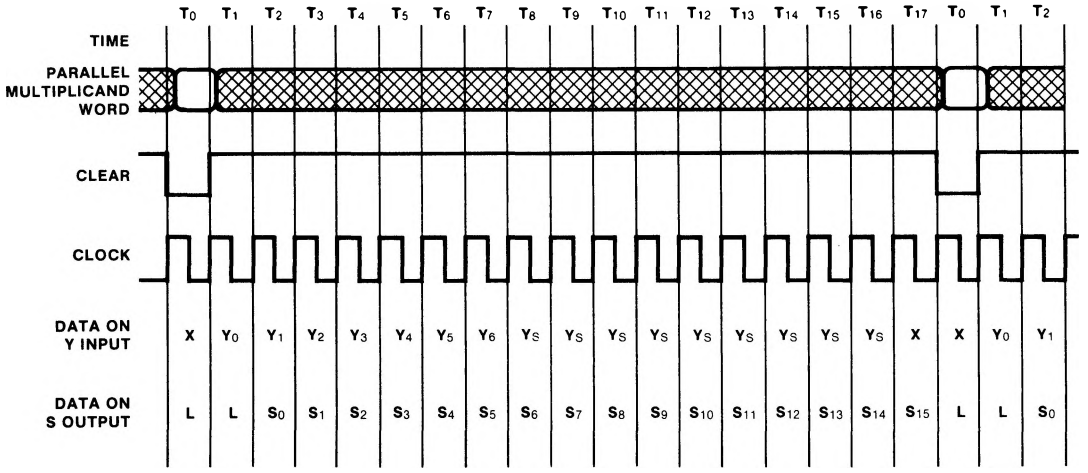


Fig. b Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication

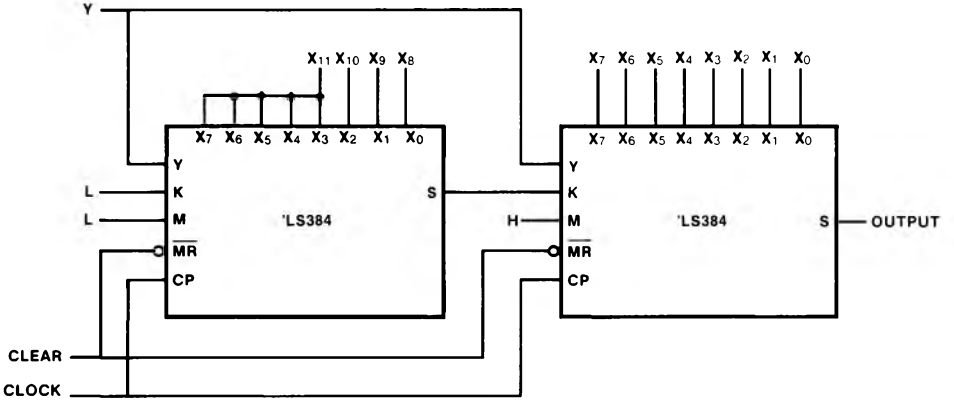


Fig. c A 12-Bit by N-Bit Two's Complement Multiplier

DC CHARATERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{OS}	Output Short Circuit Current	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		155	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to S		20 20	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to S		25	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW K to CP	18 18		ns	Fig. 3-6
t_s (H) t_s (L)	Setup Time HIGH or LOW Y to CP	32 32		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW K or Y to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW X_i to $\overline{MR}$	13 13		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW X_i to $\overline{MR}$	0 0		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	18		ns	