



54LS503/DM74LS503

8-Bit Successive Approximation Register (with Expansion Control)

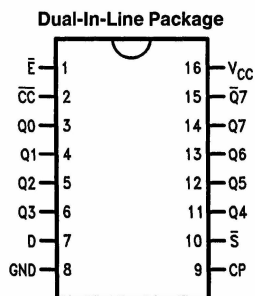
General Description

The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ($\bar{E}$) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on $\bar{E}$, after a START operation, forces Q7 HIGH and prevents the device from accepting serial data. With the $\bar{E}$ input of an 'LS503 connected to the $\bar{CC}$ output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its $\bar{CC}$ output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

Features

- Performs serial-to-parallel conversion
- Expansion control for longer words
- Storage and control for successive approximation A to D conversion
- Low power Schottky version of 2503

Connection Diagram

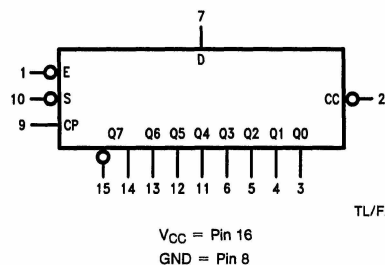


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Order Number 54LS503DMQB, 54LS503FMQB,
D74LS503WM or DM74LS503N

See NS Package Number J16A, M16B, N16E or W16A

Logic Symbol



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Pin Names	Description
D	Serial Data Input
$\bar{S}$	Start Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$\bar{E}$	Conversion Enable Input (Active LOW)
$\bar{CC}$	Conversion Complete Output (Active LOW)
Q0-Q7	Parallel Register Outputs
$\bar{Q}7$	Complement of Q7 Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS503			DM74LS503			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Voltage			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW S to CP	5 5			5 5			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW S to CP	5 5			5 5			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW S to CP	5 5			5 5			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW D to CP	5 5			5 5			ns
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

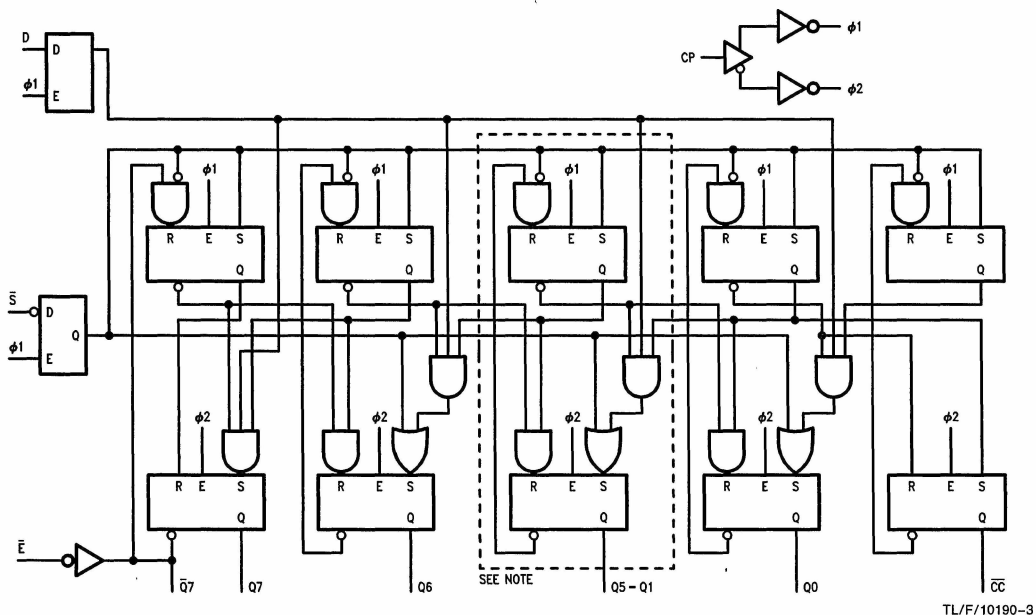
Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	54LS 2.5 DM74 2.7			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	54LS DM74		0.4 0.5	V
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			−0.8	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	54LS −20 DM74 −20		−100 −100	mA
I _{CC}	Supply Current	V _{CC} = Max			65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Symbol	Parameter	R _L = 2 kΩ, C _L = 15 pF		Units
		Min	Max	
f _{max}	Maximum Count Frequency	25		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Qn or CC		35 25	ns
t _{PLH} t _{PHL}	Propagation Delay E to Q7		20 24	ns

Logic Diagram



Note: Cell logic is repeated for register stages Q5 to Q1.

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Connection for Longer Word Lengths

