54/7476
54H/74H76
54LS/74LS76

DUAL JK FLIP-FLOP

(With Separate Sets, Clears and Clocks)

DESCRIPTION — The '76 and 'H76 are dual JK master/slave flip-flops with separate Direct Set, Direct Clear and Clock Pulse inputs for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM

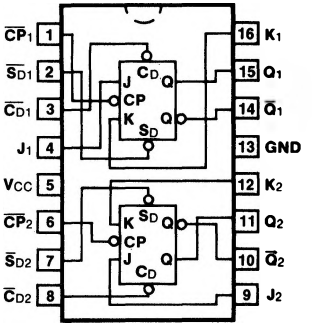
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

The 'LS76 is a dual JK, negative edge-triggered flip-flop also offering individual Direct Set, Direct Clear and Clock Pulse inputs. When the Clock Pulse input is HIGH, the JK inputs are enabled and data is accepted. This data will be transferred to the outputs according to the Truth Table on the HIGH-to-LOW clock transitions.

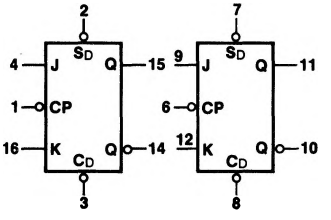
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7476PC, 74H76PC 74LS76PC		9B
Ceramic DIP (D)	A	7476DC, 74H76DC 74LS76DC	5476DM, 54H76DM 54LS76DM	6B
Flatpak (F)	A	7476FC, 74H76FC 74LS76FC	5476FM, 54H76FM 54LS76FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL

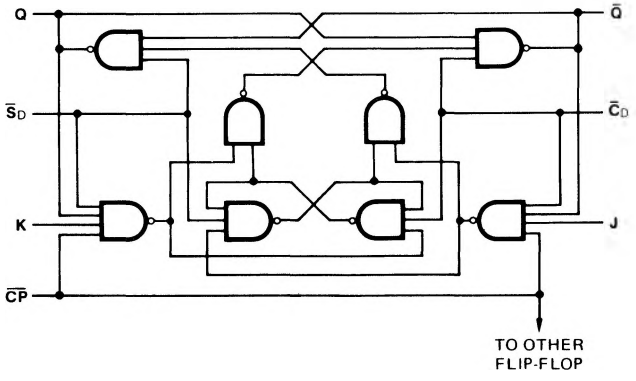


V_{CC} = Pin 5
GND = Pin 13

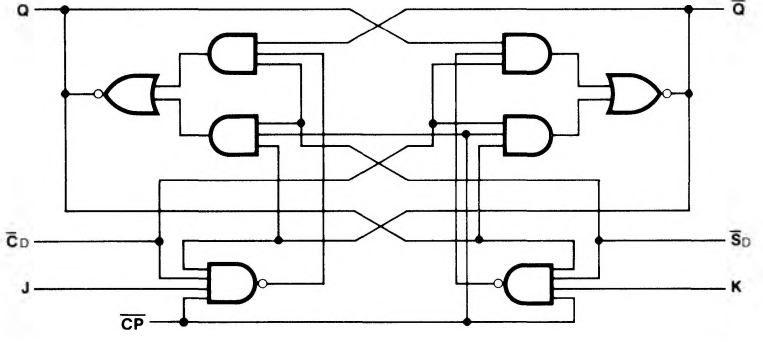
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	2.5/2.5	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	10/5.0 (2.5)

LÓGIC DIAGRAMS (one half shown)
'76, 'H76



'LS76



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		40		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF, R_L = 400 Ω		C_L = 25 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		25 40		21 27		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		25 40		13 24		20 30	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		20		ns	
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		0		ns	Fig. 3-18 ('76, 'H76)
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		0		20		ns	Fig. 3-7 ('LS76)
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		12 28		20 13.5		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	25		16		25		ns	Fig. 3-10