54/7490A 54LS/74LS90 DECADE COUNTER

DESCRIPTION — The '90 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divideby-five counter. It can be connected to operate with a conventional BCD output pattern or it can be connected to provide a 50% duty cycle output. In the BCD mode, HIGH signals on the Master Set (MS) inputs set the outputs to BCD nine. HIGH signals on the Master Reset (MR) inputs force all outputs LOW. For a similar counter with corner power pins, see the 'LS290; for dual versions, see the 'LS390 and 'LS490.

ORDERING CODE: See Section 9

	PIN	COMMERCIAL GRADE	MILITARY GRADE	PKG
PKGS	ουτ	V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	$V_{CC} = +5.0 V \pm 10\%,$ $T_A = -55^{\circ}C \text{ to } +125^{\circ}C$	TYPE
Plastic DIP (P)	A	7490APC, 74LS90PC		9A
Ceramic DIP (D)	A	7490ADC, 74LS90DC	5490ADM, 54LS90DM	6A
Flatpak (F)	A	7490AFC, 74LS90FC	5490AFM, 54LS90FM	31

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW	
CP ₀	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	0.125/1.5	
CP ₁	÷5 Section Clock Input (Active Falling Edge)	3.0/3.0	0.250/2.0	
MR1, MR2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25	
MS1, MS2	Asynchronous Master Set (Preset 9) Inputs (Active HIGH)	1.0/1.0	0.5/0.25	
Qo	÷2 Section Output*	20/10	10/5.0 (2.5)	
Q1 — Q3	÷5 Section Outputs	20/10	10/5.0 (2.5)	

*The Q0 output is guaranteed to drive the full rated fan-out plus the \overline{CP}_1 input.



FUNCTIONAL DESCRIPTION — The '90 is a 4-bit ripple type decade counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. A gated AND asynchronous Master Reset (MR₁, MR₂) is provided which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁, MS₂) is provided which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH). Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.:

- A. BCD Decade (8421) Counter The \overline{CP}_1 input must be externally connected to the Q₀ output. The \overline{CP}_0 input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter The Q_3 output must be externally connected to the \overline{CP}_0 input. The input count is then applied to the \overline{CP}_1 input and a divide-by-ten square wave is obtained at output Q_0 .
- C. Divide-By-Two and Divide-By-Five Counter No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain binary divide-by-five operation at the Q_3 output.

RESET/SET INPUTS			OUTPUTS				
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q1	Q3	Q3
н	н	L	Х	L	L	L	Г
н	н	х	L	L	L	L	L
x	x	н	н	н	L	L	н
L	х	L	х	Count			
X	L	х	L	Count			
L	Х	х	L		Co	unt	
х	L	L	Х	Count			

MODE SELECTION

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

BCD COUNT SEQUENCE

COUNT	OUTPUTS					
	Q ₀	Q1	Q2	Q ₃		
0	L	L	L	L		
1	н	L	L	L		
2	L	н	L	L		
3	н	н	L	L		
4	L	L	н	L		
5	н	L	н	L		
6	L	н	н	L		
7	н	н	н	L		
8	L	L	L	н		
9	н	L	L	н		

NOTE: Output Q₀ is connected to Input CP₁ for BCD count.



••••••	PARAMETER	54/74	54/74LS	UNITS	CONDITIONS
SYMBOL		Min Max		UNIT 5	CONDITIONS
Ін	Input HIGH Current, CP0	1.0	0.2	mA	$V_{CC} = Max, V_{IN} = 5.5$
ևո	Input HIGH Current CP1	1.0	0.4	mA	$V_{CC} = Max, V_{IN} = 5.5$
lcc	Power Supply Current	42	15	mA	V _{CC} = Max
AC CHAR	ACTERISTICS: V _{CC} = +5.0 V, T _A = -	54/74	Section 3 for 54/74LS CL = 15 pF	waveforms a	and load configurations)
STMBOL	FARAMETER	$R_L = 400 \Omega$			
f _{max}	Maximum Count Frequency, CP0	Min Max 32	Min Max 32	MHz	Figs. 3-1, 3-9
f _{max}	Maximum Count Frequency, CP1	16	16	MHz	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP ₀ to Q ₀	16 18	16 18	ns	Figs. 3-1, 3-9
tPLH tPHL	Propagation Delay CP0 to Q3	48 50	48 50	ns	Figs. 3-1, 3-9
tplh tphL	Propagation Delay CP1 to Q1	16 21	16 21	ns	Figs. 3-1, 3-9
telh tehl	Propagation Delay CP1 to Q2	32 35	32 35	ns	Figs. 3-1, 3-9
tplH tpHL	Propagation Delay CP1 to Q3	32 35	32 35	ns	Figs. 3-1, 3-9
tplH	Propagation Delay MS to Q ₀ and Q ₃	30	30	ns	Figs. 3-1, 3-17
tPHL	Propagation Delay MS to Q_1 and Q_3	40	40	ns	Figs. 3-1, 3-17
tphL	Propagation Delay MR to Q _n	40	40	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: $V_{CC} = +5.0 \text{ V}, \text{ T}_{A} = +25^{\circ} \text{ C}$

SYMBOL	PARAMETER	54/74	54/74LS	UNITS	CONDITIONS
		Min Ma	x Min Max		
t _w (H)	CP0 Pulse Width HIGH	15	15	ns	Fig. 3-9
t _w (H)	CP1 Pulse Width HIGH	30	30	ns	Fig. 3-9
tw (H)	MS Pulse Width HIGH	15	15	ns	Fig. 3-17
tw (H)	MR Pulse Width HIGH	15	15	ns	Fig. 3-17
trec	Recovery Time, MS to CP	25	25	ns	Fig. 3-17
trec	Recovery Time, MR to CP	25	25	ns	Fig. 3-17

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