



54AC/74AC648

Octal Transceiver/Register with TRI-STATE® Outputs

General Description

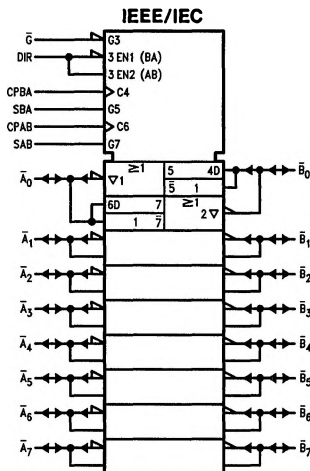
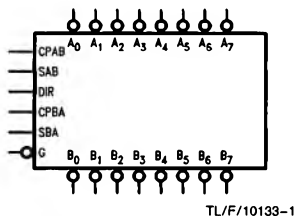
The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1 thru 4* (See Page 2).

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

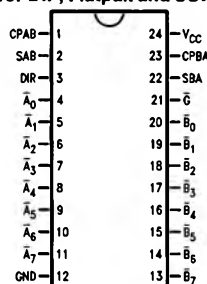
Ordering Code: See Section 8

Logic Symbols

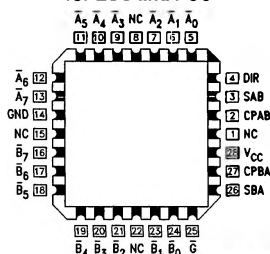


Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC



Pin Names	Description
$\bar{A}_0$ – $\bar{A}_7$	Data Register A Inputs, Data Register A TRI-STATE Outputs
$\bar{B}_0$ – $\bar{B}_7$	Data Register B Inputs, Data Register B TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\bar{G}$	Output Enable Inputs

Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A ₀ –A ₇	B ₀ –B ₇	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	$\nearrow$	X	X	X			Clock A _n Data into A Register
H	X	X	$\nearrow$	X	X			Clock B _n Data into B Register
L	H	X	X	L	X	Input	Output	A _n to B _n —Real Time (Transparent Mode)
L	H	$\nearrow$	X	L	X			Clock A _n Data into A Register
L	H	H or L	X	H	X			A Register to B _n (Stored Mode)
L	H	$\nearrow$	X	H	X			Clock A _n Data into A Register and Output to B _n
L	L	X	X	X	L	Output	Input	B _n to A _n —Real Time (Transparent Mode)
L	L	X	$\nearrow$	X	L			Clock B _n Data into B Register
L	L	X	H or L	X	H			B Register to A _n (Stored Mode)
L	L	X	$\nearrow$	X	H			Clock B _n Data into B Register and Output to A _n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Irrelevant

$\nearrow$ = LOW-to-HIGH Transition

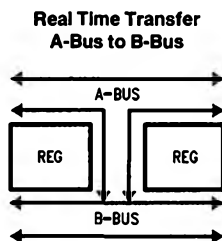


FIGURE 1

TL/F/10133-7

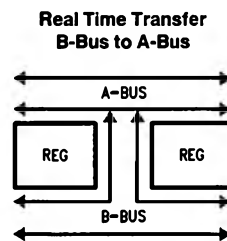


FIGURE 2

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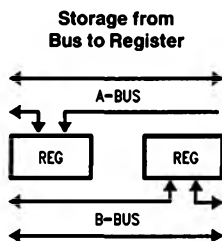


FIGURE 3

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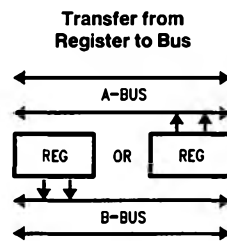
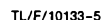


FIGURE 4

TL/F/10133-10



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		2.1		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15		3.15			
		5.5	2.75	3.85	3.85		3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		0.9		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35		1.35			
		5.5	2.75	1.65	1.65		1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		2.9		V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		4.4			
		5.5	5.49	5.4	5.4		5.4			
		3.0		2.56	2.4		2.46		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7		3.76			
		5.5		4.86	4.7		4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		0.1			
		5.5	0.001	0.1	0.1		0.1			
		3.0		0.36	0.50		0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.50		0.44			
		5.5		0.36	0.50		0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		±1.0		μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50		−75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0		80.0		μA	V _{IN} = V _{CC} or GND
I _{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0		±6.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.5 1.5	10.0 7.0	15.5 11.0			1.5 1.5	17.0 12.0	ns	2-3, 4
t _{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10.5			1.5 1.5	14.5 11.5	ns	2-3, 4
t _{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	6.0 4.0	10.0 7.0			1.5 1.0	11.0 7.5	ns	2-3, 4
t _{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	5.5 3.5	9.0 7.5			1.5 1.0	10.0 8.0	ns	2-3, 4
t _{PLH}	Propagation Delay SBA or SAB to A _n or B _n (with A _n or B _n HIGH or LOW)	3.3 5.0	1.5 1.5	7.5 5.5	12.5 9.0			1.5 1.5	14.0 10.0	ns	2-3, 4
t _{PHL}	Propagation Delay SBA or SAB to A _n or B _n (with A _n or B _n HIGH or LOW)	3.3 5.0	1.5 1.5	7.5 5.5	12.5 9.5			1.5 1.5	14.0 10.5	ns	2-3, 4
t _{PZH}	Enable Time G̅ to A _n or B _n	3.3 5.0	1.5 1.5	6.5 5.0	11.0 8.0			1.0 1.0	11.5 9.0	ns	2-5
t _{PZL}	Enable Time G̅ to A _n or B _n	3.3 5.0	1.5 1.5	7.0 5.0	11.0 8.0			1.0 1.0	12.5 9.0	ns	2-6
t _{PHZ}	Disable Time G̅ to A _n or B _n	3.3 5.0	1.5 1.5	7.5 6.0	12.0 10.0			1.0 1.0	13.0 11.0	ns	2-5
t _{PLZ}	Disable Time G̅ to A _n or B _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0			1.0 1.0	12.5 10.0	ns	2-6
t _{PZH}	Enable Time DIR to A _n or B _n	3.3 5.0	1.5 1.5	6.0 4.5	12.5 9.5			1.0 1.0	14.0 10.5	ns	2-5
t _{PZL}	Enable Time DIR to A _n or B _n	3.3 5.0	1.5 1.5	6.5 4.5	13.0 9.0			1.5 1.0	14.5 10.5	ns	2-6
t _{PHZ}	Disable Time DIR to A _n or B _n	3.3 5.0	1.5 1.5	7.0 5.5	11.5 9.0			1.0 1.0	13.5 10.0	ns	2-5
t _{PLZ}	Disable Time DIR to A _n or B _n	3.3 5.0	1.5 1.5	7.0 5.0	13.5 9.5			1.5 1.0	15.0 10.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} * (V)	74AC		54AC	74AC	Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -55°C to +125°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW, Bus to Clock	3.3	2.0	3.0		3.5	ns	2-7
		5.0	1.5	2.0		2.0		
t _h	Hold Time, HIGH or LOW, Bus to Clock	3.3	-1.5	0		0	ns	2-7
		5.0	-0.5	1.0		1.0		
t _w	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5		4.0	ns	2-3
		5.0	2.0	3.0		3.0		

*Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	65.0	pF	V _{CC} = 5.0V
C _{I/O}	Input/Output Capacitance	15.0	pF	V _{CC} = 5.0V