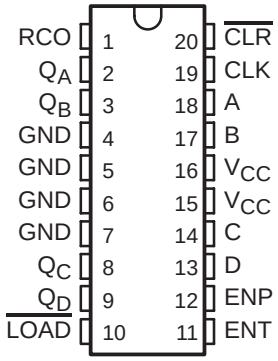
SCAS170 − D3624, AUGUST 1990 − REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Synchronously Programmable**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

This synchronous, presettable 4-bit decade counter features an internal carry look-ahead circuitry for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock-input waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load ($\overline{LOAD}$) input disables the counter and causes the outputs to agree with the setup data after the next clock rising edge regardless of the levels of the enable inputs. The clear function for the 74ACT11160 is asynchronous, and a low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (ENP and ENT) inputs and a ripple-carry (RCO) output. Both count-enable inputs must be held high to count, and ENT is fed forward to enable RCO. RCO thus enabled will produce a high-level pulse while the count is 9 (HLLH). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed regardless of the level of the clock input.

This counter features a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.

The 74ACT11160 is characterized for operation from −40°C to 85°C.

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TEXAS INSTRUMENTS
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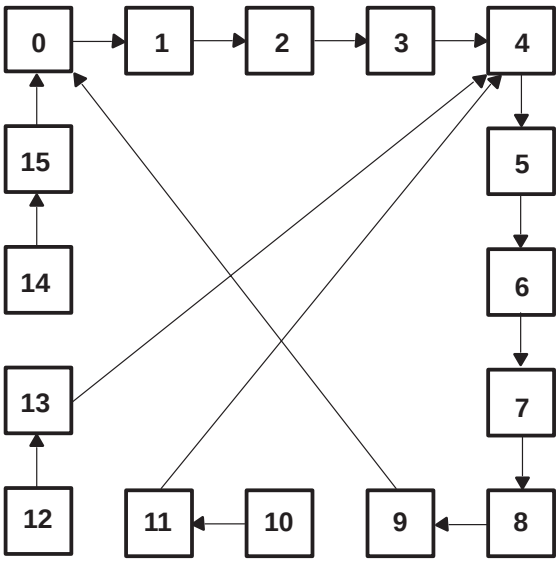
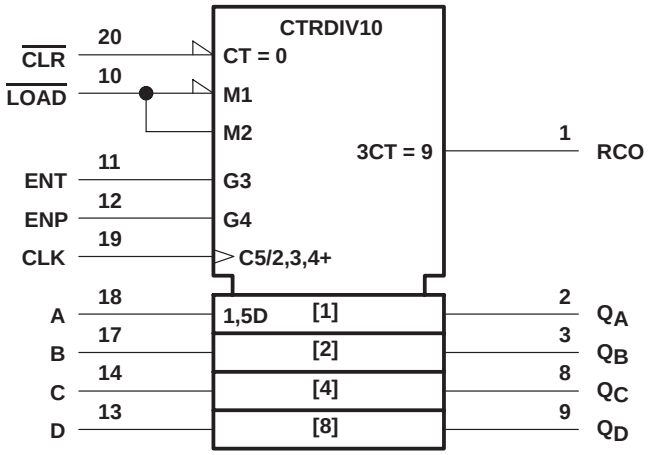
state diagram



logic symbol†

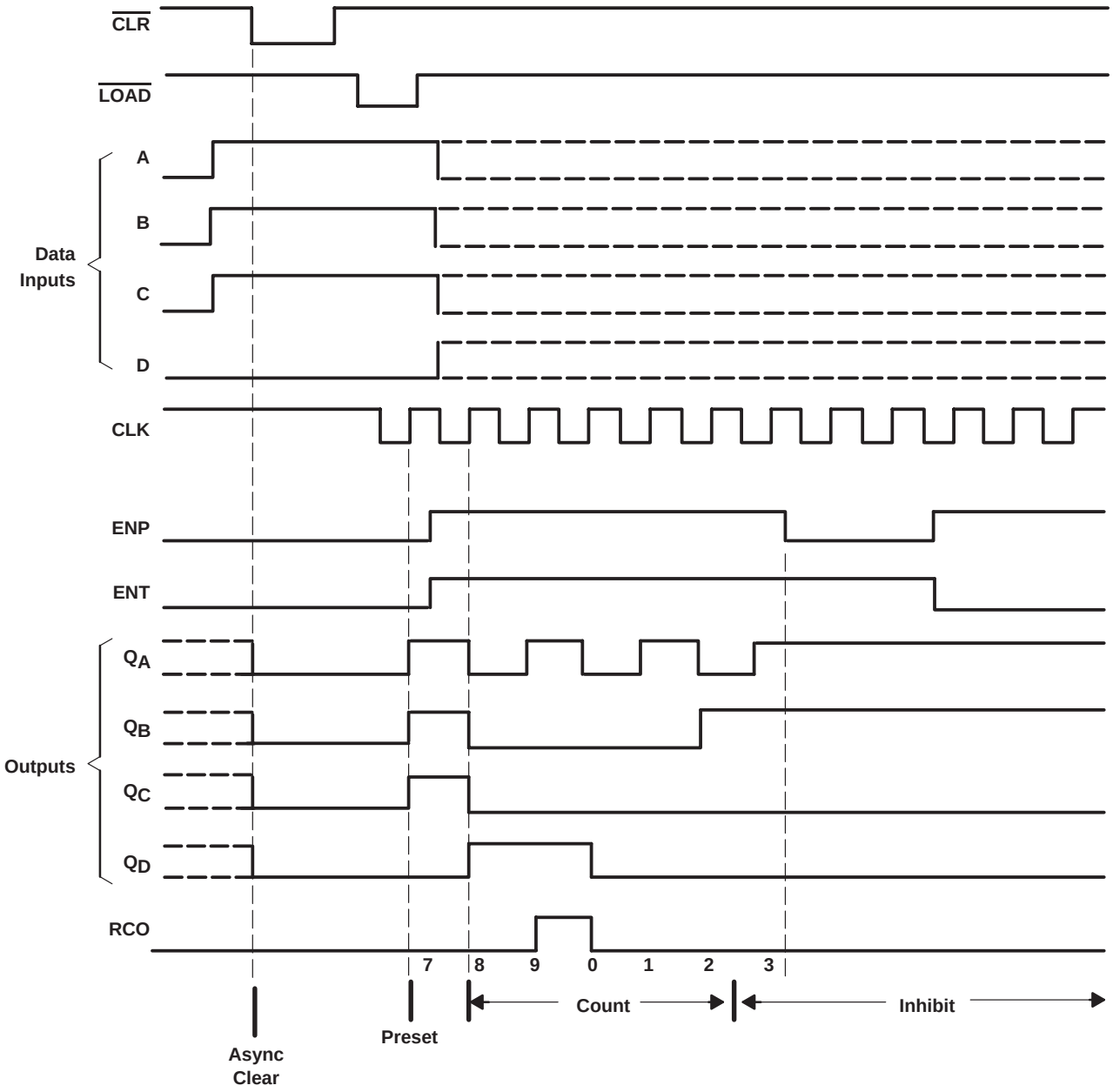


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

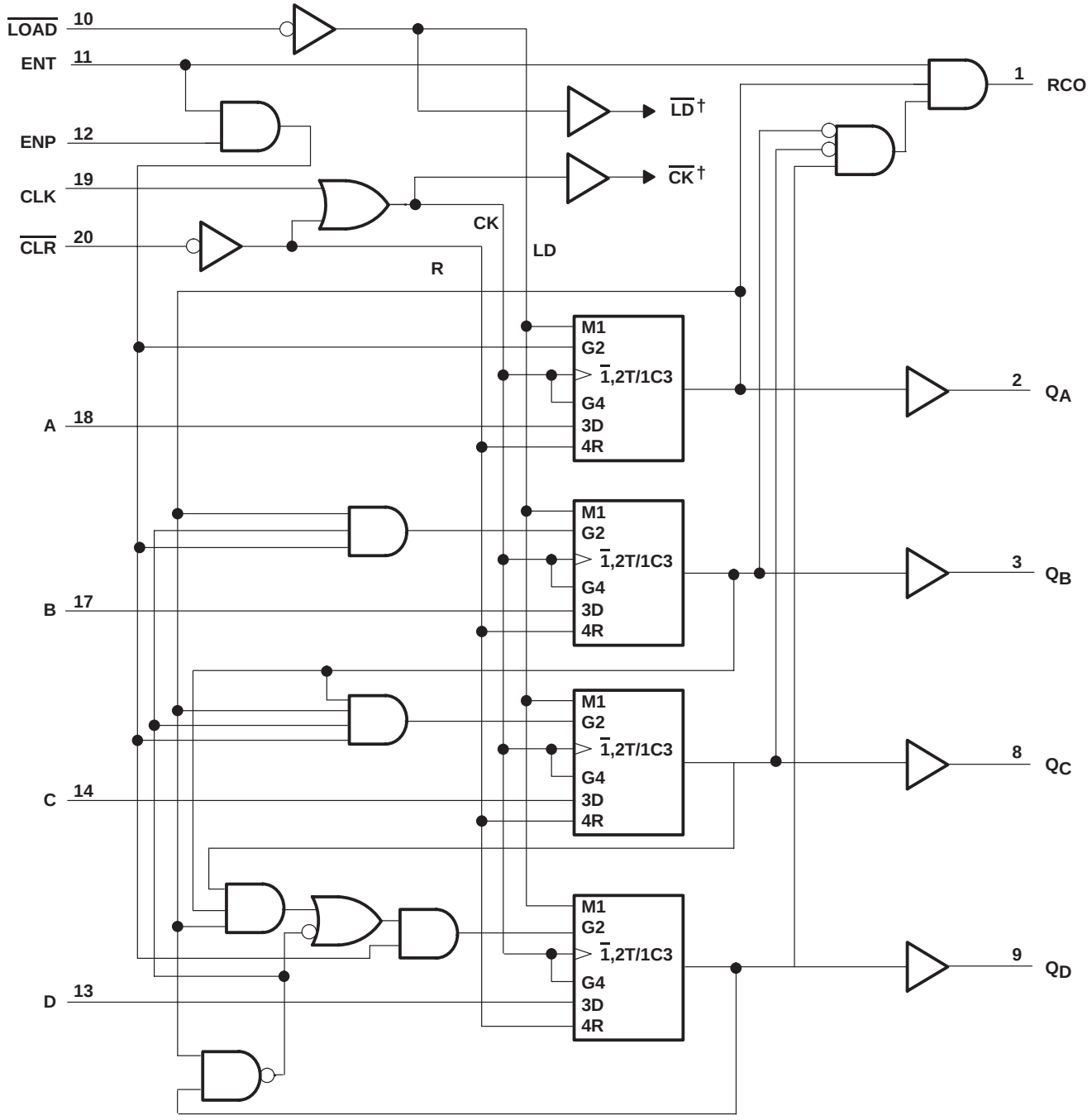
output sequence

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine (RCO high), zero, one, two, and three
4. Inhibit counting

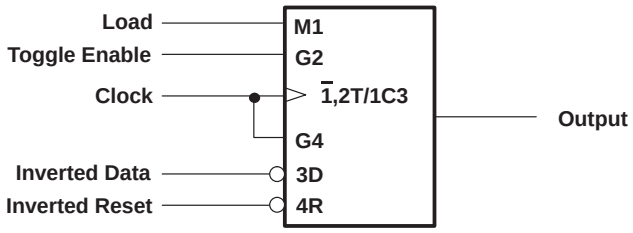


logic diagram (positive logic)

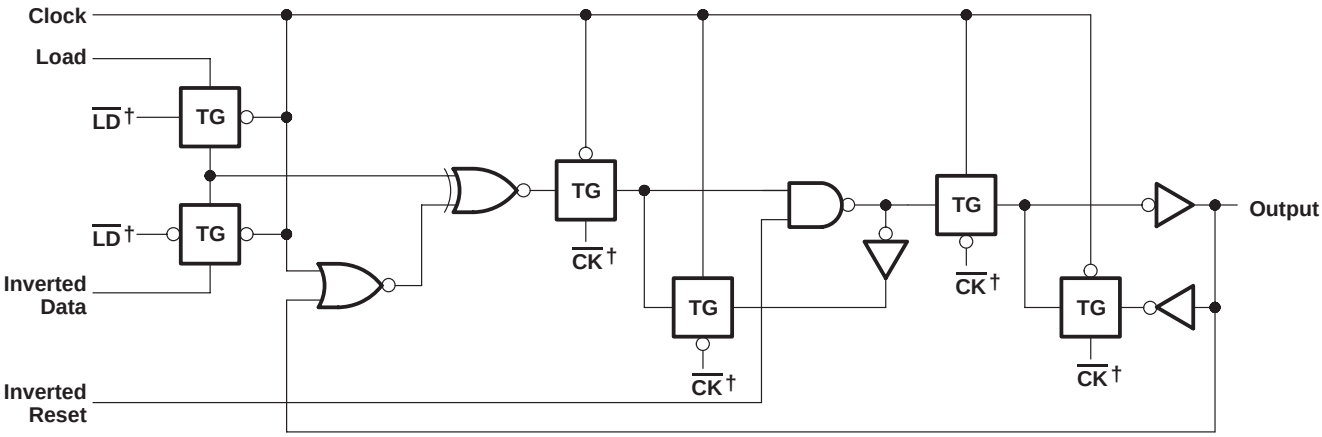


† For the sake of simplicity, the routing of the complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

logic symbol, each D/T flip-flop (positive logic)



logic diagram, each D/T flip-flop (positive logic)



† The origins of the signals $\overline{LD}$ and $\overline{CK}$ are shown in the logic diagram of the overall device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±125 mA
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 µA		4.5 V	4.4			4.4		V
			5.5 V	5.4			5.4		
	I_{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA†		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
			5.5 V			0.1		0.1	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA†		5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			8		80	µA
ΔI_{CC}‡	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		3.5				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	100	0	100	MHz
t_w	Pulse duration	CLK high or low	5		5		ns
		$\overline{CLR}$ low	5		5		
t_{su}	Setup time before CLK↑	A, B, C, D	1		1		ns
		$\overline{LOAD}$	7		7		
		ENP, ENT	7		7		
		$\overline{CLR}$ inactive	5		5		
		$\overline{CLR}$ low	5		5		
		$\overline{CLR}$ high (inactive)	5		5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		ns

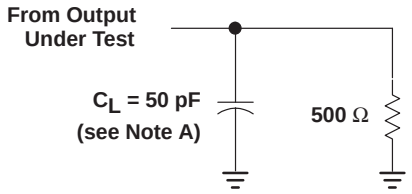
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			100	125		100		MHz
t_{PLH}	CLK	RCO	3.8	6.9	9.1	3.8	10.1	ns
t_{PHL}			4.4	8.3	10.8	4.4	12	
t_{PLH}	CLK	Any Q	2.8	5.8	8.3	2.8	9.1	ns
t_{PHL}			3.5	6.7	9.1	3.5	10.2	
t_{PLH}	ENT	RCO	2.3	4.3	5.6	2.3	6	ns
t_{PHL}			3.1	6.7	9.2	3.1	10.1	
t_{PHL}	$\overline{CLR}$	Any Q	4.4	8.7	11.9	4.4	13.2	ns
t_{PHL}	$\overline{CLR}$	RCO	5.4	10.1	13.2	5.4	14.7	ns

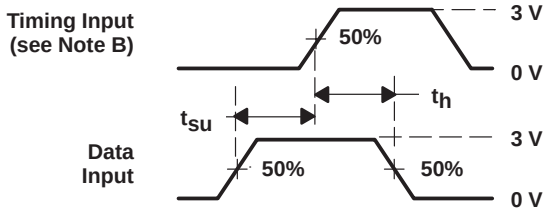
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	Outputs enabled	C_L = 50 pF,	f = 1 MHz	60	pF

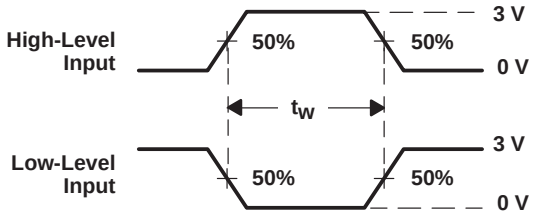
PARAMETER MEASUREMENT INFORMATION



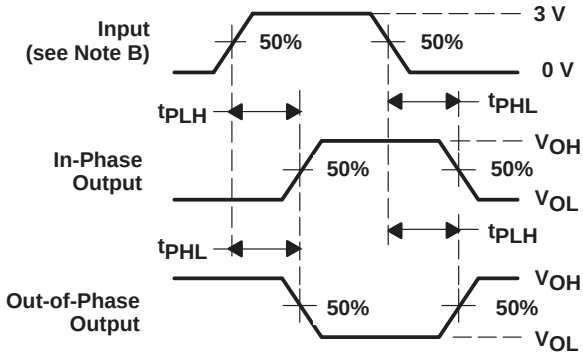
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. For testing f_{max} and pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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