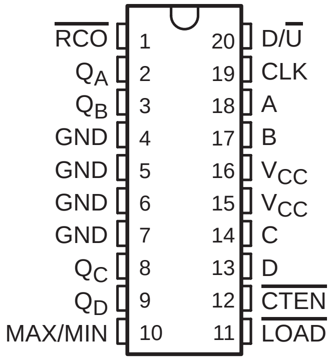
74ACT11191
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

SCAS106A − D3455, FEBRUARY 1990 − REVISED APRIL 1993

- **Inputs Are TTL-Voltage Compatible**
- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



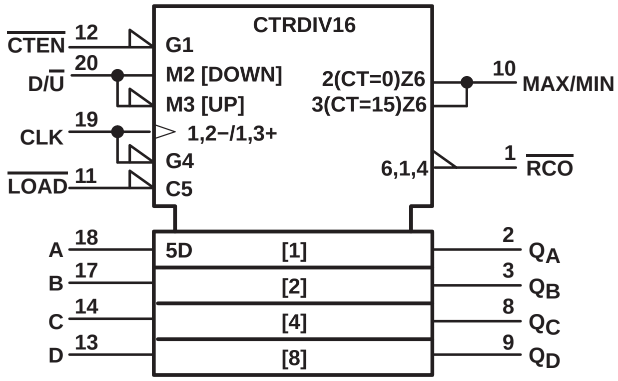
description

The 74ACT11191 is a synchronous, 4-bit binary reversible up/down counter. A synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{\text{CTEN}}$) is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{\text{U}}$) input. When D/$\overline{\text{U}}$ is low, the counter counts up and when D/$\overline{\text{U}}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{\text{CTEN}}$ and D/$\overline{\text{U}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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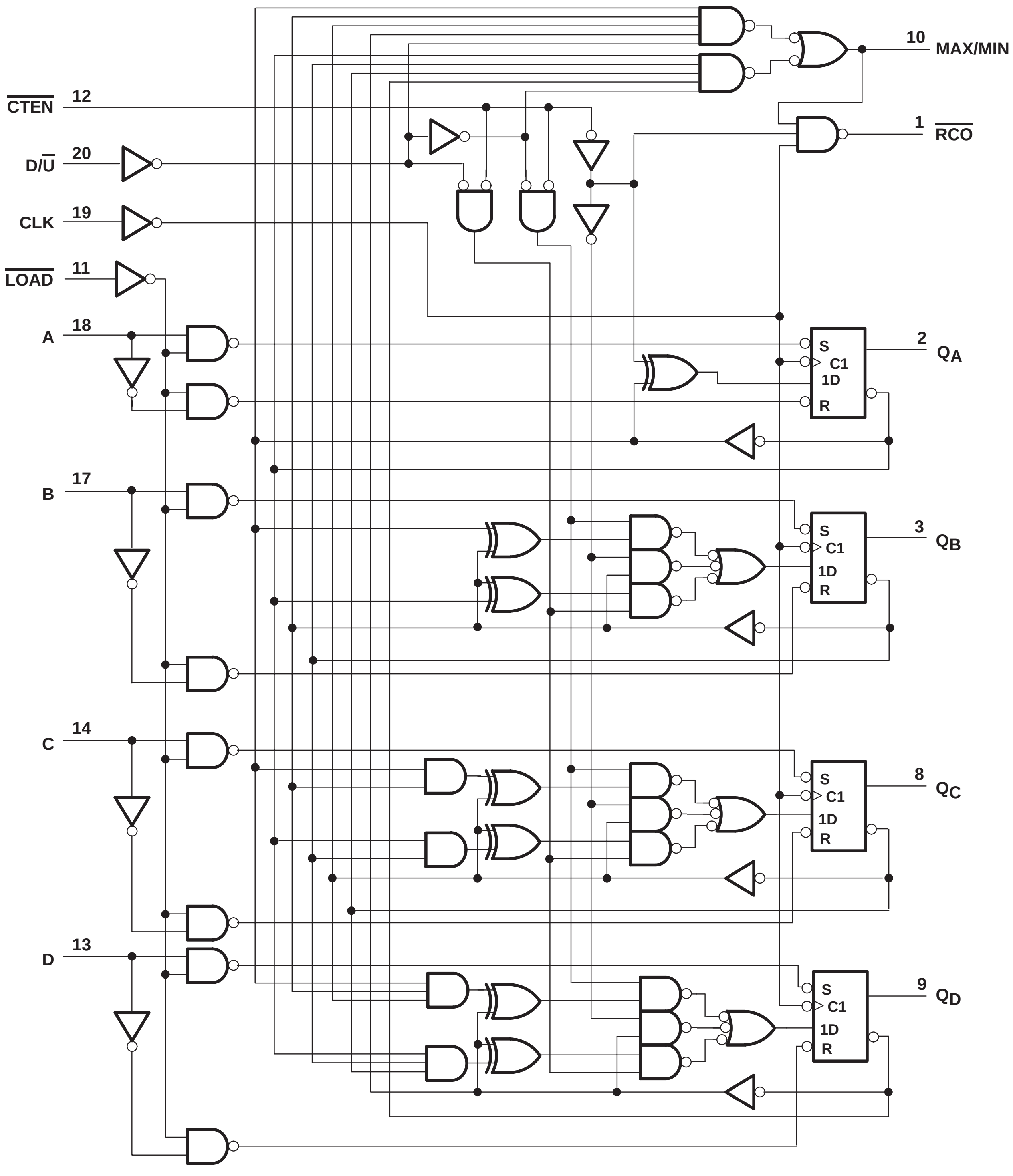
description (continued)

These counters are fully programmable; that is, they may be preset to any number between 0 and 15 by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counter to be used as a modulo-N divider by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (15) counting up. The ripple clock output ($\overline{\text{ROC}}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counter can easily be cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The 74ACT11191 is characterized for operation from − 40°C to 85°C.

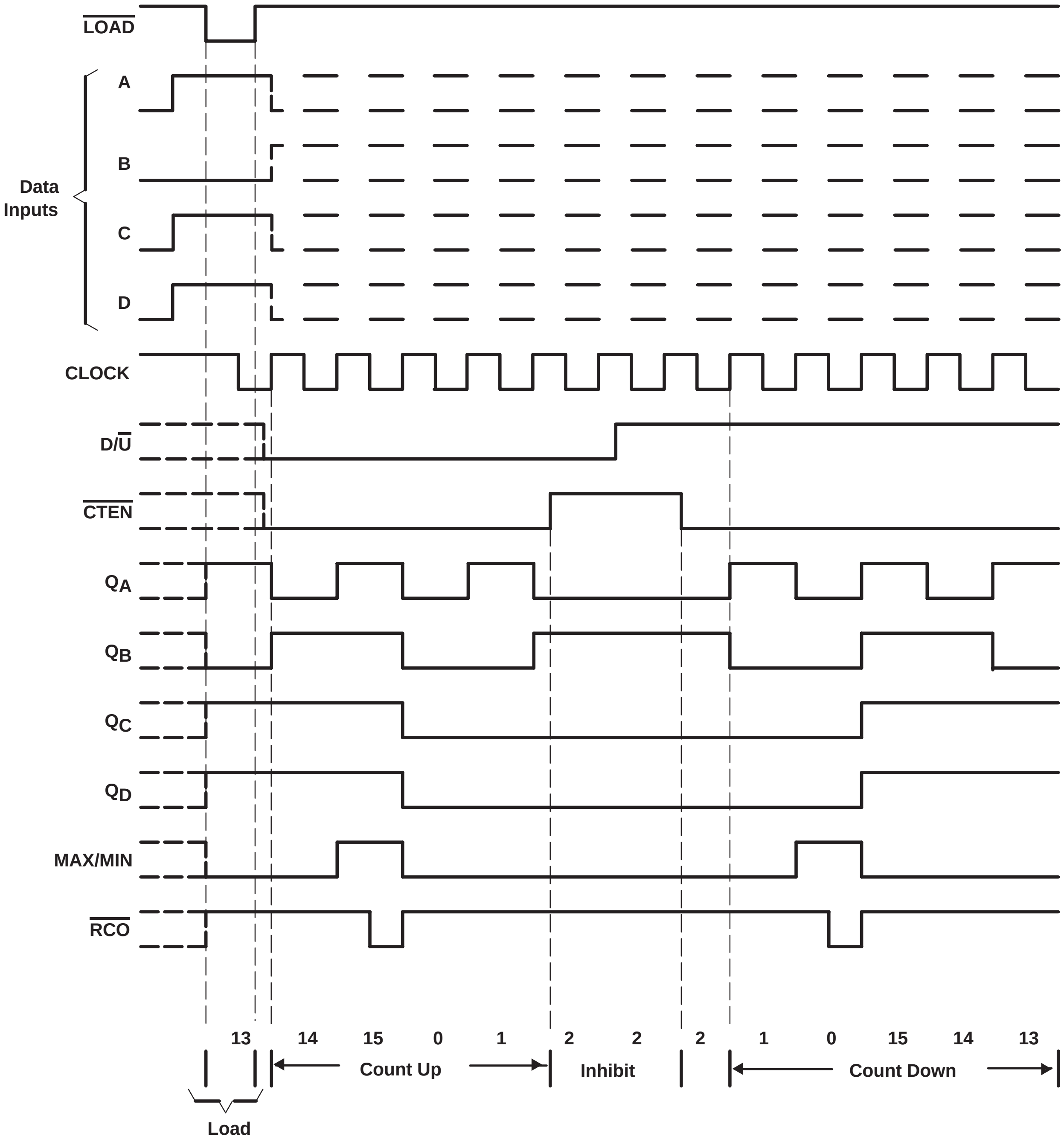
logic diagram (positive logic)



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±50 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage		2	V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		−24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	− 40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = − 50 µA	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	I_{OH} = − 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = − 75 mA[‡]	5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA[‡]	5.5 V					1.65	
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	µA
ΔI_{CC}[§]	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4				pF

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			T_A = 25°C				
			MIN	**MAX**	**MIN**	**MAX**	**UNIT**
f_{clock}	Clock frequency		0	65	0	65	MHz
t_w	Pulse duration	$\overline{\text{LOAD}}$ low	4		4		ns
		CLK high or low	7.7		7.7		
t_{su}	Setup time	Data before $\overline{\text{LOAD}}$↓	3		3		ns
		$\overline{\text{CTEN}}$ before CLK↑	7.5		7.5		
		D/$\overline{\text{U}}$ before CLK↑	8.5		8.5		
		$\overline{\text{LOAD}}$ inactive before CLK↑	2		2		
t_h	Hold time	Data after $\overline{\text{LOAD}}$↓	2.5		2.5		ns
		$\overline{\text{CTEN}}$ after CLK↑	1.5		1.5		
		D/$\overline{\text{U}}$ after CLK↑	0.5		0.5		

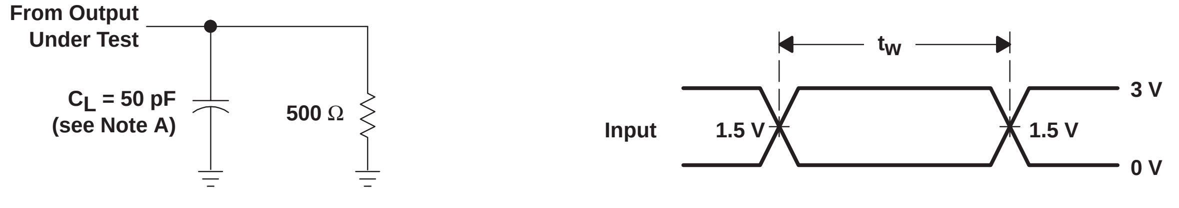
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			65	95		65		MHz
t_{PLH}	$\overline{\text{LOAD}}$	Any Q	4	7.6	10.8	4	12.2	ns
t_{PHL}			3.8	7.4	10.5	3.8	11.9	
t_{PLH}	$\overline{\text{LOAD}}$	MAX/MIN	5.2	9.7	13.9	5.2	15.8	ns
t_{PHL}			4.7	9.5	13.6	4.7	15.4	
t_{PLH}	$\overline{\text{LOAD}}$	$\overline{\text{RCO}}$	5.4	10.5	15.1	5.4	17.1	ns
t_{PHL}			5.8	11	15.7	5.8	17.9	
t_{PLH}	A, B, C, or D	Any Q	4.5	7.6	10.1	4.5	11.6	ns
t_{PHL}			3.7	7.1	10.3	3.7	11.7	
t_{PLH}	A, B, C, or D	MAX/MIN	5.1	9.5	13.6	5.1	15.4	ns
t_{PHL}			4.7	9.2	13.4	4.7	15.2	
t_{PLH}	A, B, C, or D	$\overline{\text{RCO}}$	5.5	10.3	14.8	5.5	17.2	ns
t_{PHL}			5.9	10.9	15.5	5.9	18	
t_{PLH}	CLK	$\overline{\text{RCO}}$	4.4	7.4	9.5	4.4	11	ns
t_{PHL}			3.5	6.7	9.5	3.5	10.8	
t_{PLH}	CLK	Any Q	3.6	6.7	9.2	3.6	10.4	ns
t_{PHL}			4.2	7.1	9.4	4.2	10.8	
t_{PLH}	CLK	MAX/MIN	5	8	10.3	5	11.7	ns
t_{PHL}			5.3	8.6	11.5	5.3	13.1	
t_{PLH}	D/$\overline{\text{U}}$	$\overline{\text{RCO}}$	4.4	8.4	11.7	4.4	13.1	ns
t_{PHL}			4.2	8.8	11.3	4.2	13	
t_{PLH}	D/$\overline{\text{U}}$	MAX/MIN	3.2	6.9	9.6	3.2	11	ns
t_{PHL}			3.6	7.2	10.3	3.6	11.6	
t_{PLH}	$\overline{\text{CTEN}}$	$\overline{\text{RCO}}$	3.9	6.4	8.2	3.9	9.2	ns
t_{PHL}			2.8	6	8.4	2.8	9.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

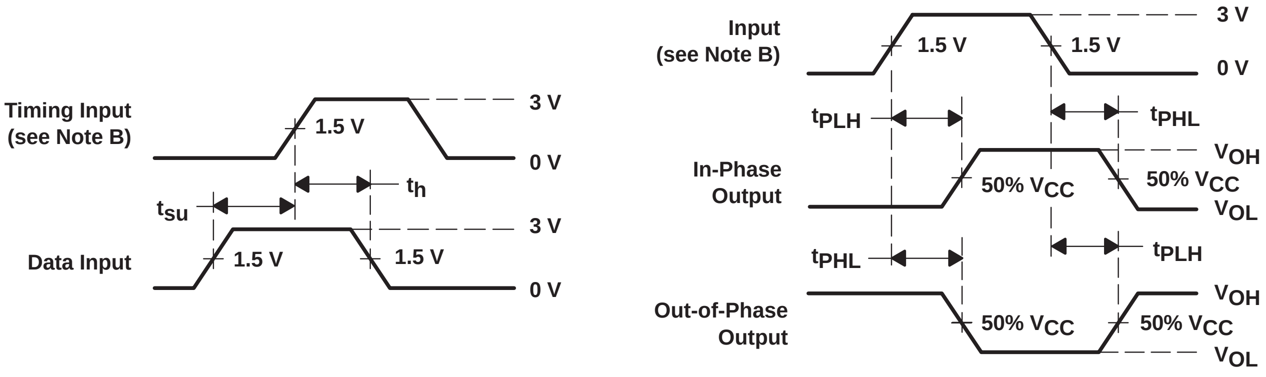
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	68	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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