- **Members of the Texas Instruments**
  ***Widebus*™ Family**

- **Inputs Are TTL-Voltage Compatible**

- **Flow-Through Architecture Optimizes**
  PCB Layout

- **Distributed V_{CC} and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- ***EPIC*™ (Enhanced-Performance Implanted**
  CMOS) 1-μm Process

- **500-mA Typical Latch-Up Immunity at**
  125°C

- **Package Options Include Plastic 300-mil**
  Shrink Small-Outline (DL) Packages Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Packages Using 25-mil Center-to-Center
  Pin Spacings

54ACT16657 . . . WD PACKAGE
74ACT16657 . . . DL PACKAGE
(TOP VIEW)

1OE	1	56	1T/R
NC	2	55	1ODD/EVEN
1ERR	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
VCC	7	50	VCC
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
VCC	22	35	VCC
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2ERR	26	31	2PARITY
NC	27	30	2ODD/EVEN
2OE	28	29	2T/R

NC – No internal connection

description

The 'ACT16657 contain two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive (1T/$\overline{R}$ or 2T/$\overline{R}$) input determines the direction of data flow. When 1T/$\overline{R}$ (or 2T/$\overline{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when 1T/$\overline{R}$ (or 2T/$\overline{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable (1$\overline{OE}$ or 2$\overline{OE}$) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. 1PARITY (or 2PARITY) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, 1PARITY (or 2PARITY) is set to the logic level that maintains the parity sense selected by the level at the 1ODD/$\overline{EVEN}$ (or 2ODD/$\overline{EVEN}$) input. For example, if 1ODD/$\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then 1PARITY is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Copyright © 1996, Texas Instruments Incorporated

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

description (continued)

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the 1$\overline{\text{ERR}}$ (or 2$\overline{\text{ERR}}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if 1ODD/$\overline{\text{EVEN}}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then 1$\overline{\text{ERR}}$ is low, indicating a parity error.

The 74ACT16657 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16657 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16657 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	$\overline{\text{OE}}$	T/$\overline{\text{R}}$	ODD/$\overline{\text{EVEN}}$		$\overline{\text{ERR}}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
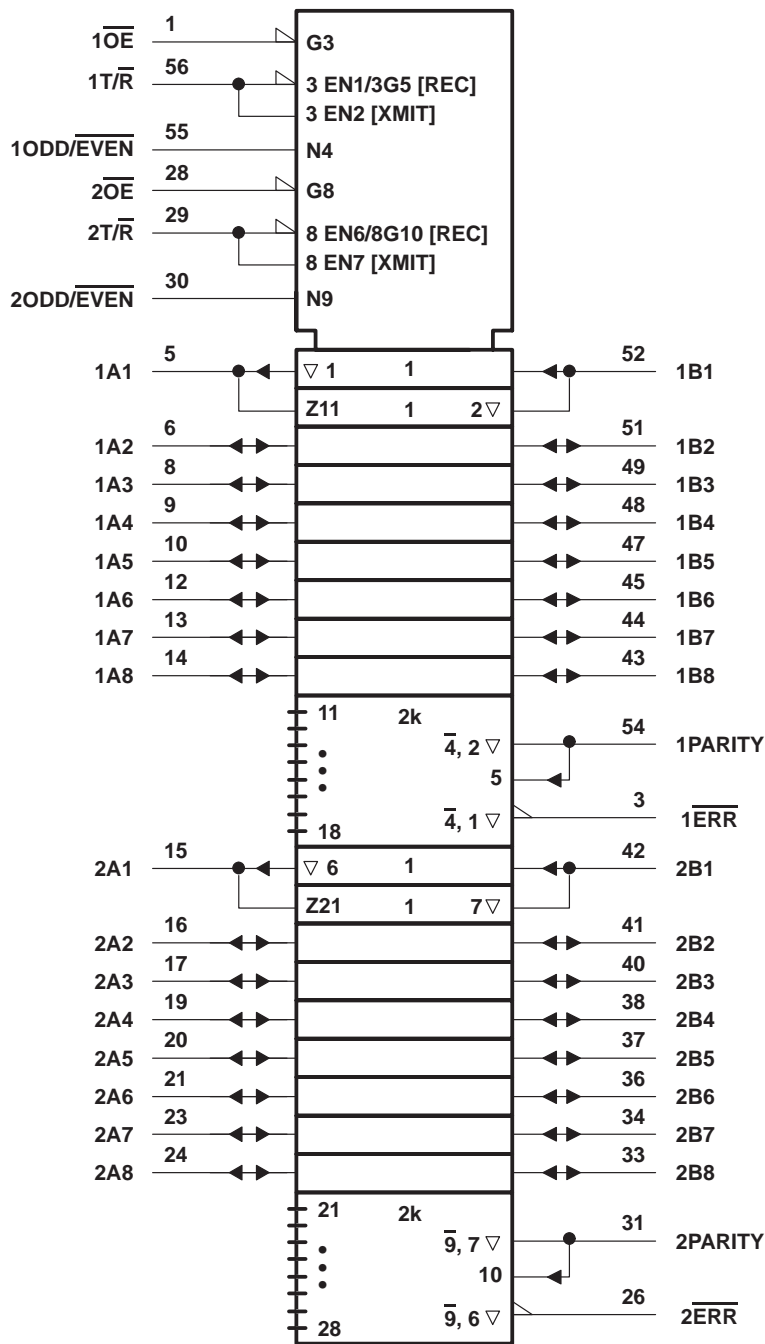
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each transceiver (positive logic)
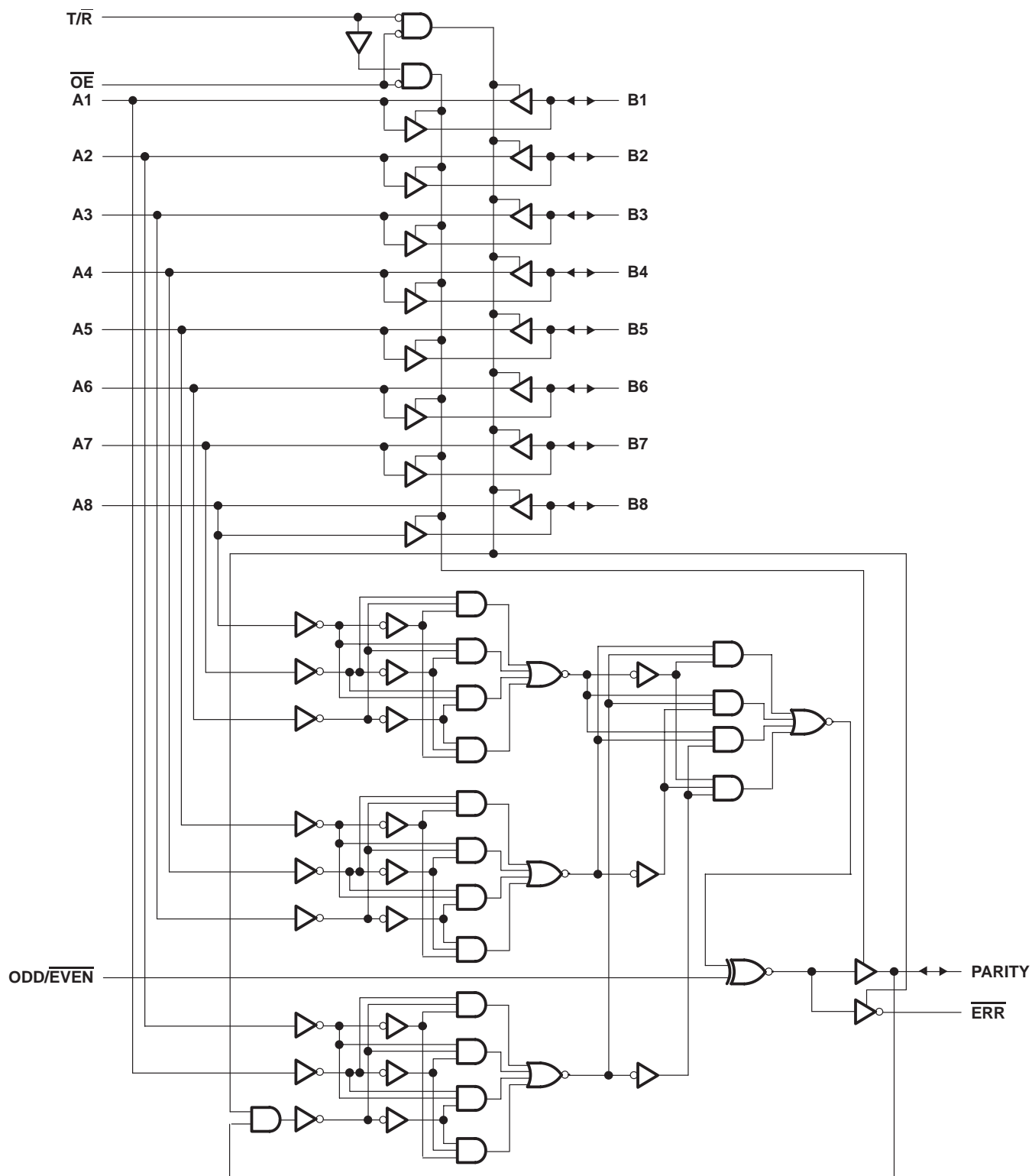
TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±500 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.4 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
   2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16657			74ACT16657			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

TEXAS
INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_CC	T_A = 25°C			54ACT16657		74ACT16657		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_OH		I_OH = −50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_OH = −24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I_OH = −75 mA†	5.5 V				3.85		3.85		
V_OL		I_OL = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_OL = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I_OL = 75 mA†	5.5 V					1.65		1.65	
I_I	A or B ports	V_I = V_CC or GND	5.5 V		±0.1			±1		±1	µA
I_OZ‡	Control inputs	V_O = V_CC or GND	5.5 V		±0.5			±5		±5	µA
I_CC		V_I = V_CC or GND, I_O = 0	5.5 V		8			80		80	µA
ΔI_CC§		One input at 3.4 V, Other inputs at V_CC or GND	5.5 V		0.9			1		1	mA
C_i	Control inputs	V_I = V_CC or GND	5 V		4.5						pF
C_o	$\overline{ERR}$	V_O = V_CC or GND	5 V		11						pF
C_io	A or B ports	V_O = V_CC or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_OZ includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_CC.

switching characteristics over recommended operating free-air temperature range, V_CC = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16657		74ACT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_PLH	A or B	B or A	4.1	7.3	9.6	4.1	10.7	4.1	10.7	ns
t_PHL			3.2	6.8	9.8	3.2	10.6	3.2	10.6	
t_PLH	A	PARITY	4	8.6	12.9	4	14.3	4	14.3	ns
t_PHL			4.3	9	13.1	4.3	14.3	4.3	14.3	
t_PLH	ODD/$\overline{EVEN}$	PARITY, $\overline{ERR}$	3.7	8.3	12.3	3.7	13.7	3.7	13.7	ns
t_PHL			4.1	8.8	12.8	4.1	14.1	4.1	14.1	
t_PLH	B	$\overline{ERR}$	3.9	8.6	13	3.9	14.6	3.9	14.6	ns
t_PHL			4.3	9	13.3	4.3	14.7	4.3	14.7	
t_PLH	PARITY	$\overline{ERR}$	3.8	8.4	12.2	3.8	13.8	3.8	13.8	ns
t_PHL			4.1	8	12.8	4.1	14.2	4.1	14.2	
t_PZH	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	2.6	6.1	10.1	2.6	11.3	2.6	11.3	ns
t_PZL			3.2	7.2	11.7	3.2	13	3.2	13	
t_PHZ	$\overline{OE}$	A, B, PARITY, or $\overline{ERR}$	5.9	8.6	10.5	5.9	11.2	5.9	11.2	ns
t_PLZ			5.3	8	9.8	5.3	10.5	5.3	10.5	

![TEXAS INSTRUMENTS logo]

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	76	pF
	Outputs disabled			35	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS
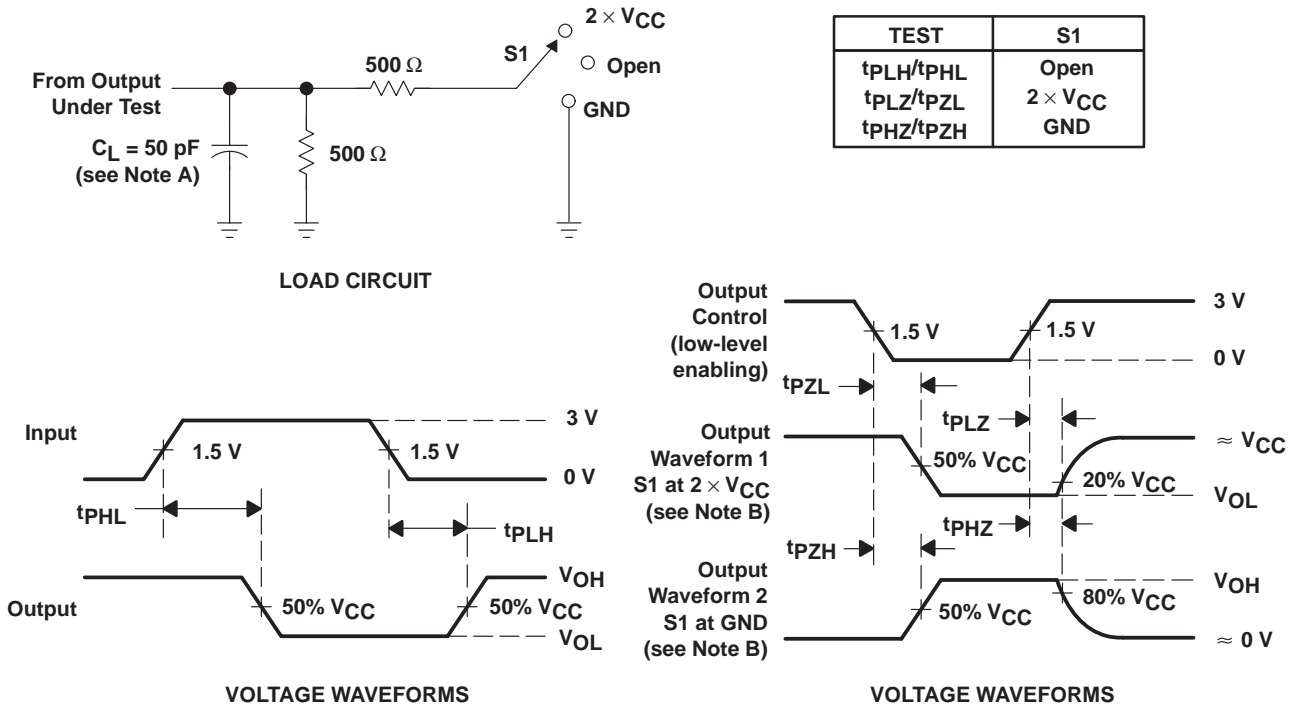
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ACT16657DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16657DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16657DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16657DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

|		
A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	
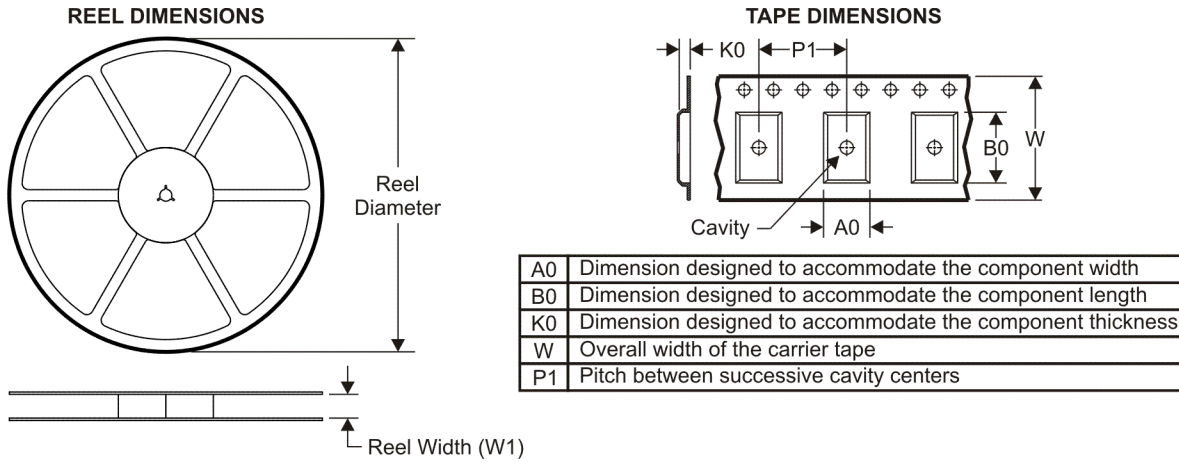
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
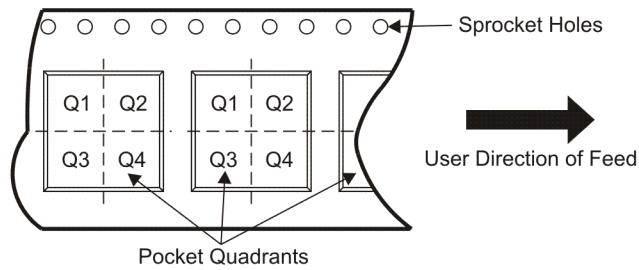
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16657DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS
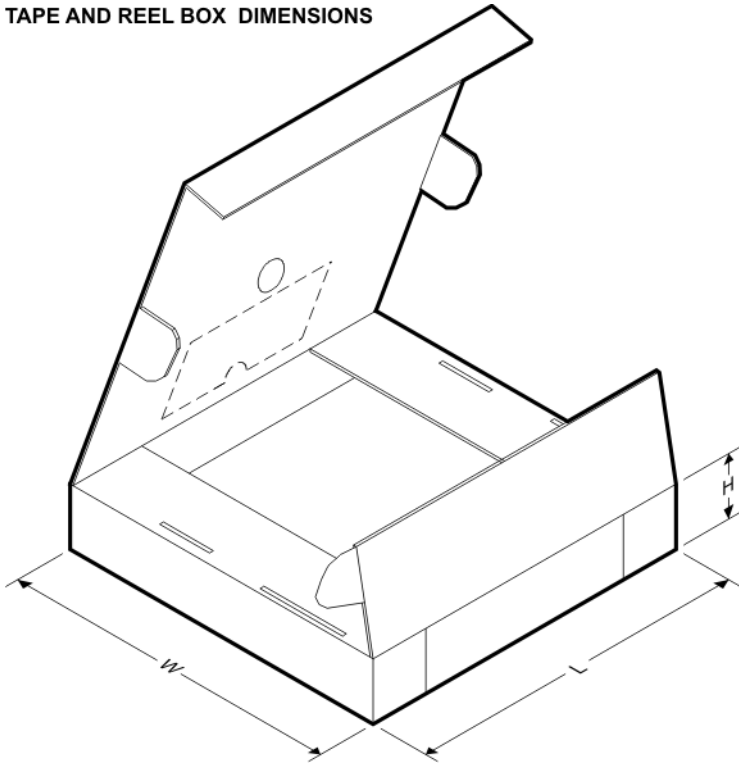
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16657DLR	SSOP	DL	56	1000	346.0	346.0	49.0

IMPORTANT NOTICE