

January 2008

74AC245, 74ACT245 Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Non-inverting buffers
- Bidirectional data path
- A and B outputs source/sink 24mA
- ACT245 has TTL-compatible inputs

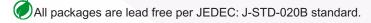
General Description

The AC/ACT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24mA at both the A and B ports. The Transmit/Receive (T/\overline{R}) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

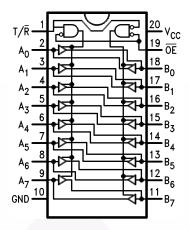
Ordering Information

Order Number	Package Number	Package Description
74AC245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



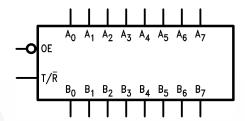
Connection Diagram



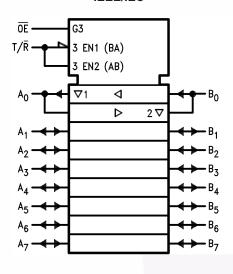
Pin Description

Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A 3-STATE Inputs or 3-STATE Outputs
B ₀ –B ₇	Side B 3-STATE Inputs or 3-STATE Outputs

Logic Symbol



IEEE/IEC



Truth Table

Inputs		
ŌĒ	T/R	Outputs
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +7.0V
I _{IK}	DC Input Diode Current	
	$V_{I} = -0.5V$	-20mA
	$V_{I} = V_{CC} + 0.5$	+20mA
V _I	DC Input Voltage	-0.5V to V _{CC} + 0.5V
I _{OK}	DC Output Diode Current	
	$V_{O} = -0.5V$	-20mA
	$V_{O} = V_{CC} + 0.5V$	+20mA
V _O	DC Output Voltage	-0.5V to V _{CC} + 0.5 V
Io	DC Output Source or Sink Current	±50mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current per Output Pin	±50mA
T _{STG}	Storage Temperature	-65°C to +150°C
T _J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating		
V _{CC}	Supply Voltage			
	AC	2.0V to 6.0V		
	ACT	4.5V to 5.5V		
VI	Input Voltage			
Vo	Output Voltage			
T _A	Operating Temperature -40°C to +85			
ΔV / Δt	Minimum Input Edge Rate, AC Devices: 125mV			
	V _{IN} from 30% to 70% of V _{CC} , V _{CC} @ 3.3V, 4.5V, 5.5V			
ΔV / Δt	Minimum Input Edge Rate, ACT Devices: 125mV/n			
	V _{IN} from 0.8V to 2.0V, V _{CC} @ 4.5V, 5.5V			

DC Electrical Characteristics for AC

				T _A = -	⊦25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.	G	uaranteed Limits	Units
V _{IH}	Minimum HIGH Level	3.0	$V_{OUT} = 0.1V$ or	1.5	2.1	2.1	V
	Input Voltage	4.5	V _{CC} – 0.1V	2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V _{IL}	Maximum LOW Level	3.0	$V_{OUT} = 0.1V$ or	1.5	0.9	0.9	V
	Input Voltage	4.5	V _{CC} – 0.1V	2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V _{OH}	Minimum HIGH Level	3.0	$I_{OUT} = -50\mu A$	2.99	2.9	2.9	V
	Output Voltage	4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -12\text{mA}$		2.56	2.46	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}$		3.86	3.76	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}^{(1)}$		4.86	4.76	
V _{OL}	Maximum LOW Level	3.0	$I_{OUT} = 50\mu A$	0.002	0.1	0.1	V
	Output Voltage	4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 12\text{mA}$		0.36	0.44	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}^{(1)}$		0.36	0.44	
I _{IN} ⁽²⁾	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I _{OLD}	Minimum Dynamic	5.5	V _{OLD} = 1.65V Max.			75	mA
I _{OHD}	Output Current ⁽³⁾	5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC} ⁽²⁾	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA
I _{OZT}	Maximum I/O Leakage Current	5.5	V_{I} (OE) = V_{IL} , V_{IH} ; V_{I} = V_{CC} , GND; V_{O} = V_{CC} , GND		±0.3	±3.0	μА

Notes:

- 1. All outputs loaded; thresholds on input associated with output under test.
- 2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .
- 3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

				T _A = -	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.	G	uaranteed Limits	Units
V _{IH}	Minimum HIGH Level	4.5	$V_{OUT} = 0.1V$ or	1.5	2.0	2.0	V
	Input Voltage	5.5	V _{CC} – 0.1V	1.5	2.0	2.0	
V _{IL}	Maximum LOW	4.5	$V_{OUT} = 0.1V$ or	1.5	0.8	0.8	V
	Level Input Voltage	5.5	V _{CC} – 0.1V	1.5	0.8	0.8	
V _{OH}	Minimum HIGH Level	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
	Output Voltage	5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}$		3.86	3.76	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OH} = -24\text{mA}^{(4)}$		4.86	4.76	
V _{OL}	Maximum LOW	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
	Level Output Voltage	5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}$		0.36	0.44	
		5.5	$V_{IN} = V_{IL} \text{ or } V_{IH},$ $I_{OL} = 24\text{mA}^{(4)}$		0.36	0.44	
I _{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I _{CCT}	Maximum I _{CC} /Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic	5.5	$V_{OLD} = 1.65V Max.$			75	mA
I_{OHD}	Output Current ⁽⁵⁾	5.5	V _{OHD} = 3.85V Min.			-75	mA
I _{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA
I _{OZT}	Maximum I/O Leakage Current	5.5	$\begin{aligned} &V_{I}\left(OE\right)=V_{IL},V_{IH};\\ &V_{I}=V_{CC},GND;\\ &V_{O}=V_{CC},GND \end{aligned}$		±0.3	±3.0	μA

Notes:

- 4. All outputs loaded; thresholds on input associated with output under test.
- 5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

			T _A	T _A = +25°C, C _L = 50pF		$T_A = -40$ °C to +85°C, $C_L = 50$ pF		
Symbol	Parameter	$V_{CC}(V)^{(6)}$	Min.	Тур.	Max.	Min.	Max.	Units
t _{PLH}	Propagation Delay,	3.3	1.5	5.0	8.5	1.0	9.0	ns
	A_n to B_n or B_n to A_n	5.0	1.5	3.5	6.5	1.0	7.0	
t _{PHL}	Propagation Delay,	3.3	1.5	5.0	8.5	1.0	9.0	ns
	A_n to B_n or B_n to A_n	5.0	1.5	3.5	6.0	1.0	7.0	
t _{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
		5.0	1.5	5.0	8.5	1.0	9.0	
t _{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	2.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	9.5	
t _{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t _{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.5	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.0	

Note:

6. Voltage range 3.3 is 3.3V \pm 0.3V. Voltage range 5.0 is 5.0V \pm 0.5V.

AC Electrical Characteristics for ACT

				_ = +25° L = 50p			to +85°C, 50pF	
Symbol	Parameter	$V_{CC}(V)^{(7)}$	Min.	Тур.	Max.	Min.	Max.	Units
t _{PLH}	Propagation Delay, A _n to B _n or B _n to A _n	5.0	1.5	4.0	7.5	1.5	8.0	ns
t _{PHL}	Propagation Delay, A _n to B _n or B _n to A _n	5.0	1.5	4.0	8.0	1.0	9.0	ns
t _{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.5	11.0	ns
t _{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.5	12.0	ns
t _{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	11.0	ns
t _{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.5	11.0	ns

Note:

7. Voltage range 5.0 is $5.0V \pm 0.5V$.

Capacitance

	Symbol	Parameter	Conditions	Тур.	Units
	C _{IN}	Input Capacitance	V _{CC} = OPEN	4.5	pF
Ī	C _{I/O}	Input/Output Capacitance	V _{CC} = 5.0V	15.0	pF
Ī	C _{PD}	Power Dissipation Capacitance	V _{CC} = 5.0V	45.0	pF

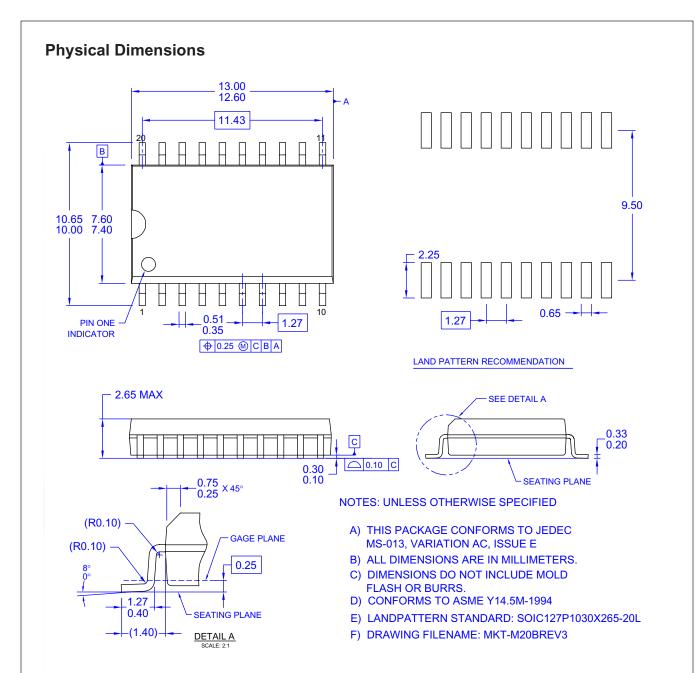
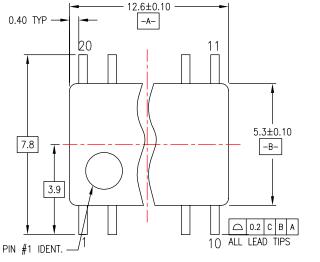
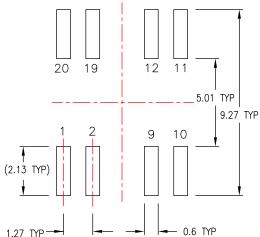


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

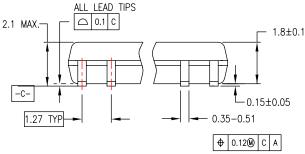
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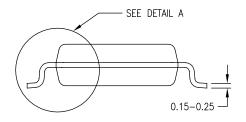
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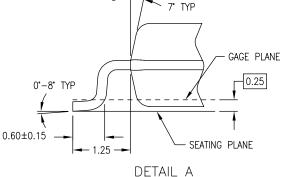




DIMENSIONS ARE IN MILLIMETERS

NOTES:

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 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



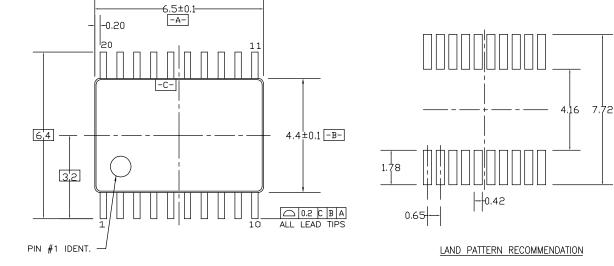
M20DREVC

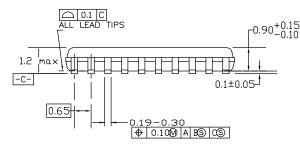
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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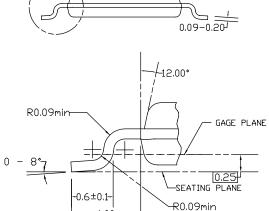






NOTES:

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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



SEE DETAIL A

DETAIL A

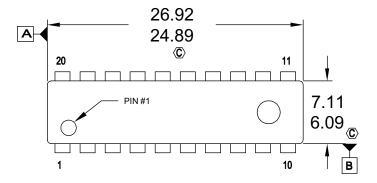
1.00

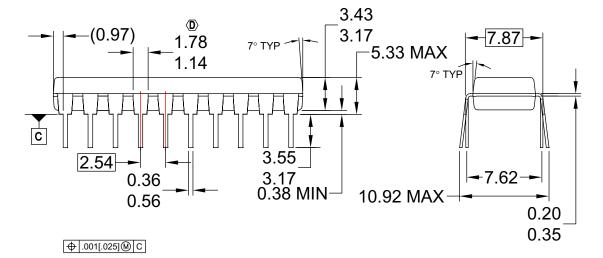
MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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NOTES:
A. CONFORMS TO JEDEC REGISTRATION MS-001,
VARIATIONS AD.

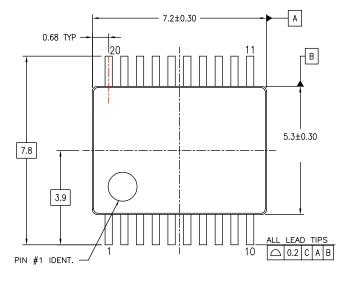
- **B. ALL DIMENSIONS ARE IN MILLIMETERS**
- © DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
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- 0.25MM.

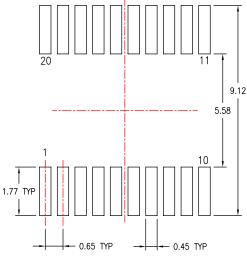
 D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

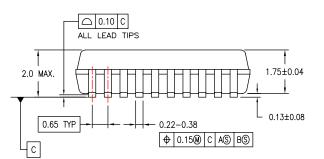
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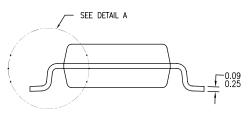
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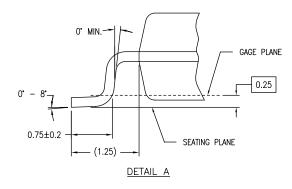




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- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M 1994.



MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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