November 2001 Revised November 2001

FAIRCHILD

SEMICONDUCTOR

74ALVC162244

Low Voltage 16-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistor in Outputs

General Description

The ALVC162244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/ receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74ALVC162244 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V. The 74ALVC162244 is also designed with 26 Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- \blacksquare 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in outputs

■ t_{PD}

- 3.8 ns max for 3.0V to 3.6V V_{CC} 4.3 ns max for 2.3V to 2.7V V_{CC} 7.6 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78ESD performance:
 - Human body model > 2000V Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74ALVC162244GX (Note 2)		54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74ALVC162244T (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: BGA package available in Tape and Reel only.

Note 3: Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

74ALVC162244



Connection Diagrams

Pin Assignment for TSSOP						
		48 — 0E ₂				
°° —	2	47 — I ₀				
0 ₁ —	3	46 — I ₁				
GND -	4	45 — GND				
0 ₂ —	5	44 — I ₂				
0 ₃ —	6	43 — I ₃				
v _{cc} –	7	42 — V _{CC}				
0 ₄ —	8	4 1 — I ₄				
°5 —	9	40 — I ₅				
GND —	10	39 — GND				
0 ₆ —	11	38 — 6				
°7 —	12	37 — I ₇				
°8 —	13	36 — I ₈				
0 ₉ —	14	35 — I ₉				
GND —	15	34 — GND				
0 ₁₀ —	16	33 — I ₁₀				
0 ₁₁	17	32 — I ₁₁				
v _{cc} —	18	31 — V _{CC}				
0 ₁₂	19	30 - I ₁₂				
0 ₁₃ —	20	29 — I ₁₃				
GND -	21	28 — GND				
0 ₁₄ —	22	27 — I ₁₄				
0 ₁₅	23	26 _ 1 <u>5</u>				
0E4 -	24	25 — OE ₃				
Pin As:	signment fo	or FBGA				

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(Top Thru View)

Pin Descriptions

Pin Names	Description
<u>OE</u> n	Output Enable Input (Active LOW)
I ₀ —I ₁₅	Inputs
O ₀ -O ₁₅	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
Α	O ₀	NC	OE ₁	\overline{OE}_2	NC	I ₀
В	O ₂	0 ₁	NC	NC	I ₁	l ₂
С	O ₄	O ₃	V _{CC}	V _{CC}	I ₃	I ₄
D	0 ₆	0 ₅	GND	GND	۱ ₅	I ₆
E	O ₈	0 ₇	GND	GND	1 ₇	l ₈
F	0 ₁₀	0 ₉	GND	GND	l ₉	I ₁₀
G	0 ₁₂	O ₁₁	V _{CC}	V _{CC}	I ₁₁	I ₁₂
Н	O ₁₄	O ₁₃	NC	NC	I ₁₃	I ₁₄
J	0 ₁₅	NC	\overline{OE}_4	OE ₃	NC	I ₁₅

Truth Tables

Inp	outs	Outputs
OE ₁	I ₀ –I ₃	O ₀ –O ₃
L	L	L
L	Н	н
Н	Х	Z
Inp	outs	Outputs
0E2	I ₄ —I ₇	04-07
L	L	L
L	Н	н
Н	Х	Z
Inp	outs	Outputs
OE ₃	I ₈ —I ₁₁	O ₈ –O ₁₁
L	L	L
L	Н	н
Н	Х	Z
Ing	outs	Outputs
OE ₄	I ₁₂ –I ₁₅	0 ₁₂ -0 ₁₅
L	L	L
L	н	н
н	Х	Z

L = HIGH Voltage Level L = LOW Voltage Level X = Immaterial (HIGH or LOW, inputs may not float) Z = High Impedance

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Functional Description

The 74ALVC162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation.The 3-STATE out-

Logic Diagram

puts are controlled by an Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.



Absolute Maximum Ratings(Note 4)

Supply Voltage (V _{CC})	-0.5V to +4.6V
DC Input Voltage (VI)	-0.5V to 4.6V
Output Voltage (V _O) (Note 5)	–0.5V to V _{CC} +0.5V
DC Input Diode Current (IIK)	
V ₁ < 0V	–50 mA
DC Output Diode Current (I _{OK})	
V _O < 0V	–50 mA
DC Output Source/Sink Current	
(I _{OH} /I _{OL})	±50 mA
DC V _{CC} or GND Current per	
Supply Pin (I _{CC} or GND)	±100 mA
Storage Temperature Range (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$

Recommended Operating

Conditions (Note 6)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V _{CC}
Output Voltage (V _O)	0V to V_{CC}
Free Air Operating Temperature (T _A)	$-40^{\circ}C$ to $+85^{\circ}C$
Minimum Input Edge Rate (Δt/ΔV)	
$V_{\text{IN}} = 0.8 \text{V}$ to 2.0V, $V_{\text{CC}} = 3.0 \text{V}$	10 ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
VIH	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V _{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
VIL	LOW Level Input Voltage		1.65 - 1.95		0.35 x V _{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	1.65 - 3.6	V _{CC} - 0.2		
		$I_{OH} = -2 \text{ mA}$	1.65	1.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.9		
		I _{OH} = -6 mA	2.3	1.7		V
			3	2.4		
		I _{OH} = -8 mA	2.7	2		
		I _{OH} = -12 mA	3.0	2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	1.65 - 3.6		0.2	
		I _{OL} = 2 mA	1.65		0.45	
		I _{OL} = 4 mA	2.3		0.4	
		I _{OL} = 6 mA	2.3		0.55	V
			3		0.55	
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3		0.8	
I _I	Input Leakage Current	$0 \le V_I \le 3.6V$	3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	3.6		±10	μA
I _{CC}	Quiescent Supply Current	$V_{I} = V_{CC}$ or GND, $I_{O} = 0$	3.6		40	μΑ
Δl _{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μΑ

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AC Electrical Characteristics

Symbol				T _A =	-40°C to +	$85^{\circ}C, R_{L} = 5$	500Ω			
	Parameter	C _L = 50 pF				C _L = 30 pF				Units
	Farameter	$V_{CC}=3.3V\pm0.3V$		$V_{CC} = 2.7V$		$V_{CC}=2.5V\pm0.2V$		$V_{CC}=1.8V\pm0.15V$		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay	1.3	3.8	1.5	4.3	1.0	3.8	1.5	7.6	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.3	1.5	5.6	1.0	5.1	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.1	1.5	4.5	1.0	4.0	1.5	7.2	ns

Capacitance

Symbol	Parameter		Conditions	TA = -	$T_A = +25^{\circ}C$	
	Faranieter			v _{cc}	Typical	Units
C _{IN}	Input Capacitance		$V_I = 0V \text{ or } V_{CC}$	3.3	6	pF
C _{OUT}	Output Capacitance		$V_I = 0V \text{ or } V_{CC}$	3.3	7	pF
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF	3.3	20	pF
				2.5	20	рг

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