Low-Voltage 1.8/2.5/3.3V 16-Bit Transceiver

With 3.6 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The 74ALVC16245 is an advanced performance, non-inverting 16-bit transceiver. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

The ALVC16245 is designed with byte control. It can be operated as two separate octals, or with the controls tied together, as a 16-bit wide function. The Transmit/Receive ($T/\overline{R}n$) inputs determine the direction of data flow through the bi-directional transceiver. Transmit (active–HIGH) enables data from A ports to B ports; Receive (active–LOW) enables data from B to A ports. The Output Enable inputs (\overline{OEn}), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

- Designed for Low Voltage Operation: $V_{CC} = 1.65-3.6 \text{ V}$
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.0 ns max for 3.0 to 3.6 V

3.7 ns max for 2.3 to 2.7 V 6.0 ns max for 1.65 to 1.95 V

• Static Drive: ± 24 mA Drive at 3.0 V

 \pm 12 mA Drive at 2.3 V \pm 4 mA Drive at 1.65 V

- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0 V^{\dagger}$
- Near Zero Static Supply Current in All Three Logic States (40 μA)
 Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- Second Source to Industry Standard 74ALVC16245

†To ensure the outputs activate in the 3-state condition, the output enable pins should be connected to $V_{\rm CC}$ through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the $\overline{\rm OE}$ pin.



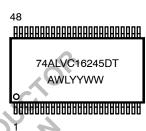
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TSSOP-48 DT SUFFIX CASE 1201



A = Assembly

Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping		
74ALVC16245DTR	TSSOP	2500/Tape & Reel		

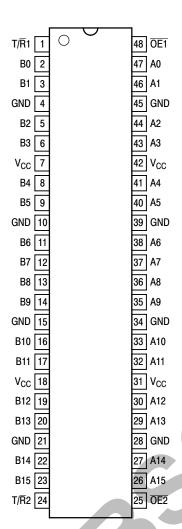


Figure 1. 48-Lead Pinout (Top View)

PIN NAMES

Pins	Function
ŌEn T/Rn A0−A15 B0−B15	Output Enable Inputs Transmit/Receive Inputs Side A Inputs or 3-State Outputs Side B Inputs or 3-State Outputs

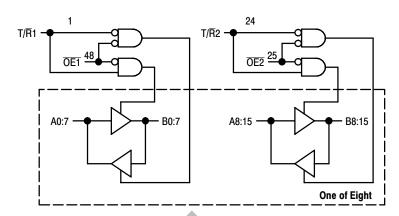


Figure 2. Logic Diagram

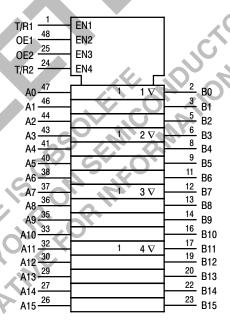


Figure 3. IEC Logic Diagram

Inp	uts	Outputs	Inputs		Outputs
OE1	T/R1	Outputs	OE2	T/R2	Outputs
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	Н	Bus A0:7 Data to Bus B0:7	L	Н	Bus A8:15 Data to Bus B8:15
Н	Х	High Z State on A0:7, B0:7	Н	Х	High Z State on A8:15, B8:15

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +4.6	V
VI	DC Input Voltage	-0.5 to +4.6	V
Vo	DC Output Voltage	-0.5 to +4.6	V
I _{IK}	DC Input Diode Current $V_{l} < GND$	-50	mA
lok	DC Output Diode Current V _O < GND	-50	mA
I _O	DC Output Sink/Source Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+ 150	°C
θ_{JA}	Thermal Resistance (Note 2)	90	°C/W
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	٧
I _{LATCH-UP}	Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 6)	± 250	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Io absolute maximum rating must be observed.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.

3. Tested to EIA/JESD22-A114-A.

4. Tested to EIA/JESD22-A115-A.

5. Tested to JESD22-C101-A.

6. Tested to EIA/JESD78.

Symbol	Parameter	Min	Тур	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
VI	Input Voltage (Note 7)	-0.5		3.6	V
V _O	Output Voltage (Active State) (3-State)	0 0		V _{CC} 3.6	V
T _A	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V,V _{CC} = 2.5 V \pm 0.2 V V _{CC} = 3.0 V \pm 0.3 V	0 0		20 10	ns/V

^{7.} Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

			T _A = -40°0	C to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage (Note 8)	1.65 V ≤ V _{CC} < 2.3 V	0.65 x V _{CC}		V
		2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		
		2.7 V < V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 8)	1.65 V ≤ V _{CC} < 2.3 V		0.35 x V _{CC}	V
		2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	
		2.7 V < V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{ I}_{OH} = -100 \mu\text{A}$	V _{CC} - 0.2		V
		V _{CC} = 1.65 V; I _{OH} = -4 mA	1.2		
		V _{CC} = 2.3 V; I _{OH} = -6 mA	2.0		
		$V_{CC} = 2.3 \text{ V}; I_{OH} = -12 \text{ mA}$	1.7		
		$V_{CC} = 2.7 \text{ V}; I_{OH} = -12 \text{ mA}$	2.2	0	
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -12 \text{ mA}$	2.4	.0	
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -24 \text{ mA}$	2.0		
V _{OL}	LOW Level Output Voltage	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$	110	0.2	V
		V _{CC} = 1.65 V; I _{OL} = 4 mA	.0	0.45	
		V _{CC} = 2.3 V; I _{OL} = 6 mA	16.11	0.4	
		V _{CC} = 2.3 V; I _{OL} = 12 mA		0.7	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA	0.1.	0.55	
l _l	Input Leakage Current	$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_1 \le 3.6 \text{ V}$) *	±5.0	μΑ
l _{OZ}	3-State Output Current	1.65 V \leq V _{CC} \leq 3.6 V; 0 V \leq V _O \leq 3.6 V; V _I = V _{IH} or V _{IL}		±10	μΑ
I _{OFF}	Power-Off Leakage Current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 3.6 \text{ V}$		10	μΑ
I _{CC}	Quiescent Supply Current (Note 9)	1.65 V ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		40	μΑ
		$1.65 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 3.6 \text{ V} \le \text{V}_{I}, \text{V}_{O} \le 3.6 \text{ V}$		±40	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$2.7 \text{ V} < \text{V}_{CC} \le 3.6 \text{ V}; \text{V}_{IH} = \text{V}_{CC} - 0.6 \text{ V}$		750	μΑ

^{8.} These values of V_I are used to test DC electrical characteristics only.
9. Outputs disabled or 3-state only.

AC CHARACTERISTICS (Note 10; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500 \Omega$)

		~O,			Lim	nits			
					$T_A = -40^{\circ}C$	C to +85°C			
	C	V 064	V _{CC} = 3.0	V to 3.6 V	V _{CC} = 2.3	V to 2.7 V	V _{CC} = 1.6	5 to1.95 V	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t _{PLH} t _{PHL}	Propagation Delay Input to Output	1	1.0 1.0	3.0 3.0	1.0 1.0	3.7 3.7	1.0 1.0	6.0 6.0	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	1.0 1.0	4.4 4.4	1.0 1.0	5.7 5.7	1.0 1.0	9.3 9.3	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.0 1.0	4.1 4.1	1.0 1.0	5.2 5.2	1.0 1.0	7.6 7.6	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 11)			0.5 0.5		0.5 0.5		0.75 0.75	ns

^{10.} For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

 ^{11.} Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	Note 12	6	pF
C _{OUT}	Output Capacitance	Note 12	7	pF
C _{PD}	Power Dissipation Capacitance	Note 12, 10 MHz	20	pF

12. V_{CC} = 1.8, 2.5 or 3.3 V; V_{I} = 0 V or V_{CC} .

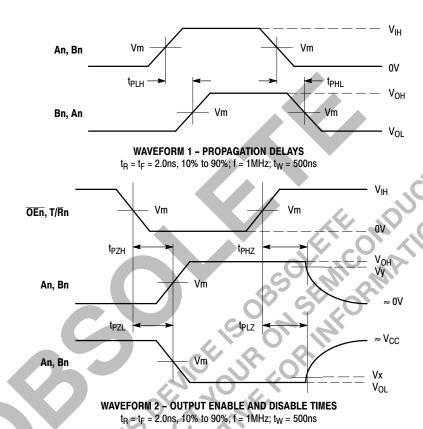
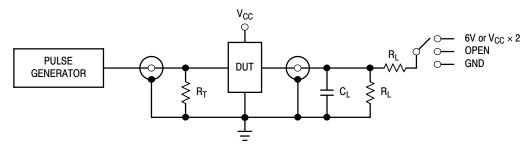


Figure 4. AC Waveforms

) (()	V _{CC}	
Symbol	3.3 V ±0.3 V	2.5 V ±0.2 V	1.8 V ±0.15 V
V _{IH}	2.7 V	V _{CC}	V _{CC}
V _m	1.5 V	V _{CC} /2	V _{CC} /2
V _x	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
V _y	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V



$\begin{array}{c c} t_{PLH}, t_{PHL} & Open \\ \hline t_{PZL}, t_{PLZ} & 6 \ V \ at \ V_{CC} = 3.3 \pm 0.3 \ V; \\ V_{CC} \times 2 \ at \ V_{CC} = 2.5 \pm 0.2 \ V; \ 1.8 \ V \pm 0.15 \ V \\ \hline t_{PZH}, t_{PHZ} & GND \\ \hline \\ C_L = 30 \ pF \ or \ equivalent \ (Includes \ jig \ and \ probe \ capacitance) \\ R_L = 500 \ \Omega \ or \ equivalent \\ R_T = Z_{OUT} \ of \ pulse \ generator \ (typically 50 \ \Omega) \\ \hline \\ \textbf{Figure 5. Test Circuit} \\ \hline \end{array}$	TEST	SWITCH
		Open
C _L = 30 pF or equivalent (Includes jig and probe capacitance) R _L = 500 Ω or equivalent R _T = Z _{OUT} of pulse generator (typically 50 Ω) Figure 5. Test Circuit	V _C	
C _L = 30 pF or equivalent (Includes jig and probe capacitance) R _L = 500 Ω or equivalent R _T = Z _{OUT} of pulse generator (typically 50 Ω) Figure 5. Test Circuit		GND
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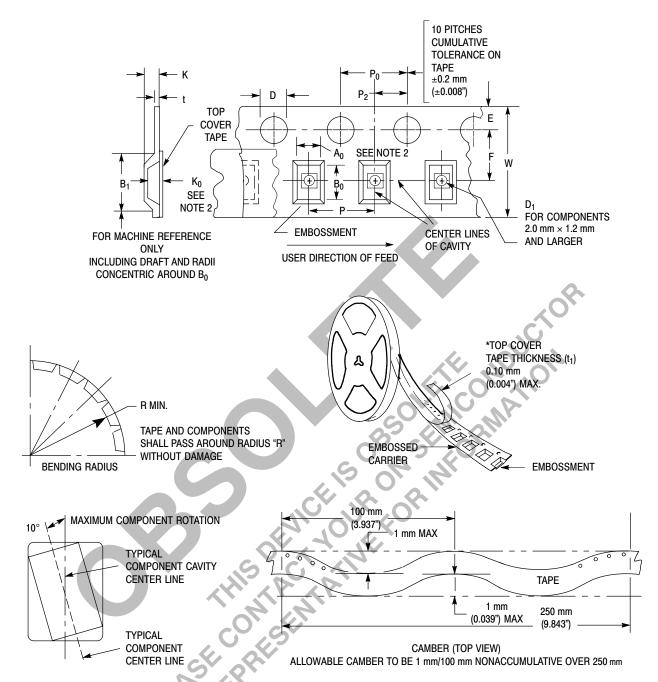


Figure 6. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B ₁ Max	D	D ₁	E	F	к	Р	Po	P ₂	R	Т	w
24mm	20.1mm (0.791")	1.5 + 0.1mm -0.0 (0.059 +0.004" -0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

^{1.} Metric Dimensions Govern-English are in parentheses for reference only.

^{2.} A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

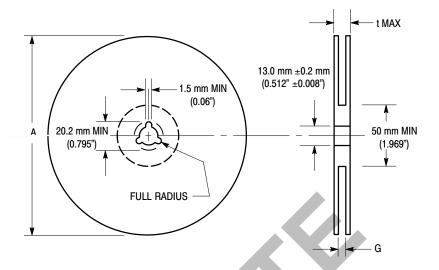


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm	24.4 mm + 2.0 mm, -0.0	30.4 mm
	(14.173")	(0.961" + 0.078", -0.00)	(1.197")

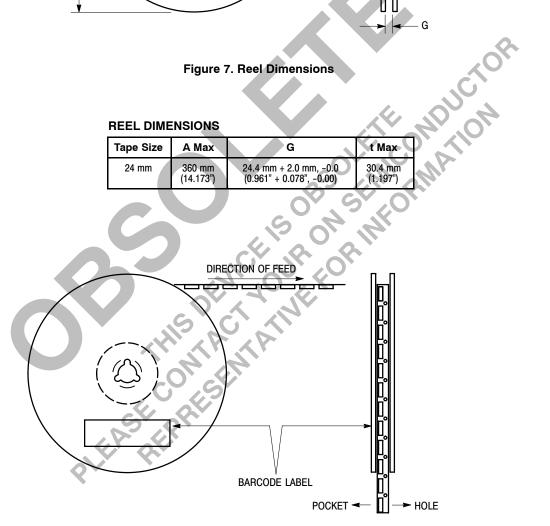


Figure 8. Reel Winding Direction

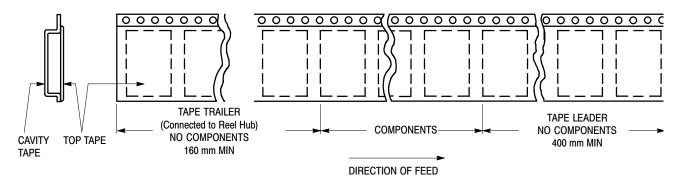


Figure 9. Tape Ends for Finished Goods

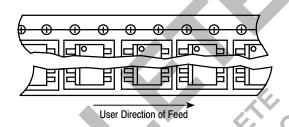


Figure 10. Reel Configuration

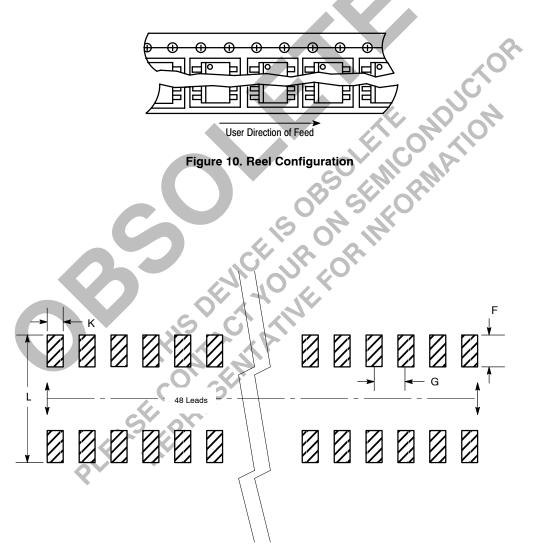
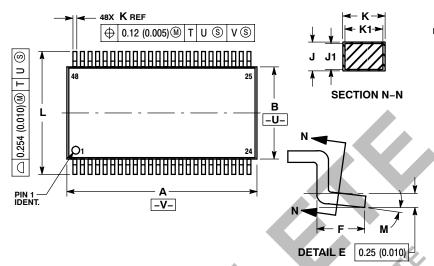


Figure 11. Package Footprint

PACKAGE DIMENSIONS

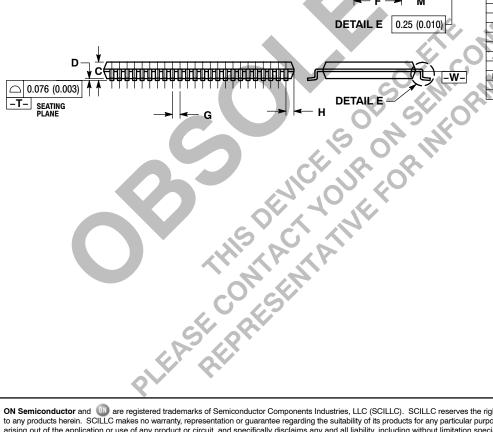
TSSOP DT SUFFIX CASE 1201-01 ISSUE A



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
 B. DIMENSIONS A AND B DO NOT INCLUDE
- DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
- DIMENSION K DUES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 DIMENSIONS A AND B ARE TO BE
- DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	12.40	12.60	0.488	0.496
В	6.00	6.20	0.236	0.244
С	4	1.10		0.043
D	0.05	0.15	0.002	0.006
E	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
Н	0.37	i	0.015	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8°	0 °	8°



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