

August 1998 Revised June 2005

74LCXR162245

Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs/Outputs and 26 Ω Series Resistors in the Outputs

General Description

The LCXR162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) $V_{\rm CC}$ applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/\overline{R} inputs determine the direction of data flow through the device. The $\overline{\rm OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

In addition, all A and B outputs include equivalent 26Ω (nominal) series resistors to reduce overshoot and undershoot and are designed to sink/source up to 12 mA at $V_{CC}=3.0V.$

The LCXR162245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V-3.6V V_{CC} specifications provided
- \blacksquare A and B side outputs have equivalent 26 $\!\Omega$ series resistors
- 5.3 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μ A I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Flow through pinout
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:

Human body model > 2000V

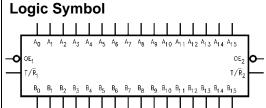
Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down $\overline{\text{OE}}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCXR162245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LCXR162245MEX		48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LCXR162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LCXR162245MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Devices also available in Tape and Reel. Specify by appending the suffix letter "x" to the ordering code.



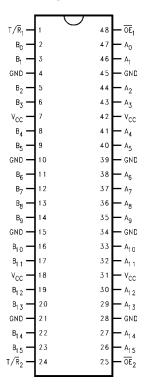
Pin Descriptions

	Pin Names	Description
_	OE _n	Output Enable Input
-		Transmit/Receive Input
	A ₀ -A ₁₅	Side A Inputs or 3-STATE Outputs
	B ₀ -B ₁₅	Side B Inputs or 3-STATE Outputs

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DS500052

Connection Diagram



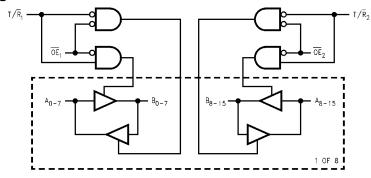
Truth Tables

Inputs		Outputs
\overline{OE}_1 T/\overline{R}_1		
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	Н	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H X HIGH Z State on A ₀ -A ₇ , B ₀ -		HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇ (Note 2)

Inputs		Outputs
OE₂ T/R₂		
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	Н	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
н х		HIGH Z State on A ₈ –A ₁₅ , B ₈ –B ₁₅ (Note 2)

Note 2: A and B port inputs are still active

Logic Diagram



Absolute Maximum Ratings(Note 3) Parameter Units Symbol Value Conditions ٧ -0.5 to +7.0 Supply Voltage V_{CC} ٧ DC Input Voltage -0.5 to +7.0 V_{I} DC Output Voltage Output in 3-STATE Vo -0.5 to +7.0 ٧ Output in HIGH or LOW State (Note 4) -0.5 to $V_{CC} + 0.5$ DC Input Diode Current -50 $V_I < GND$ mΑ I_{IK} V_O < GND DC Output Diode Current -50 I_{OK} mΑ +50 $V_O > V_{CC}$ DC Output Source/Sink Current ±50 mΑ I_{O} I_{CC} DC Supply Current per Supply Pin ±100 mΑ DC Ground Current per Ground Pin I_{GND} ±100 mΑ Storage Temperature -65 to +150

Recommended Operating Conditions (Note 5)

Symbol	Parameter			Max	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	V
VI	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	V
I _{OH} /I _{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		±12	
		$V_{CC} = 2.7V - 3.0V$		±8	mA
		$V_{CC} = 2.3V - 2.7V$		±4	
T _A	Free-Air Operating Temperature		-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: IO Absolute Maximum Rating must be observed.

 $\mathsf{T}_{\mathsf{STG}}$

Note 5: Unused pins (Inputs or I/O's) must be held HIGH or LOW. They may not Float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{cc}	T _A = -40°C	to +85°C	Units
Symbol	Farameter	Conditions	(V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 - 3.6	2.0		1 °
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 - 3.6		0.8	1 °
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2		
		$I_{OH} = -4 \text{ mA}$	2.3	1.8		l
		$I_{OH} = -4 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -6 \text{ mA}$	3.0	2.4		1 '
		$I_{OH} = -8 \text{ mA}$	2.7	2.0		l
		$I_{OH} = -12 \text{ mA}$	3.0	2.0		l
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	
		$I_{OL} = 4 \text{ mA}$	2.3		0.6	l
		$I_{OL} = 4 \text{ mA}$	2.7		0.4	v
		$I_{OL} = 6 \text{ mA}$	3.0		0.55	1 °
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3.0		0.8	1
lı .	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		±5.0	μА
oz	3-STATE I/O Leakage	$0 \le V_O \le 5.5V$	2.3 - 3.6		±5.0	
		$V_I = V_{IH}$ or V_{IL}				μА

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	v _{cc}	T _A = -40°	C to +85°C	Units
Cyllibol	r arameter	Conditions	(V)	Min	Max	Oilles
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μА
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	цА
		$3.6V \le V_I$, $V_O \le 5.5V$ (Note 6)	2.3 - 3.6		±20	μΛ
Δl _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} -0.6V	2.3 - 3.6		500	μА

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

		$T_A = -40$ °C to $+85$ °C, $R_L = 500 \Omega$						
Symbol	Parameter	V _{CC} = 3.	BV ± 0.3V V _{CC}	V _{CC}	= 2.7V	V _{CC} = 2	.5V ± 0.2	Units
Syllibol	Farameter	C _L =	50 pF	C _L =	50 pF	C _L =	30 pF	Units
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.3	1.5	6.0	1.5	6.4	
t _{PLH}	A _n to B _n or B _n to A _n	1.5	5.3	1.5	6.0	1.5	6.4	ns
t _{PZL}	Output Enable Time	1.5	7.3	1.5	8.0	1.5	9.5	no
t_{PZH}		1.5	7.3	1.5	8.0	1.5	9.5	ns
t _{PLZ}	Output Disable Time	1.5	6.4	1.5	6.9	1.5	7.7	ns
t_{PHZ}		1.5	6.4	1.5	6.9	1.5	7.7	115
toshl	Output to Output Skew (Note 7)		1.0					ns
t _{OSLH}			1.0					115

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{cc}	T _A = 25°C	Units
Oyillboi	T arameter	Conditions	(V)	Typical	Oille
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.35	V
		$C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{IL} = 0 \text{V}$	2.5	0.25	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.35	V
		$C_{I} = 30 \text{ pF}, V_{IH} = 2.5 \text{V}, V_{II} = 0 \text{V}$	2.5	-0.25	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_{I} = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}$	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

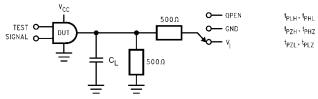
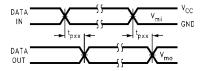
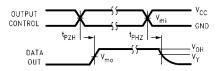


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

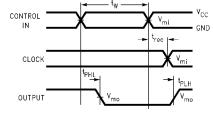
Test	Switch
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t _{PZH} ,t _{PHZ}	GND



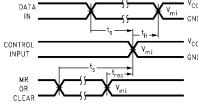
Waveform for Inverting and Non-Inverting Functions



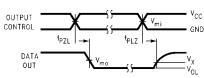
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay. Pulse Width and \mathbf{t}_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

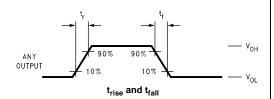
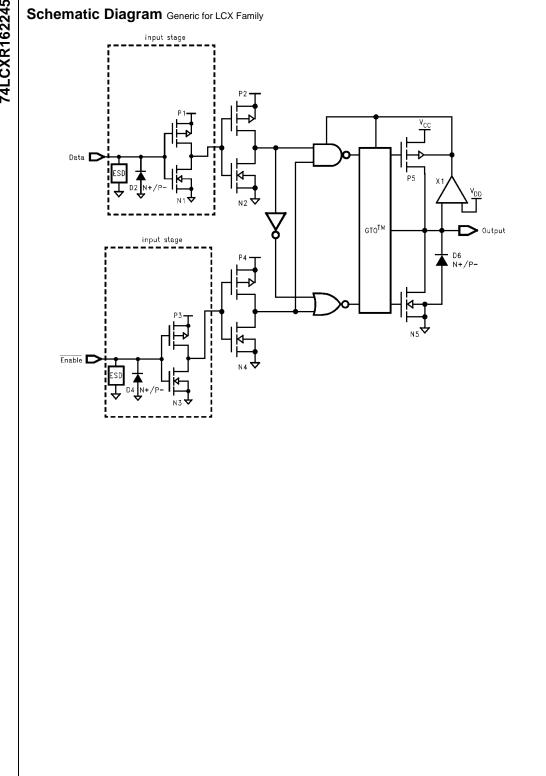
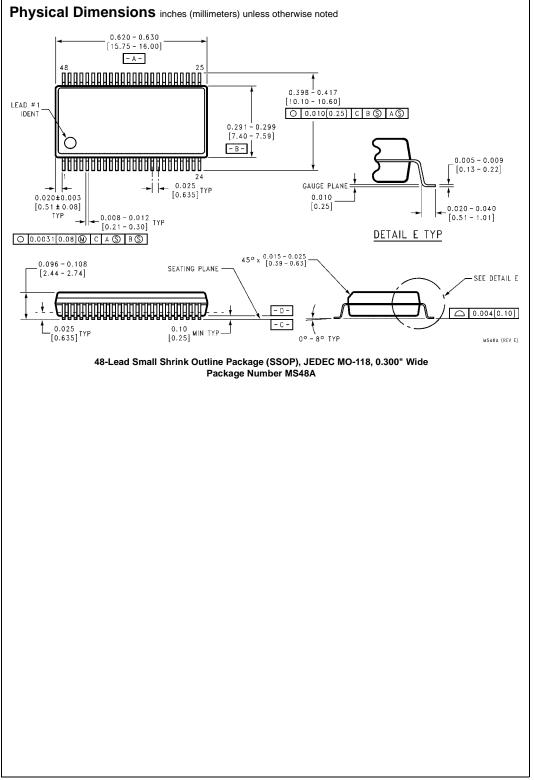


FIGURE 2. Waveforms (Input Characteristics; f = 1MHz, $t_R = t_F = 3ns$)

Symbol		V _{CC}	
Cymbol	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V _{CC} /2
V_{mo}	1.5V	1.5V	V _{CC} /2
V _x	V _{OL} + 0.3V	V _{OL} + 0.3V	V _{OL} + 0.15V
V _v	V _{OH} – 0.3V	$V_{OH} - 0.3V$	V _{OH} – 0.15V





Resistors in the Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 12.50±0.10 0.40 TYP -B-99. 9.20 8.10 50. O.2 C B A ALL LEAD TIPS PIN #1 IDENT 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.17-0.27 0.50 ♦ 0.13@ A BS CS 12.00' TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS R0.16 GAGE PLANE 0.25 NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 1.00 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. DETAIL A MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

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