National Semiconductor

# 74LVQ125
# Low Voltage Quad Buffer with TRI-STATE® Outputs

## General Description

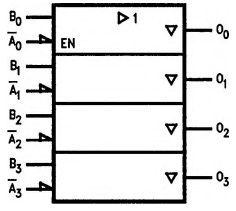
The LVQ125 contains four independent non-inverting buffers with TRI-STATE outputs.

## Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/Aerospace applications

## Ordering Code: See Section 11

## Logic Symbol

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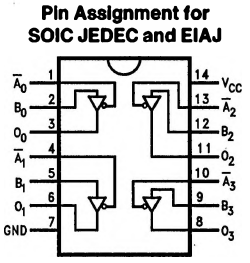
## Connection Diagram

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| Pin Names | Description |
|---|---|
| $\overline{A}_n$, $B_n$ | Inputs |
| $O_n$ | Outputs |

## Truth Table

| Inputs | | Output |
|---|---|---|
| $A_n$ | $B_n$ | $O_n$ |
| L | L | L |
| L | H | H |
| H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

| | SOIC JEDEC | SOIC EIAJ |
|---|---|---|
| Order Number | 74LVQ125SC<br>74LVQ125SCX | 74LVQ125SJ<br>74LVQ125SJX |
| See NS Package Number | M14A | M14D |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current ($I_{CC}$ or $I_{GND}$) | ±200 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or Sink Current | ±100 mA |

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteritics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| LVQ | 2.0V to 3.6V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 74LVQ | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 3.0V | 125 mV/ns |

## DC Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ125 $T_A$ = +25°C | | 74LVQ125 $T_A$ = −40°C to +85°C | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −50 μA |
| | | 3.0 | | 2.58 | 2.48 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OH}$ = −12 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0 | | 0.36 | 0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OL}$ = 12 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 3.6 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OZ}$ | Maximum TRI-STATE Leakage Current | 3.6 | | ±0.25 | ±2.5 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$ $V_I$ = $V_{CC}$, GND $V_O$ = $V_{CC}$, GND |

*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ125 $T_A = +25°C$ | | 74LVQ125 $T_A = -40°C$ to $+85°C$ | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 3.6 | | | 36 | mA | $V_{OLD}$ = 0.8V Min (Note 1) |
| $I_{OHD}$ | | 3.6 | | | −25 | mA | $V_{OHD}$ = 2.0V Min (Note 1) |
| $I_{CC}$ | Maximum Quiescent Supply Current | 3.6 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 0.6 | 1.0 | | V | (Notes 2 and 3) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | −0.6 | −1.0 | | V | (Notes 2 and 3) |
| $V_{IHD}$ | Maximum High Level Dynamic Input Voltage | 3.3 | 1.7 | 2.0 | | V | (Notes 2 and 4) |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | 3.3 | 1.5 | 0.8 | | V | (Notes 2 and 4) |

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 4:** Max number of Data Inputs (n) switching. (n − 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics: See Section 2 for Test Methodology

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ125 $T_A = +25°C$, $C_L = 50$ pF | | | 74LVQ125 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Data to Output | 2.7 | 1.0 | 7.8 | 12.7 | 1.0 | 14.0 | ns |
| | | 3.3 ±0.3 | 1.0 | 6.5 | 9.0 | 1.0 | 10.0 | |
| $t_{PHL}$ | Propagation Delay Data to Output | 2.7 | 1.0 | 7.8 | 12.7 | 1.0 | 14.0 | ns |
| | | 3.3 ±0.3 | 1.0 | 6.5 | 9.0 | 1.0 | 10.0 | |
| $t_{PZH}$ | Output Enable Time | 2.7 | 1.0 | 7.2 | 14.8 | 1.0 | 16.0 | ns |
| | | 3.3 ±0.3 | 1.0 | 6.0 | 10.5 | 1.0 | 11.0 | |
| $t_{PZL}$ | Output Enable Time | 2.7 | 1.0 | 9.0 | 14.0 | 1.0 | 16.0 | ns |
| | | 3.3 ±0.3 | 1.0 | 7.5 | 10.0 | 1.0 | 11.0 | |
| $t_{PHZ}$ | Output Disable Time | 2.7 | 1.0 | 9.0 | 14.0 | 1.0 | 15.0 | ns |
| | | 3.3 ±0.3 | 1.0 | 7.5 | 10.0 | 1.0 | 10.5 | |
| $t_{PLZ}$ | Output Disable Time | 2.7 | 1.0 | 9.0 | 14.8 | 1.0 | 16.5 | ns |
| | | 3.3 ±0.3 | 1.0 | 7.5 | 10.5 | 1.0 | 11.5 | |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew* Data to Output | 2.7 | | 1.0 | 1.5 | | 1.5 | ns |
| | | 3.3 ±0.3 | | 1.0 | 1.5 | | 1.5 | |

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ($t_{OSHL}$) or LOW to HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = Open |
| $C_{PD}$ (Note 1) | Power Dissipation Capacitance | 34 | pF | $V_{CC}$ = 3.3V |

**Note 1:** $C_{PD}$ is measured at 10 MHz.