National Semiconductor

ADVANCE INFORMATION

74LVT245
3.3V ABT Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

The LVT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

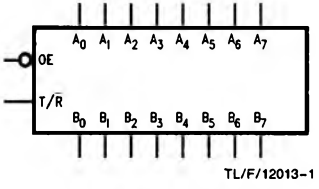
These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA

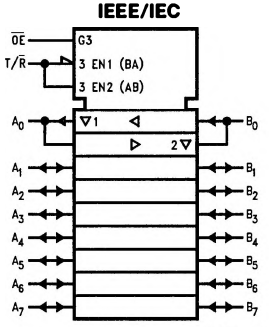
Ordering Code: See Section 11

Logic Symbols



TL/F/12013–1

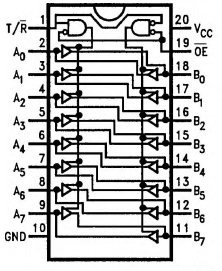
IEEE/IEC



TL/F/12013–2

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12013–3

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT245WM 74LVT245WMX	74LVT245SJ 74LVT245SJX	74LVT245MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
Output Voltage (V_O)	
Outputs in TRI-STATE	−0.5V to +7.0V
Outputs Active	−0.5V to V_{CC}
DC Output Current (I_O)	
Output in LOW State	128 mA
Output in HIGH State, $V_O > V_{CC}$	64 mA
DC Input Diode Current (I_{IK}) $V_I < 0$	−50 mA
DC Output Diode Current (I_{OK}) $V_O < 0$	−50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage	
Operating	2.7V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0V to V_{CC}
Output in "OFF" State	0V to 5.5V
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	10 ns/V
Free Air Operating Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 1)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage	2.7–3.6			0.8	V	
V_{OH}	Output HIGH Voltage	2.7–3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100\ \mu A$
		2.7	2.4			V	$I_{OH} = -8$ mA
		3.0	2.0			V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	$I_{OL} = 100\ \mu A$
		2.7			0.5	V	$I_{OL} = 24$ mA
		3.0			0.4	V	$I_{OL} = 16$ mA
		3.0			0.5	V	$I_{OL} = 32$ mA
		3.0			0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$	Bus-Held Input Minimum Drive	3.0	75			μA	$V_I = 0.8V$
			−75			μA	$V_I = 2.0V$
$I_{I(OD)}$	Bus-Held Input Over-Drive Current to Change State	3.0	500			μA	(Note 2)
			−500			μA	(Note 3)
I_I	Input Current	0 or 3.6			10	μA	$V_I = 5.5V$
	Control Pins	3.6			±1	μA	$V_I = 0V$ or V_{CC}
	Data Pins	3.6			−5	μA	$V_I = 0V$
					1	μA	$V_I = V_{CC}$
I_{IH}^+	Control Pin Input Current	3.6			10	μA	$V_{CC} \le V_I \le 5.5V$
I_{OFF}	Input or Output Current	0			±100	μA	$0V \le (V_I$ or $V_O) \le 5.5V$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 1)	Max		
I_{OZL}	TRI-STATE Output Leakage Current	3.6			−1	μA	V_O = 0V
I_{OZH}	TRI-STATE Output Leakage Current	3.6			1	μA	$V_O = V_{CC}$
$I_{OZH}+$	TRI-STATE Output Leakage Current	3.6			10	μA	$V_{CC} \le V_O \le 5.5V$
I_{CCH}	Power Supply Current	3.6			0.19	mA	V_I = GND or V_{CC}, Outputs High
I_{CCL}	Power Supply Current	3.6			12	mA	V_I = GND or V_{CC}, Outputs Low
I_{CCZ}	Power Supply Current	3.6			0.19	mA	V_I = GND or V_{CC}, Outputs Disabled
$I_{CCZH}+$	Power Supply Current	3.6			0.19	mA	V_I = GND or V_{CC}, $V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 4)	3.6			0.2	mA	One Input at V_{CC} − 0.6V Other Inputs at V_{CC} or GND

Note 1: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 2: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 3: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 4: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics : See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			Units	Conditions C_L = 50 pF, R_L = 500Ω
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 2)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 2)
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3				V	(Note 3)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3				V	(Note 3)

Note 1: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 2: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output at LOW.

Note 3: Max number of data inputs (n) switching. n−1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}).

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, C_L = 50 pF, R_L = 500Ω					Units
		V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
		Min	Typ (Note 1)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.0		4.0	1.0	4.7	ns
t_{PHL}		1.0		4.0	1.0	4.6	
t_{PZH}	Output Enable Time	1.1		5.5	1.1	7.1	ns
t_{PZL}		1.5		5.5	1.5	6.5	
t_{PHZ}	Output Disable Time	2.2		5.9	2.2	6.5	ns
t_{PLZ}		2.0		4.8	2.0	4.8	
t_{OSHL}	Output to Output Skew			1.0			ns
t_{OSLH}	(Note 2)						

Note 1: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance (Note 1)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		4		pF	V_{CC} = 0V, V_I = 0V or V_{CC}
$C_{I/O}$	I/O Capacitance		8		pF	V_{CC} = 3V, $V_{I/O}$ = 0V or V_{CC}

Note 1: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.