National Semiconductor

74LVX374
Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

General Description

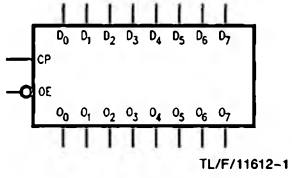
The LVX374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEOEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbols



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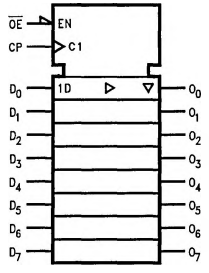
IEEE/IEC



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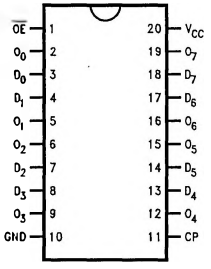
Connection Diagram

Pin Assignment for SOIC and SSOP



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX374M 74LVX374MX	74LVX374SJ 74LVX374SJX	74LVX374MSCX
See NS Package Number	M20B	M20D	MSC20

Functional Description

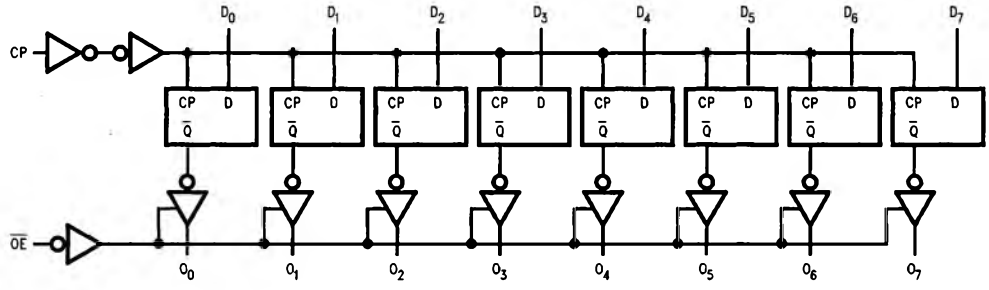
The LVX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
DC Input Voltage (V_I)	−0.5V to 7V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±25 mA
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Power Dissipation	180 mW

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_o)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	74LVX374 T_A = +25°C			74LVX374 T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
V_{IL}	Low Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				I_{OH} = −50 μA
		3.0	2.58			2.48				I_{OH} = −4 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			I_{OL} = 50 μA
		3.0			0.36		0.44			I_{OL} = 4 mA
I_{OZ}	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	3.6			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	3.6			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX374 $T_A = 25°C$ Typ	74LVX374 $T_A = 25°C$ Limit	Units	C_L (pF)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.5	0.8	V	50
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	−0.5	−0.8	V	50
V_{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	74LVX374 $T_A = +25°C$ Min	Typ	Max	74LVX374 $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay Time CP to O_n	2.7		8.5	16.3	1.0	19.5	ns	$C_L = 15$ pF
				11.0	19.8	1.0	23.0		$C_L = 50$ pF
		3.3 ±0.3		6.7	10.6	1.0	12.5		$C_L = 15$ pF
				9.2	14.1	1.0	16.0		$C_L = 50$ pF
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	2.7		7.6	14.5	1.0	17.5	ns	$C_L = 15$ pF, $R_L = 1$ kΩ
				10.1	18.0	1.0	21.0		$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		5.9	9.3	1.0	11.0		$C_L = 15$ pF, $R_L = 1$ kΩ
				8.4	12.8	1.0	14.5		$C_L = 50$ pF, $R_L = 1$ kΩ
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	2.7		11.5	18.5	1.0	22.0	ns	$C_L = 50$ pF, $R_L = 1$ kΩ
		3.3 ±0.3		9.6	13.2	1.0	15.0		$C_L = 50$ pF, $R_L = 1$ kΩ
t_W	CP Pulse Width	2.7	7.5			8.0		ns	
		3.3 ±0.3	5.0			5.5			
t_S	Setup Time D_n to CP	2.7	6.5			6.5		ns	
		3.3 ±0.3	4.5			4.5			
t_H	Hold Time D_n to CP	2.7	2.0			2.0		ns	
		3.3 ±0.3	2.0			2.0			
f_{MAX}	Maximum Clock Frequency	2.7	60	115		50		MHz	$C_L = 15$ pF
			45	60		40			$C_L = 50$ pF
		3.3 ±0.3	100	160		85			$C_L = 15$ pF
			60	95		55			$C_L = 50$ pF
t_{OSLH} t_{OSHL}	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	$C_L = 50$ pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	74LVX374 $T_A = +25°C$ Min	Typ	Max	74LVX374 $T_A = -40°C$ to $+85°C$ Min	Max	Units
C_{IN}	Input Capacitance		4	10		10	pF
C_{OUT}	Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 1)		32				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$