signetics

1024 BIT FIELD/FACTORY PROGRAMMABLE BIPOLAR ROM (256x4)

8226
8229

REFER TO PAGE 13 FOR E PACKAGE PIN CONFIGURATION.

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The 8226 (open Collector Outputs) and the 8229 (tri State Outputs) are Bipolar 1024 Bit Read Only Memories organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. Two chip enable lines are provided and the outputs are bare collector to allow for memory expansion capability.

The 8226 and 8229 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35ns.

The standard 8226 and 8229 are supplied with all outputs at a logical "1". If a programmed unit is required the Truth Table/Order Blank on page 200 can be used.

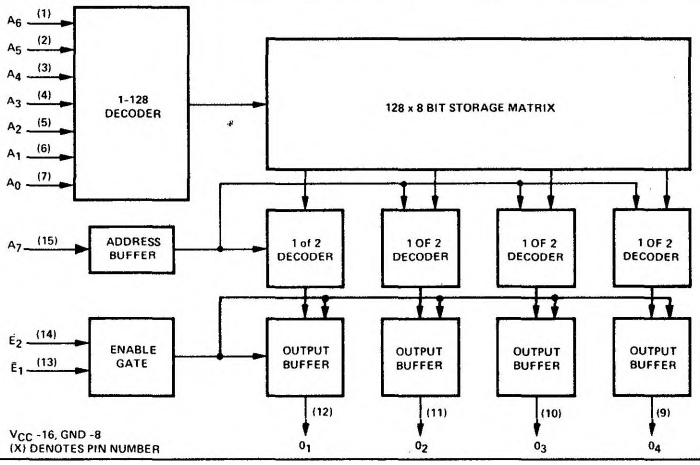
FEATURES

- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- TWO CHIP ENABLE LINES
- OPEN COLLECTOR OR TRI STATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage			0.5	V	I_{out} = 16 mA	
"1" Output Leakage			40	μA	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{OUT} = 2.6V	
8226			100	μA	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", V_{OUT} = 2.6V	
8229	-40		+40	μA	V_{out} = 0.5V, $\overline{CE}_1$, or $\overline{CE}_2$ = "1"	
"1" Output Current(8229)	-2.0			mA	V_{out} = 2.4V, $\overline{CE}_1$ = $\overline{CE}_2$ = "0"	
"0" Input Current			250	μA	V_{in} = 0.5V	
"1" Input Current			50	μA	V_{in} = 2.7V	
Input Threshold Voltage						
"0" Level	.85			V		
"1" Level			2.0	V		
Propagation Delay						
Address to Output			60	ns		
Enable to Output			50	ns		

T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Input Clamp Voltage	-1.0			V	I_{in} = 5.0 mA	
Power Consumption		130/650		mA/mW	V_{CC} = 5.00V	

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.
3. Applied voltage must not exceed 6.0V
   Input currents must not exceed ±30mA
   Output currents must not exceed ±100mA
   Storage temperature must not exceed -60°C to +150°C
4. Specifications are tentative. Final specifications will be available by Jan. 1972.

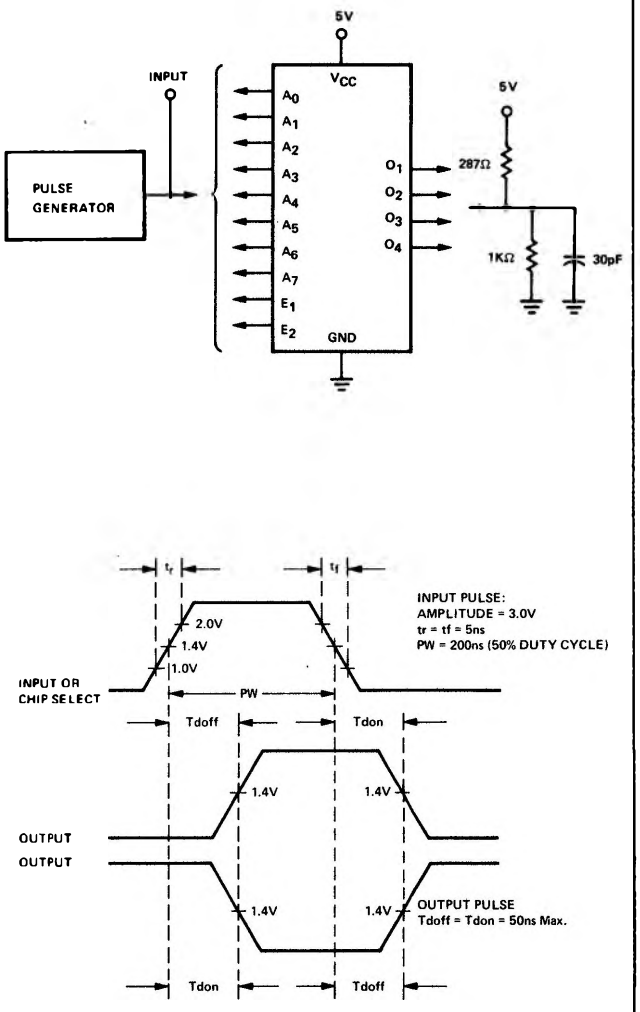
FUSING PROCEDURE

The 8226 and 8229 may be programmed by using the Curtis Electro Devices PR–24 or the Spectrum Dynamics Series 300 and 400 Programmers. Each perform the procedures outlined.

The 8226 and 8229 Standard parts, are shipped with all outputs at Logical "1". To write a logical "0" proceed as follows:

1. Remove V_{CC}.
2. Remove any load from the outputs.
3. Connect pin 13 to 5V, ± .25V and pin 14 to ground.
4. Address the desired location by applying ground for a "0" and 5.0±0.25V for a "1" at the address input pins.
5. Apply +12.5V to the output to be programmed through a 390Ω ± 10% resistor. Program one output at a time.
6. Apply +12.5V to V_{CC} (pin 16) for 50msec (1.0sec max). Do not exceed a 20% duty cycle. Limit the V_{CC} overshoot to 1.0 volts, max, by "clamp" or "crowbar" circuit. V_{CC} current requirement is 825mA max at 12.5 volts.
7. Remove V_{CC}.
8. Open the output.
9. Proceed to the next output and repeat, or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 8226/29.

AC TEST FIGURE AND WAVEFORM



Ground Pins 13 and 14 when testing address-Output delays