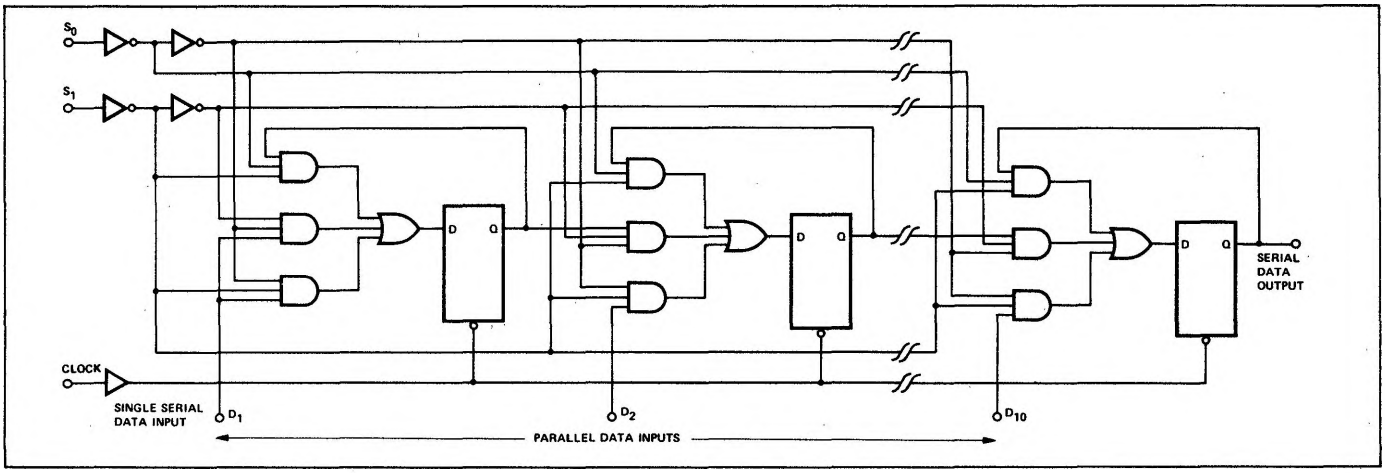
DESCRIPTION

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in, serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D_1 input can also be used for serial entry. Two control inputs, S_0 and S_1, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse. Guaranteed input clock frequency is 10MHz and the control inputs may be changed when the clock is in either the high or low state without causing false triggering. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmission, Pseudo-Random Code generation and Modulo-N Frequency Division.

TRUTH TABLE

S_0	S_1	OPERATING MODE
0	0	Hold
0	1	Clear
1	0	Load
1	1	Shift

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

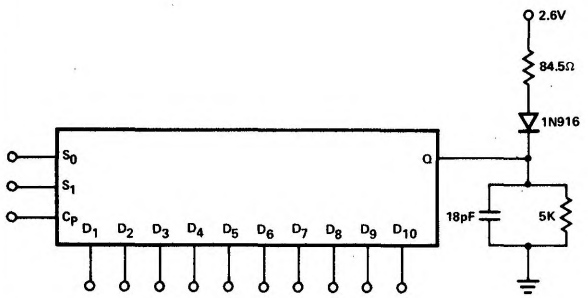
CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUTS	
"1" Output Voltage	2.6	3.4		V	2.0V	2.0V	2.0V	Pulse	-800μA	6
"0" Output Voltage		0.2	0.4	V	0.8V	2.0V	2.0V	Pulse	16mA	7
"0" Input Current										
D_n	-0.2		-1.6	mA	0.4V					
S_0 and S_1	-0.2		-1.6	mA		0.4V	0.4V			
Clock	-0.2		-2.5	mA				0.4V		
"1" Input Current										
D_n			40	μA	4.5V					
S_0 and S_1			40	μA		4.5V	4.5V			
Clock			40	μA				4.5V		

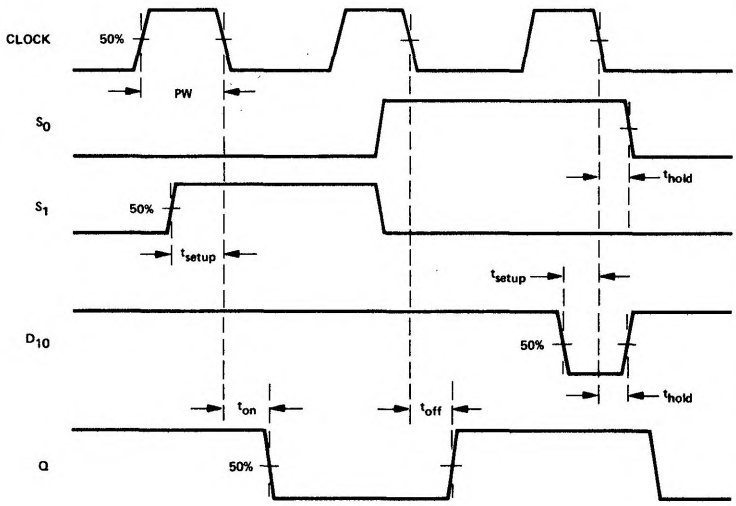
$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS					NOTES
	MIN.	TYP.	MAX.	UNITS	D_n	S_0	S_1	CLOCK	OUTPUTS	
Data Transfer Rate	10MHz	15		MHz						10
Turn-On Delay (Clock to Output)		28	50	ns						10
Turn-Off Delay (Clock to Output)		21	50	ns						10
Clock Pulse Width		40	50	ns						10
Set-Up Time (t_{setup})										10
D_n		10	15	ns						
S_0, S_1		20	25	ns						
Hold Time (t_{hold})										
D_n		4	10	ns						
S_0, S_1		9	15	ns						
Power Consumption		380	567	mW	4.5V	4.5V	4.5V	0V		8
Short Circuit Output Current	-20		-70	mA	2.0V	2.0V	2.0V	Pulse	0.0V	
Input Voltage Rating	5.5			V	10mA					

NOTES:
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. $V_{CC} = 5.25V$.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. See AC Test Figure.

AC TEST FIGURE AND WAVEFORMS





Clock Pulse Characteristics
Pulse Amplitude = 3.0V
t_r, $t_f \leq 10ns$
$PW \leq 50ns$