DESCRIPTION

The Up/Down Counter is a monolithic MSI circuit containing gates and binaries interconnected to provide a bi-directional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.

The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).

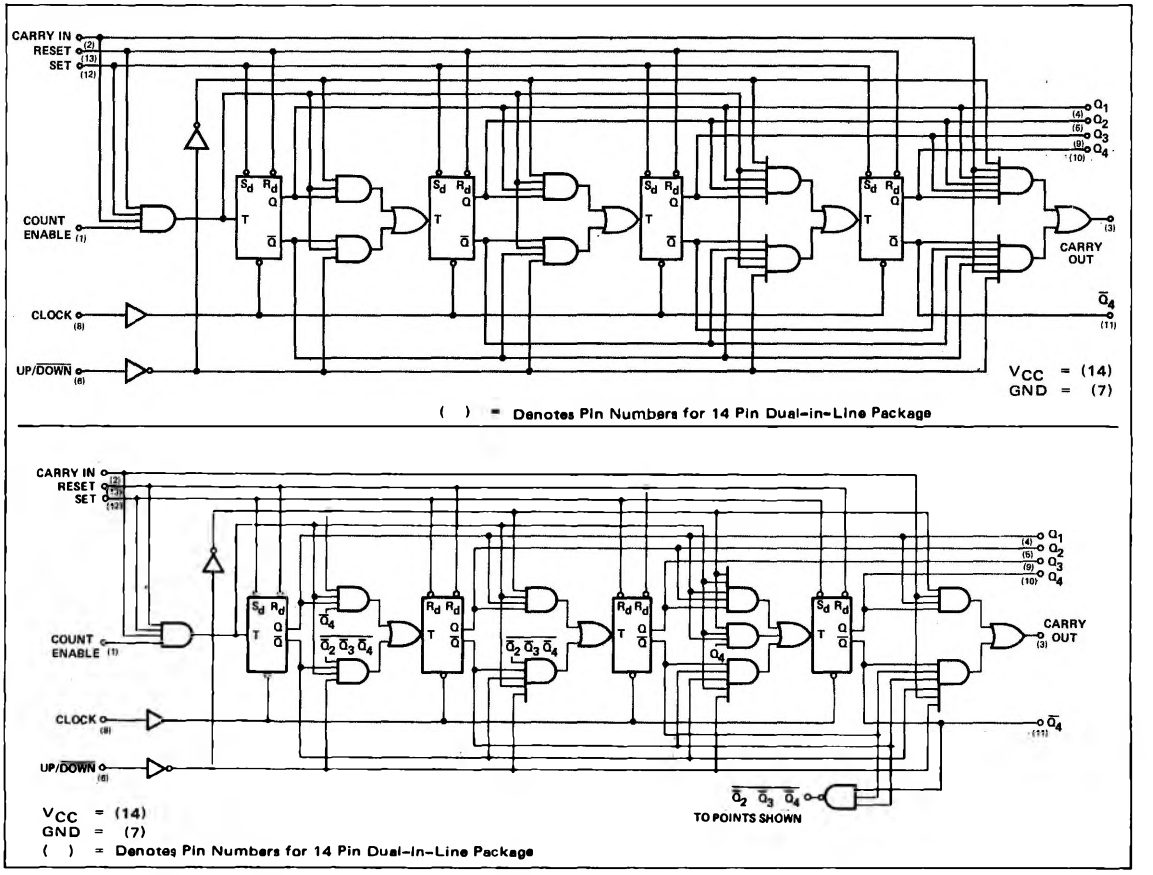
Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of "0" or "15" (8284) or of "0" or "9" (8285), and also inhibit propagation of count enable data.

Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry In" and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/$\overline{\text{Down}}$), where a "0" level will cause a "down" count and a "1" level will accomplish an "up" count.

In addition to all Q outputs of the four binaries the $\overline{Q}$ output of the most significant binary (Q4) and the Carry Out term are available.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
"1" Output Voltage												
Q_1, Q_4, Carry Out	2.6			V	0.8V	2.0V	2.0V			2.0V	-800μA	5
Q_2, Q_3, (8284)												
Q_2, Q_3 (8285)	2.6			V	Pulse		0.8V				-800μA	5, 9
$\overline{Q}_4$	2.6			V	2.0V	0.8V					-800μA	5
"0" Output Voltage												
Q_1,Q_2,Q_3,Q_4 and												
Carry Out			0.4	V	2.0V	0.8V				0.8V	9.6mA	6
$\overline{Q}_4$			0.4	V	0.8V	2.0V					9.6mA	6
"1" Input Current												
Carry In			120	μA	Pulse		5.0V			4.5V		
Set			200	μA	4.5V	Pulse						
Reset			40	μA	Pulse	4.5V						
Count Enable			40	μA				4.5V				
Clock and Up/Down			40	μA			4.5V		4.5V			
"0" Input Current												
Carry In	-0.1		-3.2	mA	Pulse		0V			0.4V		
Set	-0.1		-6.4	mA	0.4V							
Reset	-0.1		-1.6	mA		0.4V						
Count Enable	-0.1		-1.6	mA				0.4V				
Clock	-0.1		-1.6	mA					0.4V			
Up/Down	-0.1		-1.6	mA			0.4V					
Input Voltage Rating												
Carry In	5.5			V		0V	5.0V	0V		10mA		
Reset	5.5			V		10mA		0V		0V		
Set	5.5			V	10mA			0V		0V		
Count Enable	5.5			V	0V			10mA		0V		
Up/Down	5.5			V			10mA					
Output Short Circuit Current	-20		-70	mA							0V	8, 10

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS							NOTES
	MIN.	TYP.	MAX.	UNITS	SET	RESET	UP/DOWN	COUNT ENABLE	CLOCK	CARRY IN	OUTPUTS	
Power/Current Consumption		315/ 60	420/ 80	mW/ mA								10
Propagation Delay												
t_{on} Clock to Q_4 & $\overline{Q}_4$		32	45	ns								7
t_{on} Clock to Q_1, Q_2, Q_3		28	40	ns								7
t_{off} Clock to Q_n, $\overline{Q}_n$		25	35	ns								7
t_{on} Reset to Q_n		24	35	ns								7
t_{off} Set to Q_n		15	25	ns								7
t_{on} Reset to $\overline{Q}_n$		32	45	ns								7
t_{on} Carry In to Carry Out		15	25	ns								7
t_{off} Carry In to Carry Out		20	30	ns								7
Clock Min. "1" Interval	20	15		ns								7
Count Rate	20	30		MHz								
Carry In, Count Enable, & Up/Down Set-Up Time		15	25	ns								
Carry In, Count Enable & Up/Down Hold Time		0	2	ns								
Set/Reset Pulse Width		20	25	ns								

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to V_{CC}.
7. Refer to AC Test Figure.
8. Not more than one output should be shorted at a time.
9. Connect Q_4 to count enable, set the counter (1001), and count down. The counter will halt at BCD-7 (0111).
10. V_{CC} = 5.25 volts.[

AC TEST FIGURES AND WAVEFORMS

MODE OF OPERATION

8284 Binary Synchronous Up/Down Counter
8285 BCD Synchronous Up/Down Counter

	SET	RESET	CARRY IN	COUNT ENABLE	UP/$\overline{\text{DOWN}}$	FUNCTION
A. Asynchronous						
	1	0	X	X	X	"0" (0 0 0 0)
8284 Only	0	1	X	X	X	"15" (1 1 1 1)
8285 Only	0	1	X	X	X	"9" (1 0 0 1)
B. Synchronous						
	1	1	0	X	X	Hold *
	1	1	X	0	X	Hold *
	1	1	1	1	0	"Down" Count *
	1	1	1	1	1	"Up" Count *

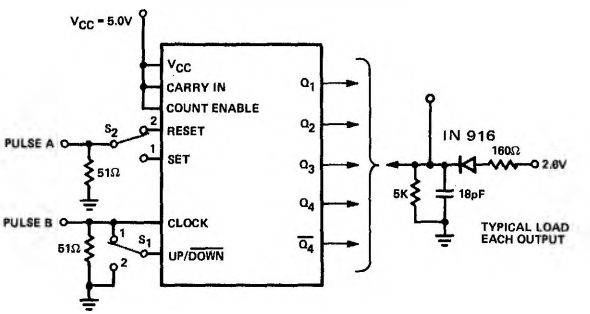
*Function is synchronous with NEGATIVE going transition of the Clock pin.
X = don't care.

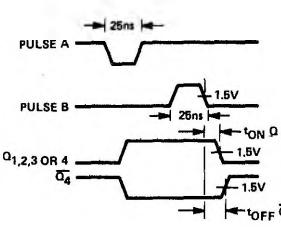
CARRY OUT

Carry Out_{8284} = Carry In ($Q_1Q_2Q_3Q_4$ UP + $\bar{Q}_1\bar{Q}_2\bar{Q}_3\bar{Q}_4$ $\overline{\text{DOWN}}$)

Carry Out_{8285} = Carry In (Q_1Q_4 UP + $\bar{Q}_1\bar{Q}_2\bar{Q}_3\bar{Q}_4$ $\overline{\text{DOWN}}$)

CLOCK MODE (t_{on} AND t_{off})

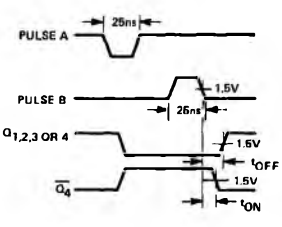




Reset Tied To V_{CC}
S_1' Position 1
S_2' Position 1

PULSE A

Pulse Amplitude = 2.6V
Pulse $Width_{(0)}$ = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points



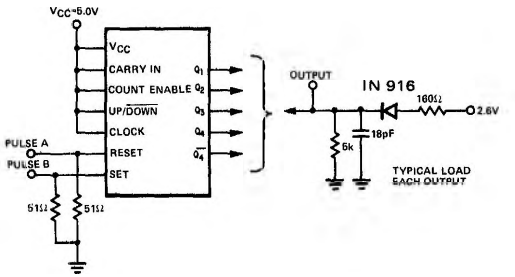
Set Tied To V_{CC}
S_1' Position 2
S_2' Position 2

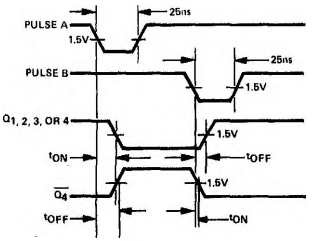
PULSE B

Pulse Amplitude = 2.6V
Pulse Width = 25ns at 1.5V
Frequency = 5 MHz
$t_r = t_f$ = 5ns at 10% to 90% Points

AC TEST FIGURES AND WAVEFORMS (Cont'd)

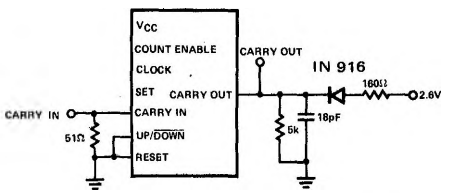
SET/RESET MODE (t_{on} and t_{off})

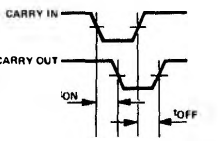




Pulse A and B
Pulse amplitude = 2.6V
Pulse width (0) =25ns
Frequency = 5MHz
$t_r = t_f$ =5ns at 10% to 90% points

CARRY IN/CARRY OUT (t_{on} and t_{off})





Carry in pulse
Pulse amplitude = 2.6V
Pulse width (0) = 50ns
Frequency =10MHz
$t_r = t_f$ =5ns at 10% to 90% points

TYPICAL APPLICATIONS

SYNCHRONOUS EXPANSION UP/DOWN COUNTERS