DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (-55°C to +125°C) specify S82S102/103, I.

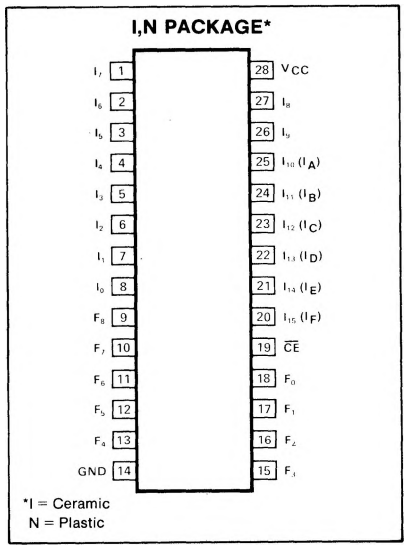
FEATURES

- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 30ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: -100μA max
  S82S102/103: -150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

APPLICATIONS

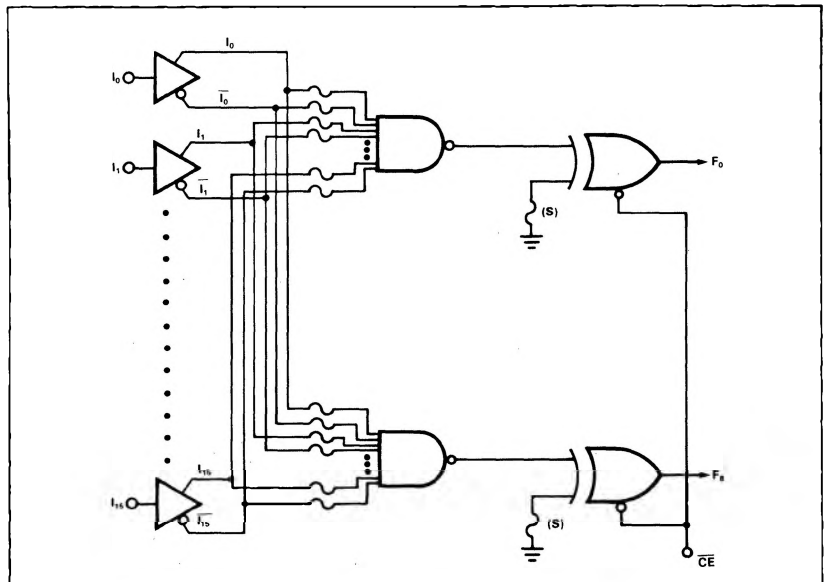
- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



*I = Ceramic
N = Plastic

LOGIC DIAGRAM

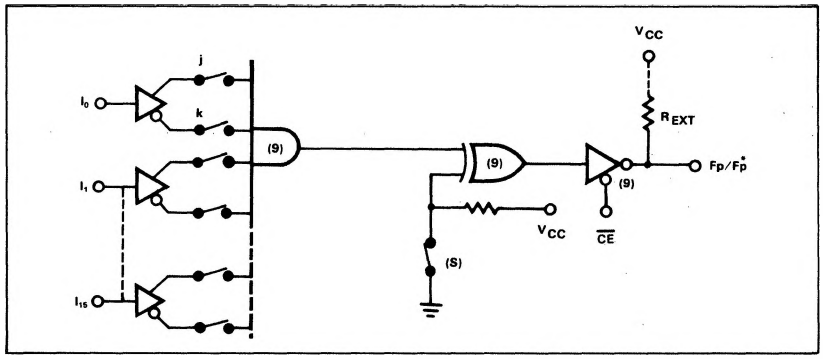


For each of the 9 outputs, either the function Fp (active high) or Fp (active low) is available, but not both. The required function polarity is user programmable via fuse (S).

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	-55 to +125	
T_{STG}	Storage	-65 to +150	

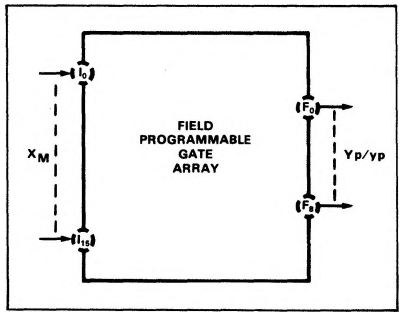
EQUIVALENT LOGIC PATH



The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_P) or active-low (F_P^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of *external* input logic variables X_m as defined below (positive logic):

At S = Open:
$F_P = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . X_m) = Y_P$
At S = Closed:
$F_P^* = \overline{CE} + (\overline{X}_0 + \overline{X}_1 + \overline{X}_2 + \ldots . X_m) = y_P$
$m = 0, 1, 2, \ldots . 15$

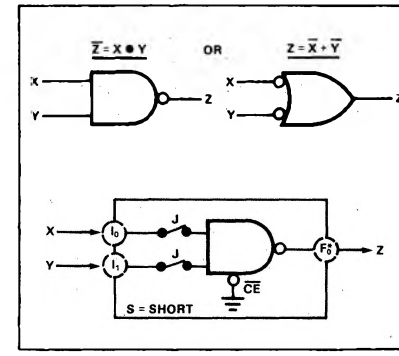


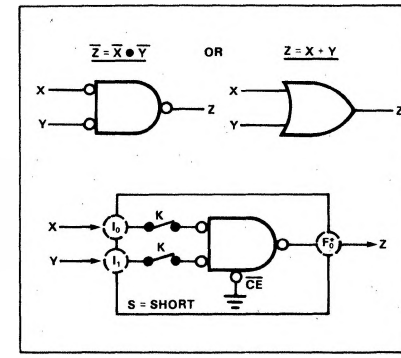
$p = 0, 1, 2, \ldots . 8$
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0- I_{15}.

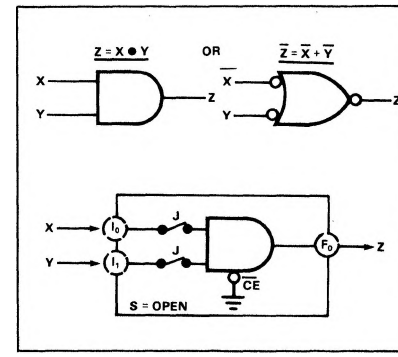
When $\overline{CE}$ = low, all gates are enabled, and $F_P^* = \overline{F}_P$ giving $y_P = \overline{Y}_P$.

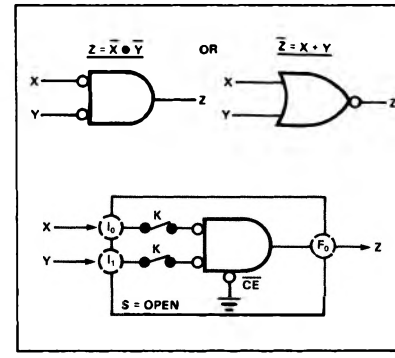
PROGRAMMABLE LOGIC FUNCTIONS

All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) of links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.









DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

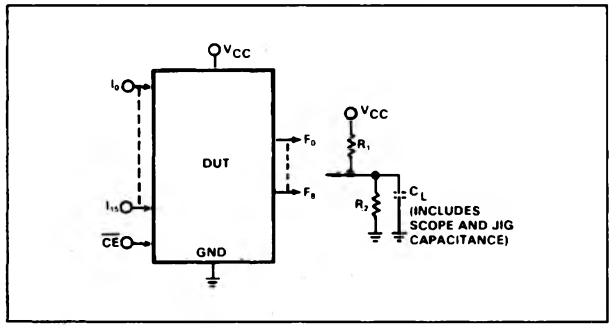
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	30		20	50	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	40	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	40	

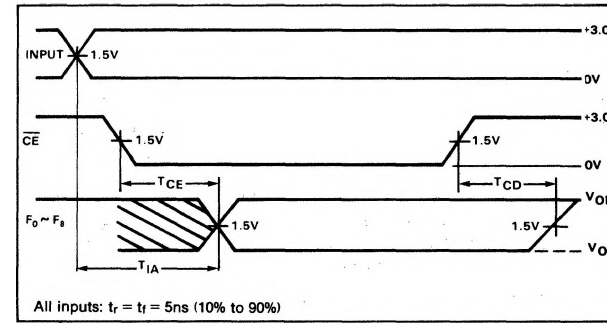
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

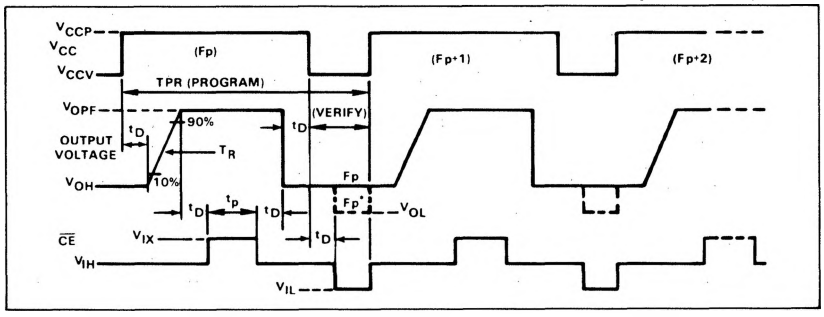
TEST LOAD CIRCUIT



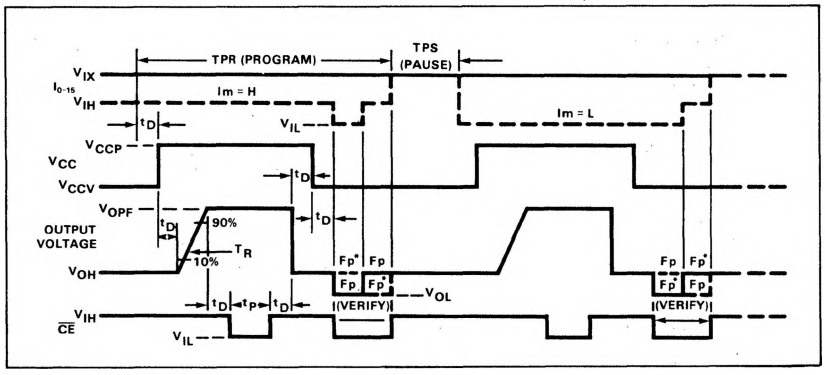
VOLTAGE WAVEFORM



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



INPUT MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



VIRGIN DEVICE

The 82S102/103 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each gate contains both true and complement values of every input variable I_m (logic Null state).
3. The polarity of each output is set to active low (F_p^* function).
4. All outputs are at a high logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 9 Boolean logic functions of 16 True, Complement, or Don't Care input variables follow the program/verify procedures for the Input Matrix and Output Polarity outlined below. To maximize recovery from programming errors, leave all links of unused gates intact.

SET-UP

Terminate all device outputs with a 10KΩ resistor to +5V.

Output Polarity

PROGRAM ACTIVE HIGH (Fp FUNCTION)

Program output polarity before programming inputs (for convenience). Program one output at a time. (S) links of unused outputs are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Raise V_{CC} (pin 28) from V_{CCV} to V_{CCP}.
B. After t_D delay, force output to be programmed to V_{OPF}.
C. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.
D. After t_D delay, remove V_{OPF} voltage source from output being programmed.
E. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
F. Repeat steps A through E for any other output.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. After t_D delay, set the $\overline{CE}$ input to V_{IL}.
B. Verify output polarity by sensing the logic state of outputs F_0 through F_8. All outputs at a low logic level are programmed active low (F_p^* function), while all outputs at a high logic level are programmed active high (F_p function).

Input Matrix

PROGRAM INPUT VARIABLE

Program one input at a time for one gate at a time. Input variable links of unused gates are not required to be fused. However, unused input variables must be programmed at Don't Care for all used gates.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A-1. If a gate contains nether I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both j and k links by executing both steps A-2 and A-3, before continuing with step C.
A-2. If a gate contains I_0, set to fuse the k link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step B.
A-3. If a gate contains $\overline{I_0}$, set to fuse the j link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
B-1. After t_D delay, raise V_{CC} from V_{CCV} to V_{CCP}.
B-2. After t_D delay, force output of gate to be programmed to V_{OPF}.
B-3. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IL} for a period t_p.
B-4. After t_D delay, remove V_{OPF} voltage source from output of gate being programmed.
B-5. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
C. Disable programmed input by returning I_0 to V_{IX}.
D. Repeat steps A through C for all other input variables.
E. Repeat steps A through D for all other gates to be programmed.
F. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

Unambiguous verification of the logic state programmed for the inputs of each gate requires prior knowledge of its programmed output polarity. Therefore, the output polarity verify procedure must precede input variable verify.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Enable all outputs by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Interrogate input variable I_0 as follows: Lower the input voltage to I_0 from V_{IX} to V_{IL}, and sense the logic state of outputs F_{0-8}.

Raise the input voltage to I_0 from V_{IL} to V_{IH} and sense the logic state of outputs F_{0-8}.

The state of I_0 contained in each gate is determined in accordance with the given truth table. Note that 2 tests are required to uniquely determine the state of the input variable contained in each gate.

B. Disable verified input by returning I_0 to V_{IX}.

C. Repeat steps A and B for all other input variables.

D. Remove V_{IX} from all input variables.

TRUTH TABLE FOR INPUT VERIFICATION

I_0	Fp	$F\dot{p}$	INPUT VARIABLE STATE	LINK FUSED
0	1	0	$\bar{I}_0$	j
1	0	1		
0	0	1	I_0	k
1	1	0		
0	1	0	Don't care	Both
1	1	0		
0	0	1	(I_0), ($\bar{I}_0$)	Neither
1	0	1		

PROGRAMMING SYSTEMS SPECIFICATIONS[1] $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	V_{CC} supply					V
V_{CCP}	Program[2]	I_{CCP} = 350 ± 50mA, Transient or steady state	8.5	8.75	9.0	
V_{CCV}	Verify		4.75	5.0	5.25	
I_{CCP}	I_{CC} limit (program)	V_{CCP} = +8.75 ± .25V, Transient or steady state	400	450	500	mA
V_{OPF}	Forced output voltage[3] (program)	I_{OP} = 150 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current limit (program)	V_{OP} = +17 ± 1V, Transient or steady state	125	150	175	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			5.0	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10.0	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				100	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

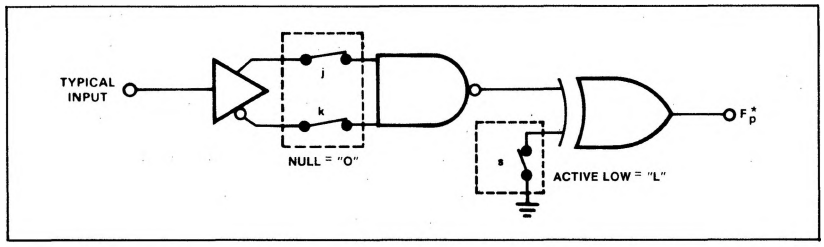
1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of a gate output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

PROGRAMMING

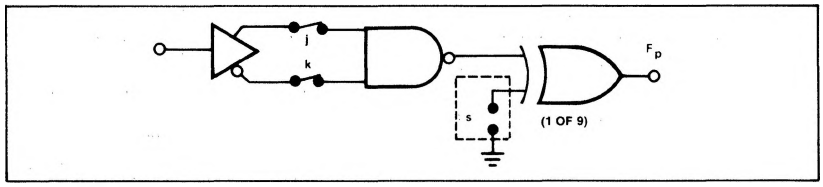
In a virgin device all Ni-Cr links are intact. The initial programmed state of each gate is shown in the Typical Gate illustration.

To program inputs and outputs of each gate for implementing the desired logic function, fuse Ni-Cr links as indicated in the fuse link diagrams.

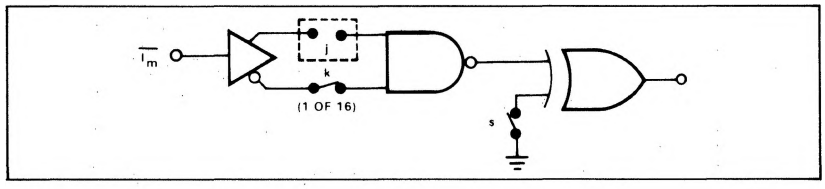
TYPICAL GATE



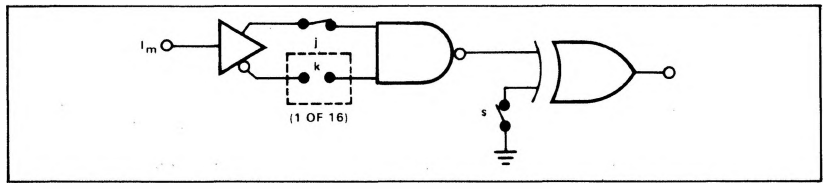
OUTPUT ACTIVE HIGH = FUSE LINK S



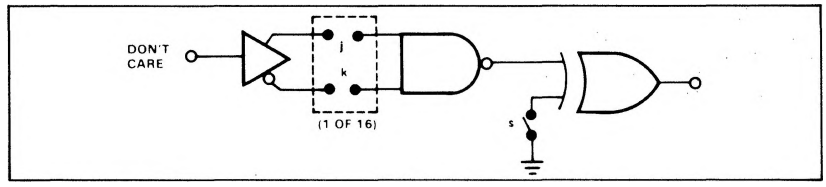
INPUT $\overline{I}m$ = FUSE LINK J



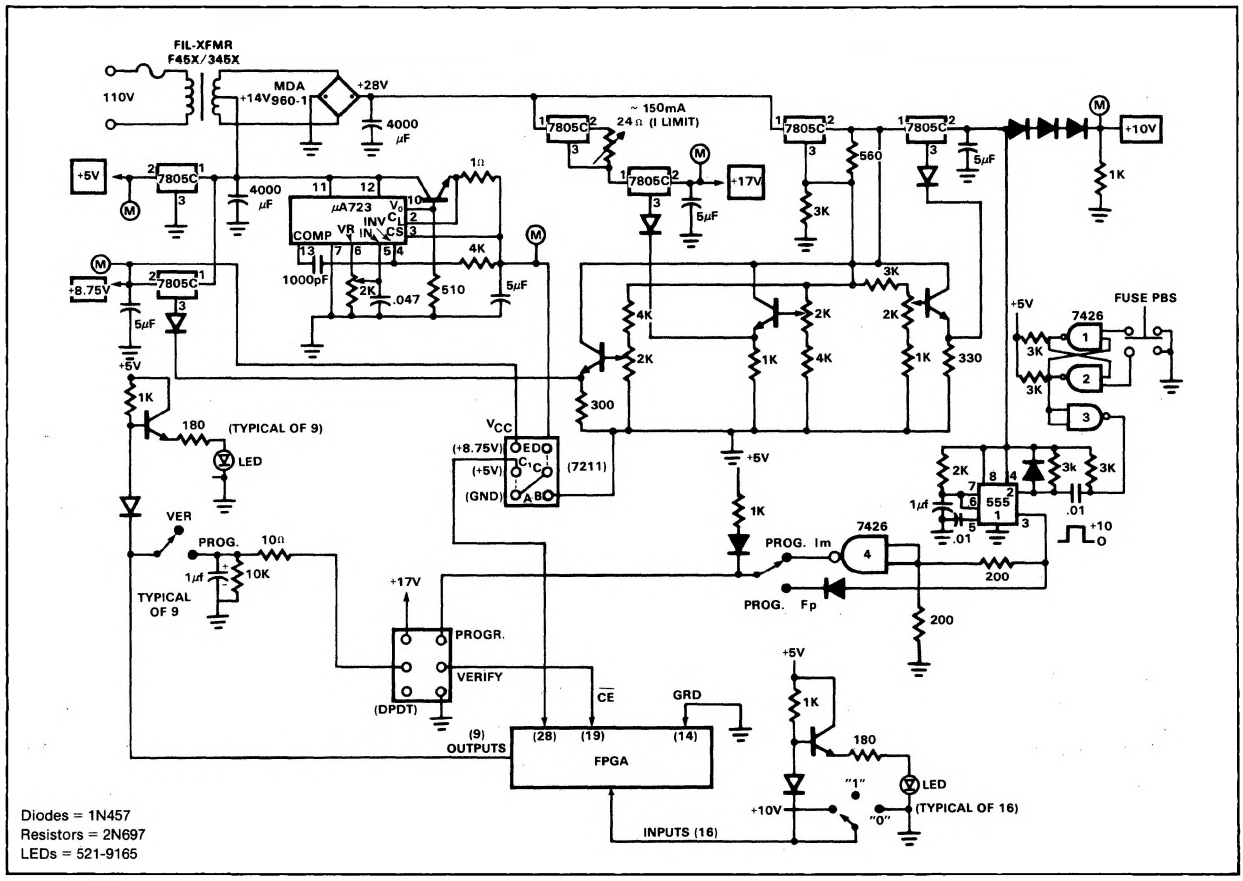
INPUT Im = FUSE LINK K



INPUT DON'T CARE = FUSE BOTH LINKS J, K



FPGA MANUAL FUSER



16X9 FPGA PROGRAM TABLE

CUSTOMER NAME _____	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # _____	*CF (XXXX)* _____
SIGNETICS DEVICE # _____	*CUSTOMER SYMBOLIZED PART #* _____
TOTAL NUMBER OF PARTS _____	*DATE RECEIVED* _____
PROGRAM TABLE # _____	*COMMENTS* _____

F_0 = _____

F_1 = _____

F_2 = _____

F_3 = _____

F_4 = _____

F_5 = _____

F_6 = _____

F_7 = _____

F_8 = _____

OUTPUT POLARITY		INPUT VARIABLE															
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_A	I_B	I_C	I_D	I_E	I_F
F_0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
F_1	16	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
F_2	32	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
F_3	48	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
F_4	64	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
F_5	80	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
F_6	96	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
F_7	112	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
F_8	128	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
Active-high = H Active-low = L		I_m = H $\overline{I_m}$ = L Don't Care = —															

The number in each cell in the table denotes its address for programmers with a decimal address display.