OBJECTIVE SPECIFICATION

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S23 (open Collector Outputs) and the 82S123 (Tristate Outputs) are Bipolar 256 Bit Read Only Memories organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. A chip enable line is provided and the outputs are bare collector or Tristate to allow for memory expansion capability.

The 82S23 and 82S123 are fully TTL compatible and include on-the-chip decoding. Typical access time is 25 nS.

The standard 82S23 and 82S123 are supplied with all outputs at a logical "0." If a programmed unit is required the Truth Table/Order Blank on page 4-43 of the TTL MSI/Memory Handbook may be used.

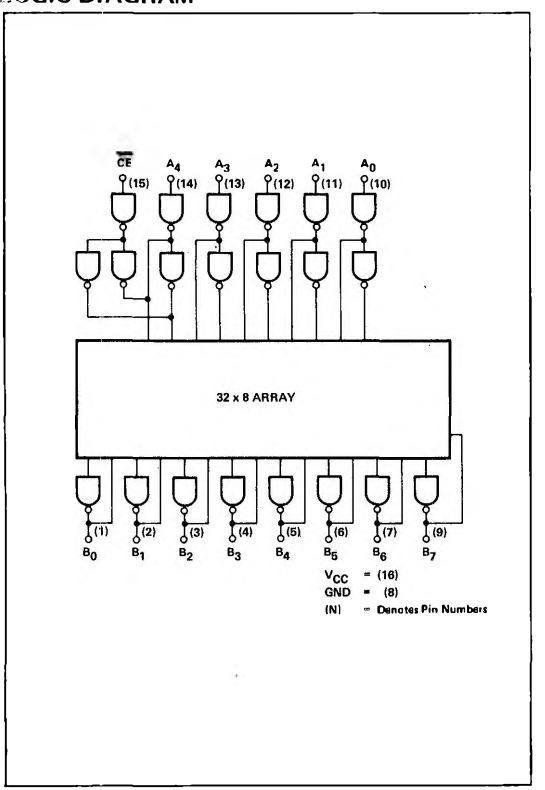
FEATURES

- PNP INPUTS
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- A CHIP ENABLE LINE
- OPEN COLLECTOR OR TRISTATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- BOARD PROGRAMMABLE

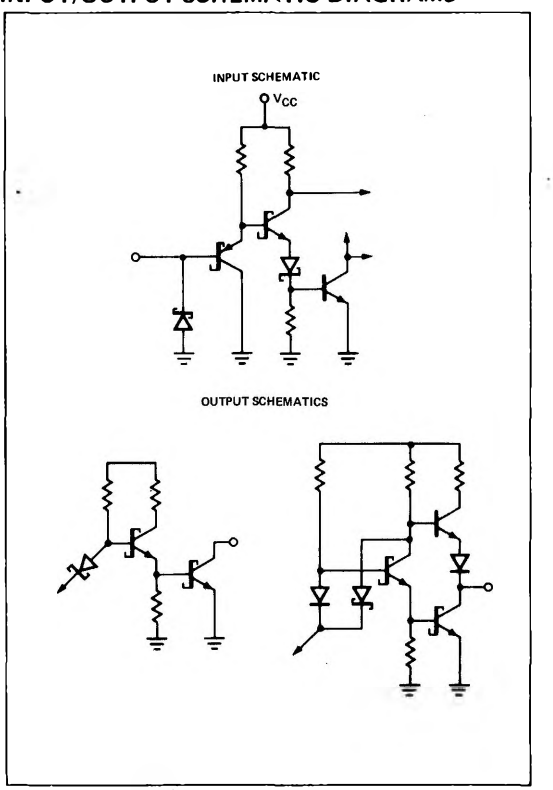
APPLICATIONS

- PROTOTYPING
- VOLUME PRODUCTION
- MICROPROGRAMMING
- HARDWIRED ALGORITHMS
- CONTROL STORE

LOGIC DIAGRAM



INPUT/OUTPUT SCHEMATIC DIAGRAMS



OBJECTIVE ELECTRICAL CHARACTERISTICS (T_A = 25°C and V_{CC} = 5.0V)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"0" Output Voltage				V	I_{out} = 20mA	
"1" Output Leakage			40	μA	CE = "1" V_{out} = 2.6V	
82S23			100	μA	CE = "0" V_{out}=2.6V After Fusing	
82S123	-40		+40	μA	V_{out} = 0.5V/V_{out} = 2.4V, CE = "1"	
"1" Output Current 82S123	- 2.0			mA	V_{out} = 2.4V, CE = "0"	After Fusing
"0" Input Current			250	μA	V_{in} = 0.5V	
"1" Input Current			50	μA	V_{in} = 2.7V	
Input Threshold Voltage						
"0" Level	.80			V		
"1" Level			2.0	V		
Propagation Delay						
Address to Output		25	40	ns		
Enable to Output		15	35	ns		
Input Clamp Voltage	-1.0			V	I_{in} = 5.0mA	
Power Consumption					V_{cc} = 5.00V	
82S23		80/400	100/500	mA/mW		
82S123		80/400	100/500	mA/mW		

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1" "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8 mA.
8. One AC fan-out is defined as 50 pF.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. By DC tests per the truth table, all inputs have guaranteed thresholds of 0.8V for logical "0" and 2.0V for logical "1".
11. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
12. For detailed conditions, see AC testing.
13. Connect an external 1K resistor from V_{CC} to the output terminal for this test.
14. V_{CC} = 5.25V.

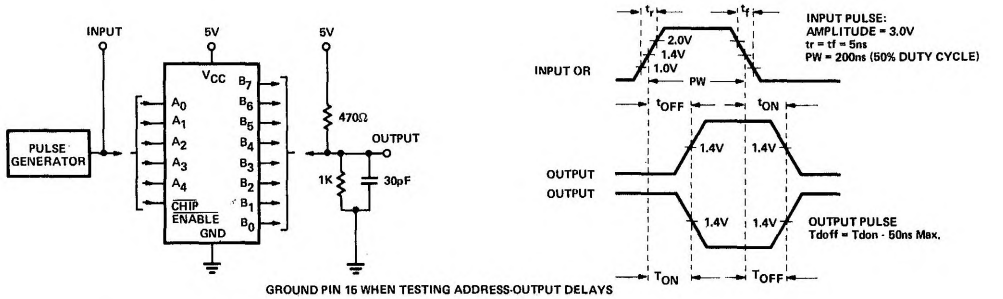
OBJECTIVE FUSING PROCEDURE

The 82S23/82S123 standard part is shipped with all outputs at Logical "0". To write a Logical "1" proceed as follows:
1. GND Pin 8 and apply 5V to V_{CC}, Pin 16.
2. Remove any load from the outputs.
3. Ground the Chip Enable.
4. Address the desired location by applying ground for a "0" and 5.0 ±0.25V for a "1" at the address input lines.
5. Raise V_{CC} to 10.0V ±0.5V.
6. Apply 65 ±3 mA to the output to be programmed to logic "1". (The voltage will be between 12 to 18V until fused, and must be clamped at 20.0V max.)
7. Release fusing current.
8. Reduce V_{CC} to 5.0V.
9. Proceed to the next output and repeat,or change address and repeat procedure.
10. Continue until the entire bit pattern is programmed into your custom 82S23/82S123.

NOTE:

After 1.0 SEC of programming, a 25% duty cycle on power must be imposed to avoid over heating.

AC TEST FIGURE AND WAVEFORMS



FUNCTIONAL DIAGRAM