

2-INPUT, 4-BIT DIGITAL MULTIPLEXER

82S66 82S67

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S66/82S67 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing Schottky TTL circuit structures. The 82S67 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

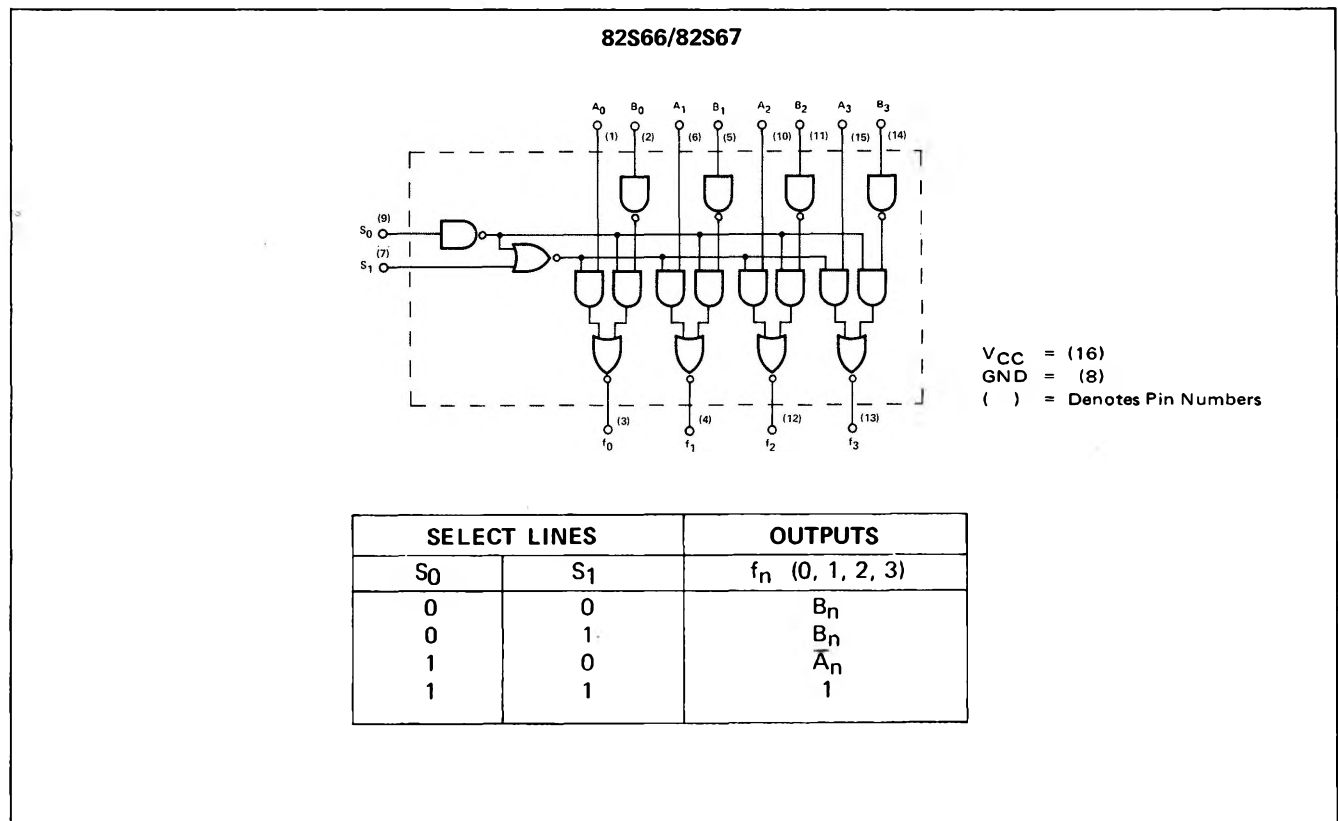
The multiplexer is able to choose from two different input sources, each containing 4 bits: $A = (A_0, A_1, A_2, A_3)$, $B = (B_0, B_1, B_2, B_3)$. The selection is controlled by the input S_0 , while the second control input, S_1 , is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with adder elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS
- OPEN COLLECTOR OUTPUTS (82S67)
- INHIBIT STATE

LOGIC DIAGRAM AND TRUTH TABLE



SIGNETICS DIGITAL 8000 SERIES TTL/MSI – 82S66/67

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A _n	B _n	S ₀	S ₁		
"1" Output Voltage (82S66)	2.7	3.5		V	0.8V	2.0V	0.8V	0.8V	–1mA	
"0" Output Voltage			0.5	V	2.0V	2.0V	2.0V	0.8V	20mA	
"1" Output Leakage Current (82S67)			250	μA	0.8V	2.0V	2.0V	0.8V	5.5V	
"0" Input Current										
A _n , B _n			–400	μA	0.5V	0.5V	0V	0V		
S ₀ , S ₁			–400	μA			0.5V	0.5V		
"1" Input Current										
A _n , B _n			10	μA	4.5V	4.5V		2.0V		
S ₀ , S ₁			10	μA			4.5V	4.5V		
Output Short Circuit Current (82S66)	–40		–100	mA						12

T_A = 25°C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
	MIN	TYP	MAX	UNITS	A _n	B _n	S ₀	S ₁		
Turn-on/Turn-off Times (82S66)										
S ₁ to f _n			15	ns						9
S ₀ to f _n			18	ns						9
A _n to f _n			10	ns						9
B _n to f _n			12	ns						9
Propagation Delay (82S67)										
S ₁ to f _n			18	ns						9
S ₀ to f _n			20	ns						9
A _n to f _n			12	ns						9
B _n to f _n			15	ns						9
Power/Current Consumption			365/69	mW/mA	4.5V	0V	4.5V	0V		12

NOTES:

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND logic definition:
"UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC}.
- Refer to AC Test Figure.
- This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
- Manufacturer reserves the right to make design and process changes and improvements.
- V_{CC} = 5.25 V.

AC TEST FIGURE AND WAVEFORMS

