INTEGRATED CIRCUITS

DATA SHEET

80C528/83C528

CMOS single-chip 8-bit microcontroller

Product specification 1995 Feb 02

IC20 Data Handbook

Philips
Semiconductors

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CMOS single-chip 8-bit microcontrollers | 80C528/83C528

DESCRIPTION

The 8XC528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C528 — 32k bytes mask programmable ROM
- 80C528 — ROMless version of the 83C528
- 87C528 — 32k bytes EPROM (described in a separate data sheet)

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

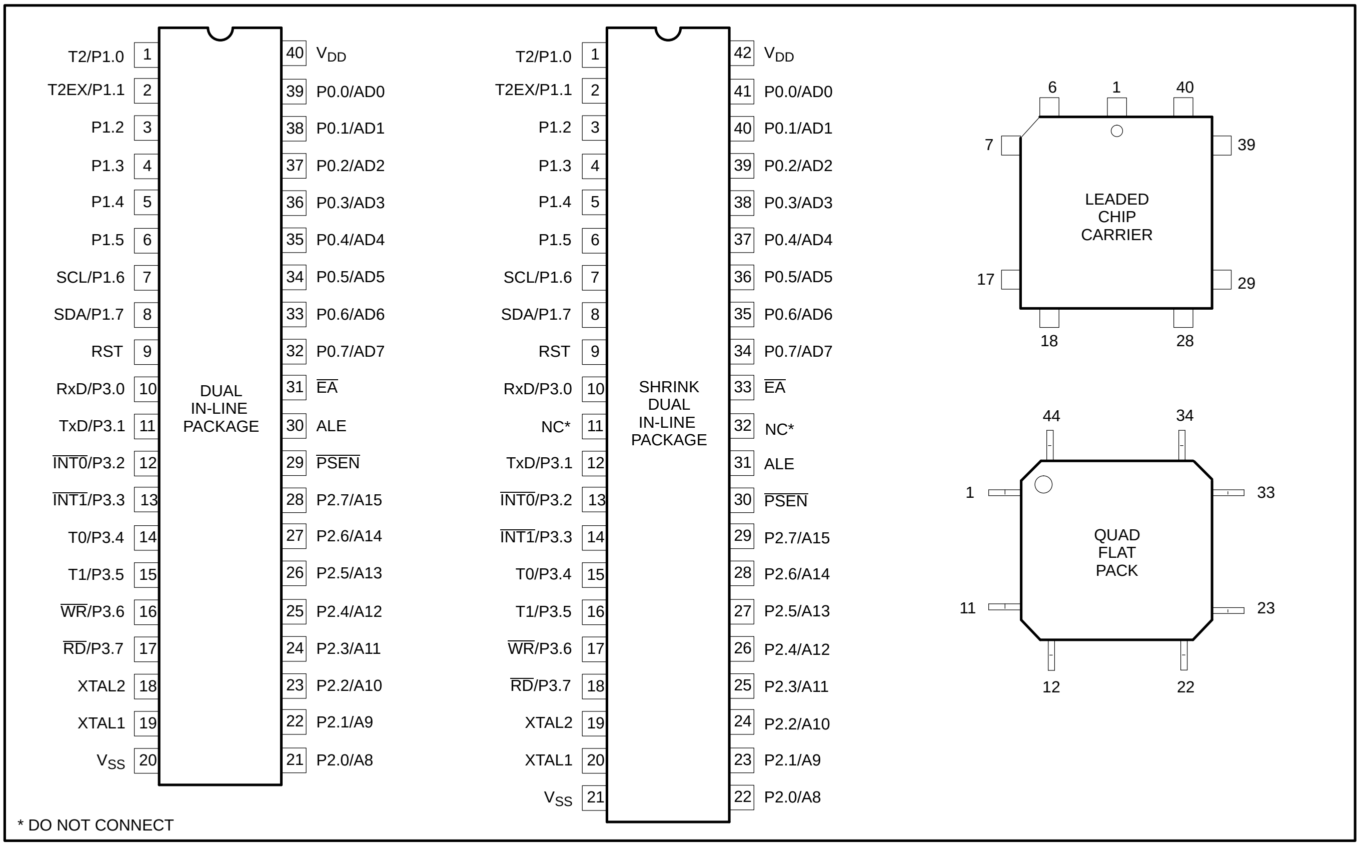
The 8XC528 contains a 32k × 8 ROM (83C528), a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I^{2}C-bus), and on-chip oscillator and timing circuits.

In addition, the 8XC528 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

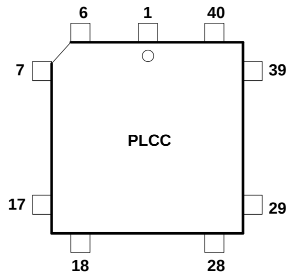
- 80C51 instruction set
  - 32k × 8 ROM (83C528)
  - ROMless (80C528)
  - 512 × 8 RAM
  - Memory addressing capability
    64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I^{2}C serial interface
  - Four 8-bit I/O ports
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Extended temperature ranges
- ROM code protection
- 7-source and 7-vector interrupt structure with 2 priority levels
- Up to 3 external interrupt request inputs
- Two programmable power reduction modes (Idle and Power-down)
- Termination of Idle mode by any interrupt, external or WDT (watchdog) reset
- XTAL frequency range: 1.2 MHz to 16 MHz

PIN CONFIGURATIONS



* DO NOT CONNECT

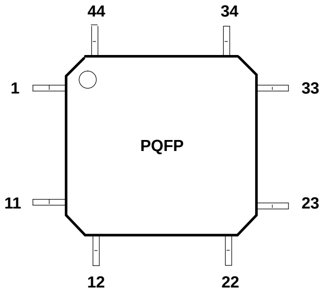
CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC*	23	NC*
2	P1.0/T2	24	P2.0/A8
3	P1.1/T2EX	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{\text{PSEN}}$
11	P3.0/RxD	33	ALE
12	NC*	34	NC*
13	P3.1/TxD	35	$\overline{\text{EA}}$
14	P3.2/$\overline{\text{INT0}}$	36	P0.7/AD7
15	P3.3/$\overline{\text{INT1}}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{\text{WR}}$	40	P0.3/AD3
19	P3.7/$\overline{\text{RD}}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{DD}

* DO NOT CONNECT

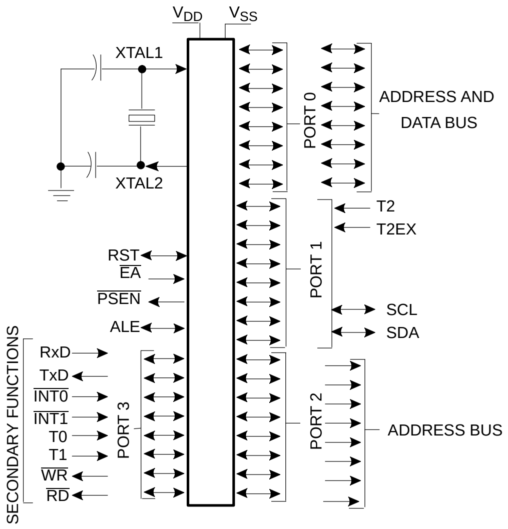
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{\text{PSEN}}$
5	P3.0/RxD	27	ALE
6	NC*	28	NC*
7	P3.1/TxD	29	$\overline{\text{EA}}$
8	P3.2/$\overline{\text{INT0}}$	30	P0.7/AD7
9	P3.3/$\overline{\text{INT1}}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{\text{WR}}$	34	P0.3/AD3
13	P3.7$\overline{\text{RD}}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC*	39	NC*
18	P2.0/A8	40	P1.0/T2
19	P2.1/A9	41	P1.1/T2EX
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

* DO NOT CONNECT

LOGIC SYMBOL



ORDERING INFORMATION

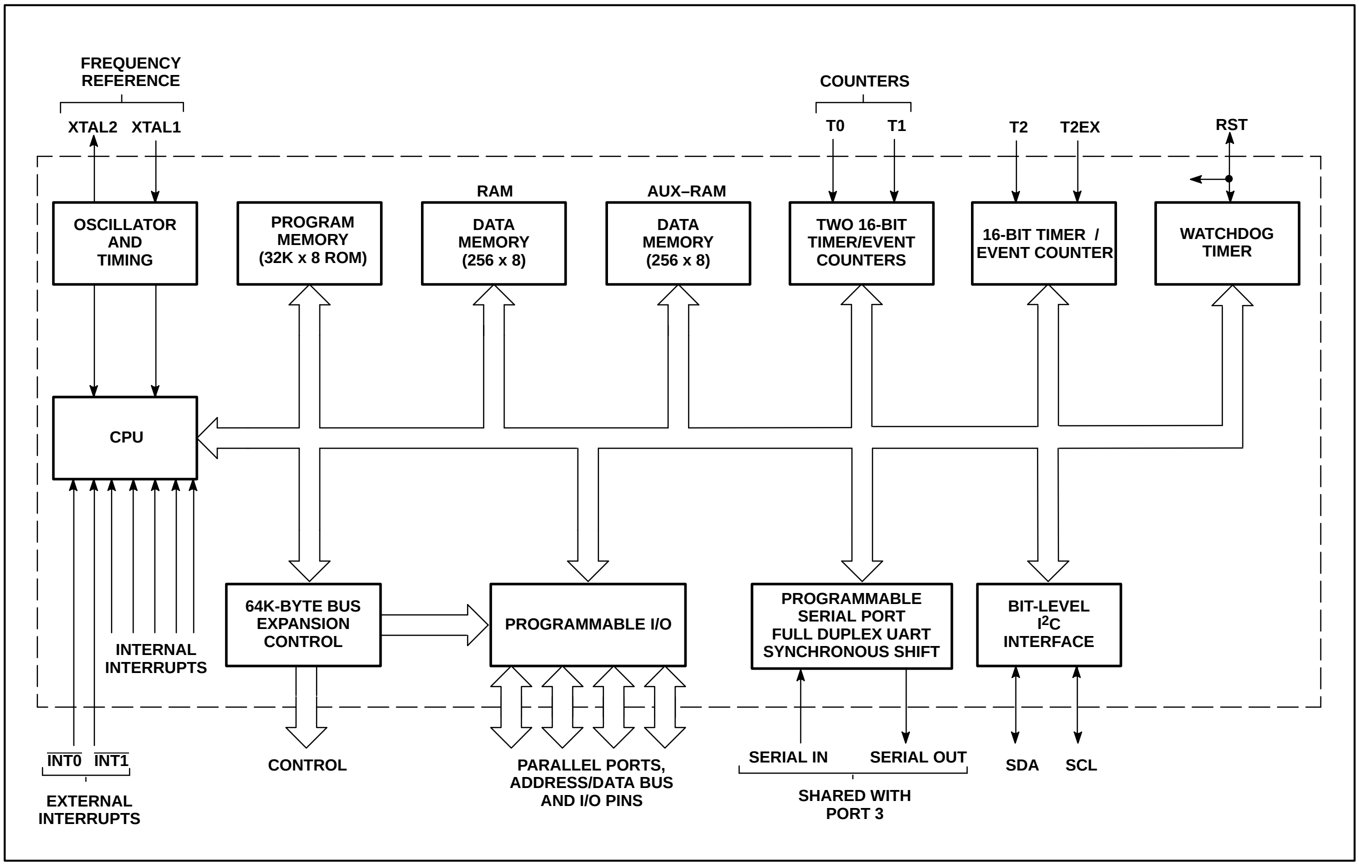
PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER			TEMPERATURE ^{o}C RANGE AND PACKAGE	FREQ MHz
ROMless	**ROM**	**ROMless**	**ROM**	**Drawing Number**		
P80C528FBP	P83C528FBP/xxx	P80C528FBP N	P83C528FBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P80C528FBA	P83C528FBA/xxx	P80C528FBA A	P83C528FBA A	SOT187-2	0 to +70, Plastic Leaded Chip Carrier	16
P80C528FBB	P83C528FBB/xxx	P80C528FBB B	P83C528FBB B	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
P80C528FFP	P83C528FFP/xxx	P80C528FFP N	P83C528FFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P80C528FFA	P83C528FFA/xxx	P80C528FFA A	P83C528FFA A	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier	16
P80C528FFB	P83C528FFB/xxx	P80C528FFB B	P83C528FFB B	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
P80C528FHP	P83C528FHP/xxx	P80C528FHP N	P83C528FHP N	SOT129-1	–40 to +125, Plastic Dual In-line Package	16
P80C528FHA	P83C528FHA/xxx	P80C528FHA A	P83C528FHA A	SOT187-2	–40 to +125, Plastic Leaded Chip Carrier	16
P80C528FHB	P83C528FHB/xxx	P80C528FHB B	P83C528FHB B	SOT307-2	–40 to +125, Plastic Quad Flat Pack	16
	P83C528FBR/xxx			SOT270-1	0 to +70, Plastic Shrink Dual In-Linr Package	16

NOTE:

1. xxx denotes the ROM code number.

EPROM	Drawing Number	TEMPERATURE °C RANGE AND PACKAGE	FREQ MHz
P87C528EBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	16
P87C528EBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	16
P87C528EBA AA	SOT187-2	0 to +70, Plastic Leaded Chip Carrier	16
P87C528EBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
P87C528EBB B	SOT307-2	0 to +70, Plastic Quad Flat Pack	16
P87C528EFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	16
P87C528EFF FA	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	16
P87C528EFF FA	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier	16
P87C528EFL KA	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
P87C528EFB B	SOT307-2	–40 to +85, Plastic Quad Flat Pack	16
P87C528GBP N	SOT129-1	0 to +70, Plastic Dual In-line Package	20
P87C528GBF FA	0590B	0 to +70, Ceramic Dual In-line Package w/Window	20
P87C528GBA A	SOT187-2	0 to +70, Plastic Leaded Chip Carrier	20
P87C528GBL KA	1472A	0 to +70, Ceramic Leaded Chip Carrier w/Window	20
P87C528GFP N	SOT129-1	–40 to +85, Plastic Dual In-line Package	20
P87C528GFF FA	0590B	–40 to +85, Ceramic Dual In-line Package w/Window	20
P87C528GFA A	SOT187-2	–40 to +85, Plastic Leaded Chip Carrier	20
P87C528GFL KA	1472A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	20

BLOCK DIAGRAM



PIN DESCRIPTION

	PIN NO.					
MNEMONIC	**DIP**	**SDIL**	**LCC**	**QFP**	**TYPE**	**NAME AND FUNCTION**
V_{SS}	20	21	22	16	I	**Ground:** circuit ground potential.
V_{DD}	40	42	44	38	I	**Power Supply:** +5V power supply pin during normal operation, Idle mode and Power-down mode.
P0.0–0.7	39–32	41–34	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	1–8	2–9	40–44 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which have open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 can sink/source one TTL (4 LSTTL) inputs.
	1	1	2	40	I	**T2 (P1.0):** Timer/counter 2 external count input (following edge triggered).
	2	2	3	41	I	**T2EX (P1.1):** Timer/counter 2 trigger input.
	7	7	8	2	I/O	**SCL (P1.6):** I^2C serial port clock line.
	8	8	9	3	I/O	**SDA (P1.7):** I^2C serial port data line.
P2.0–P2.7	21–28	22–29	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	10–18 (11=NC)	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the SC80C51 family, as listed below:
	10	10	11	5	I	**RxD (P3.0):** Serial input port
	11	12	13	7	O	**TxD (P3.1):** Serial output port
	12	13	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	13	14	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	14	15	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	16	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	17	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	18	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	9	9	10	4	I/O	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}. After a watchdog timer overflow, this pin is pulled high while the internal reset signal is active.
ALE	30	31	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{\text{PSEN}}$	29	30	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}$	31	33	35	29	I	**External Access Enable:** $\overline{\text{EA}}$ must be externally held low during RESET to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{\text{EA}}$ is held high during RESET, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. $\overline{\text{EA}}$ is don't care after RESET.
XTAL1	19	20	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	19	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

Table 1. 8XC524/8XC528 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes):										
DPH	Data pointer high	83H									00H
DPL	Data pointer low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*#	Interrupt enable	A8H	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*#	Interrupt priority	B8H	–	PS1	PT2	PS0	PT1	PX1	PT0	PX0	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	SDA	SEL	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON	Power control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
RCAP2H#	Capture high	CBH									00H
RCAP2L#	Capture low	CAH									00H
SBUF	Serial data buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial controller	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
S1BIT#	Serial I^{2}C data	D9H/RD	SDI	0	0	0	0	0	0	0	x0000000B
		WR	SD0	X	X	X	X	X	X	X	0xxxxxxxB
S1INT#	Serial I^{2}C interrupt	DAH	INT	X	X	X	X	X	X	X	0xxxxxxxB
			DF	DE	DD	DC	DB	DA	D9	D8	
S1SCS*#	Serial I^{2}C control	D8H/RD	SDI	SCI	CLH	BB	RBF	WBF	STR	ENS	xxxx0000B
		WR	SD0	SC0	CLH	X	X	X	STR	ENS	00xxxx00B
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*#	Timer 2 control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
TH0	Timer high 0	8CH									00H
TH1	Timer high 1	8DH									00H
TH2#	Timer high 2	CDH									00H
TL0	Timer low 0	8AH									00H
TL1	Timer low 1	8BH									00H
TL2#	Timer low 2	CCH									00H
T3#	Watchdog timer	FFH									00H
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
WDCON#	Watchdog control	A5H									A5H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

Table 2. Internal and External Program Memory Access with Security Bit Set

INSTRUCTION	ACCESS TO INTERNAL PROGRAM MEMORY	ACCESS TO EXTERNAL PROGRAM MEMORY
MOVC in internal program memory	YES	YES
MOVC in external program memory	NO	YES

ROM CODE PROTECTION

By setting a mask programmable security bit, the ROM content in the 83C528 is protected, i.e., it cannot be read out by any test mode or by any instruction in the external program memory space. The MOVC instructions are the only ones which have access to program code in the internal or external program memory. The $\overline{EA}$ input is latched during RESET and is 'don't care' after RESET (also if security bit is not set). This implementation prevents reading from internal program code by switching from external program memory to internal program memory during MOVC instruction or an instruction that handles immediate data. Table 2 lists the access to the internal and external program memory by the MOVC instructions when the security bit has been set to logical one. If the security bit has been set to a logical 0 there are no restrictions for the MOVC instructions.

INTERNAL DATA MEMORY

The internal data memory is divided into three physically separated segments: 256 bytes of RAM, 256 bytes of AUX-RAM, and a 128 bytes special function area. These can be addressed each in a different way.

- RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
- RAM 128 to 255 can only be addressed indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
- AUX-RAM 0 to 255 is indirectly addressed in the same way as external data memory with the MOVX instructions. Address pointers are R0, R1 of the selected register bank and DPTR. An access to AUX-RAM 0 to 255 will not affect ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 255 will be performed with the MOVX DPTR instructions in the same way as in the 8051 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that these external data memory cannot be accessed with R0 and R1 as address pointer.

TIMER 2

Timer 2 is functionally equal to the Timer 2 of the 8052AH. Timer 2 is a 16-bit timer/counter. These 16 bits are formed by two special function registers TL2 and TH2. Another pair of special function register RCAP2L and RCAP2H form a 16-bit capture register or a 16-bit reload register. Like Timer 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2N in the special function register T2CON. It has three operating modes: capture, autoload, and baud rate generator mode which are selected by bits in T2CON.

WATCHDOG TIMER T3

The watchdog timer consists of an 11-bit prescaler and an 8-bit timer formed by special function register T3. The prescaler is incremented by an on-chip oscillator with a fixed frequency of 1MHz. The maximum tolerance on this frequency is –50% and +100%. The 8-bit timer increments every 2048 cycles of the on-chip oscillator. When a timer overflow occurs, the microcontroller is reset and a reset output pulse of 16 × 2048 cycles of the on-chip oscillator is generated at pin RST. The internal RESET signal is not inhibited when the external RST pin is kept low by, for example, an external reset circuit. The RESET signal drives port 1, 2, 3 into the high state and port 0 into the high impedance state.

The watchdog timer is controlled by one special function register WDCON with the direct address location A5H. WDCON can be read and written by software. A value of A5H in WDCON halts the on-chip oscillator and clears both the prescaler and timer T3. After the RESET signal, WDCON contains A5H. Every value other than A5H in WDCON enables the watchdog timer. When the watchdog timer is enabled, it runs independently of the XTAL-clock.

Timer T3 can be read on the fly. Timer T3 can only be written if WDCON contains the value 5AH. A successful write operation to T3 will clear the prescaler and WDCON, leaving the watchdog enabled and preventing inadvertent changes of T3. To prevent an overflow of the watchdog timer, the user program has to reload the watchdog timer within periods that are shorter than the programmed watchdog timer internal. This time interval is determined by an 8-bit value that has to be loaded in register T3 while at the same time the prescaler is cleared by hardware.

Watchdog timer interval =

$$\frac{[256 - (T3)] \times 2048}{\text{on} - \text{chip oscillator frequency}}$$

BIT-LEVEL I^{2}C INTERFACE

This bit-level serial I/O interface supports the I^{2}C-bus. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I^{2}C specification concerning the input levels and output drive capability. Consequently, these pins have an open drain output configuration. All the four modes of the I^{2}C-bus are supported:

- master transmitter
- master receiver
- slave transmitter
- slave receiver

The advantages of the bit-level I^{2}C hardware compared with a full software I^{2}C implementation are:

- the hardware can generate the SCL pulse
- Testing a single bit (RBF respectively, WBF) is sufficient as a check for error free transmission.

The bit-level I^{2}C hardware operates on serial bit level and performs the following functions:

- filtering the incoming serial data and clock signals
- recognizing the START condition
- generating a serial interrupt request SI after reception of a START condition and the first falling edge of the serial clock
- recognizing the STOP condition
- recognizing a serial clock pulse on the SCL line
- latching a serial bit on the SDA line (SDI)
- stretching the SCL LOW period of the serial clock to suspend the transfer of the next serial data bit

- setting Read Bit Finished (RBF) when the SCL clock pulse has finished and Write Bit Finished (WBF) if there is no arbitration loss detected (i.e., SDA = 0 while SDO = 1)
- setting a serial clock Low-to-High detected (CLH) flag
- setting a Bus Busy (BB) flag on a START condition and clearing this flag on a STOP condition
- releasing the SCL line and clearing the CLH, RBF and WBF flags to resume transfer of the next serial data bit
- generating an automatic clock if the single bit data register S1BIT is used in master mode.

The following functions must be done in software:

- handling the I^{2}C START interrupts
- converting serial to parallel data when receiving
- converting parallel to serial data when transmitting
- comparing the received slave address with its own
- interpreting the acknowledge information
- guarding the I^{2}C status if RBF or WBF = 0.

Additionally, if acting as master:

- generating START and STOP conditions
- handling bus arbitration
- generating serial clock pulses if S1BIT is not used.

Three SFRs control the bit-level I^{2}C interface: S1INT, S1BIT and S1SCS.

INTERRUPT SYSTEM

The interrupt structure of the 8XC528 is the same as that used in the 80C51, but includes two additional interrupt sources: one for the third timer/counter, T2, and one for the I^{2}C interface. The interrupt enable and interrupt priority registers are IE and IP.

IE: Interrupt Enable Register

This register is located at address A8H. Refer to Table 3.

IE SFR (A8H)

7	6	5	4	3	2	1	0
EA	ES1	ET2	ES	ET1	EX1	ET0	EX0

IP: Interrupt Priority Register

This register is located at address B8H. Refer to Table 4.

IP SFR (B8H)

7	6	5	4	3	2	1	0
–	PS1	PT2	PS	PT1	PX1	PT0	PX0

The interrupt vector locations and the interrupt priorities are:

Source		**Priority within Level**
Vector	Address	
0003H	IE0	Highest
002BH	TF2+EXF2	
0053H	SI (I^{2}C)	
000BH	TF0	
0013H	IE1	
001BH	TF1	
0023H	R1+T1	Lowest

Table 3. Description of IE Bits

MNEMONIC	BIT	FUNCTION
EA	IE.7	General enable/disable control: 0 = **NO** interrupt is enabled. 1 = **ANY** individually enabled interrupt will be accepted.
ES1	IE.6	Enable **bit-level I$_2$C I/O** interrupt
ET2	IE.5	Enable **Timer 2** interrupt
ES	IE.4	Enable **Serial Port** interrupt
ET1	IE.3	Enable **Timer 1** interrupt
EX1	IE.2	Enable **External** interrupt 1
ET0	IE.1	Enable **Timer 0** interrupt
EX0	IE.0	Enable **External** interrupt 0

Table 4. Description of IP Bits

MNEMONIC	BIT	FUNCTION
–	IP.7	**Reserved.**
PS1	IP.6	**Bit-level I^{2}C** interrupt priority level
PT2	IP.5	**Timer 2** interrupt priority level
PS	IP.4	**Serial Port** interrupt priority level
PT1	IP.3	**Timer 1** interrupt priority level
PX1	IP.2	**External Interrupt 1** priority level
PT0	IP.1	**Timer 0** interrupt priority level
PX0	IP.0	**External Interrupt 0** priority level

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. The power-down mode can be terminated by a RESET in the same way as in the 80C51 or in addition by one of two external interrupts, INT0 or INT1. A termination with an external interrupt does not affect the internal data memory and does not affect the special function registers. This makes it possible to exit power-down without changing the port output levels. To terminate the power-down mode with an external interrupt $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ must be switched to level-sensitive and must be enabled. The external interrupt input signal $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ must be kept low until the oscillator has restarted and stabilized. An instruction following the instruction that puts the device in the power-down mode will be executed. A reset generated by the watchdog timer terminates the power-down mode in the same way as an external RESET, and only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory.

Table 5 shows the state of I/O ports during low current operating modes.

Table 5. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70, or –40 to +85, or –40 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to V_{DD} +0.5	V
Input, output current on any two pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C (V_{DD} = 5V ±20%), –40°C to +85°C (V_{DD} = 5V ±20%), or –40°C to +125°C (V_{DD} = 5V ±10%), V_{SS}=0V

			TEST	LIMITS		
SYMBOL	PARAMETER	PART TYPE	CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6/SCL, P1.7/SDA	0°C to 70°C –40°C to +85°C –40°C to +125°C		–0.5 –0.5 –0.5	0.2V_{DD}–0.1 0.2V_{DD}–0.15 0.2V_{DD}–0.25	V V V
V_{IL1}	Input low voltage to $\overline{EA}$	0°C to 70°C –40°C to +85°C –40°C to +125°C		–0.5 –0.5 –0.5	0.2V_{DD}–0.3 0.2V_{DD}–0.35 0.2V_{DD}–0.45	V V V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[3]			–0.5	0.3V_{DD}	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA	0°C to 70°C –40°C to +85°C –40°C to +125°C		0.2V_{DD}+0.9 0.2V_{DD}+1.0 0.2V_{DD}+1.0	V_{DD}+0.5 V_{DD}+0.5 V_{DD}+0.5	V V V
V_{IH1}	Input high voltage, XTAL1, RST	0°C to 70°C –40°C to +85°C –40°C to +125°C		0.7V_{DD} 0.7V_{DD}+0.1 0.7V_{DD}+0.1	V_{DD}+0.5 V_{DD}+0.5 V_{DD}+0.5	V V V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[3]			0.7V_{DD}	6.0	V
V_{OL}	Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA[1]		I_{OL} = 1.6mA[4]		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[1]		I_{OL} = 3.2mA[4]		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA		I_{OL} = 3.0mA[4]		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3		V_{DD} = 5V ±10%, I_{OH} = –60µA I_{OH} = –25µA I_{OH} = –10µA	2.4 0.75V_{DD} 0.9V_{DD}		V V V
V_{OH1}	Output high voltage, Port 0 in external bus mode, ALE, $\overline{PSEN}$, RST[2]		V_{DD} = 5V ±10%, I_{OH} = –800µA I_{OH} = –300µA I_{OH} = –80µA	2.4 0.75V_{DD} 0.9V_{DD}		V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	0°C to 70°C –40°C to +85°C –40°C to +125°C	V_{IN} = 0.45V		–50 –75 –75	µA µA µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	0°C to 70°C –40°C to +85°C –40°C to +125°C	See note 5		–650 –750 –750	µA µA µA

DC ELECTRICAL CHARACTERISTICS (Continued)

T_{amb} = 0°C to +70°C (V_{DD} = 5V ±20%), –40°C to +85°C (V_{DD} = 5V ±20%), or –40°C to +125°C (V_{DD} = 5V ±10%), V_{SS}=0V

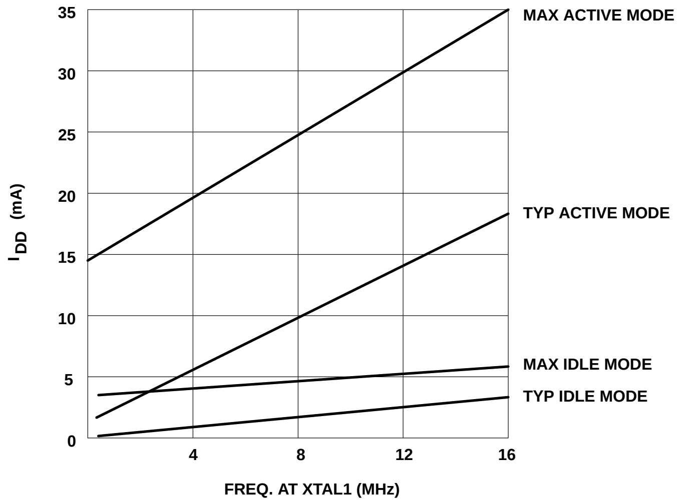
SYMBOL	PARAMETER	PART TYPE	TEST CONDITIONS	LIMITS		UNIT
				MIN	MAX	
I_{IL1}	Input leakage current, port 0, $\overline{EA}$		0.45<Vi<V_{DD}		±10	µA
I_{IL2}	Input leakage current, P1.6/SCL, P1.7/SDA		0V<Vi<6.0V 0V<V_{DD}<6.0V		±10	µA µA
I_{DD}	Power supply current:		See notes 6, 7			
	Active mode				35	mA
	Idle mode				6	mA
	Power down mode				100	µA
	Power down mode	–40°C to +125°C			150	µA
R_{RST}	Internal reset pull-down resistor			50	150	kΩ
C_{IO}	Capacitance of I/O buffer		Freq.=1MHz T_{amb} = 25°C		10	pF

NOTES:

1. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level ouput voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
3. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so a voltage below $0.3V_{DD}$ will be recognized as a logic 0 while an input above $0.7V_{DD}$ will be recognized as a logic 1.
4. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8–bit port: –
   Port 0: 26mA
   Ports 1, 2, & 3: 15mA
   Maximum total I_{OL} for all output pins: 71mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
5. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
6. See Figures 9 through 12 for I_{DD} test conditions.
7. I_{DDMAX} at other frequencies can be derived from the figure below, where FREQ is the external oscillator frequency in MHz. I_{DDMAX} is given in mA.



VALID ONLY WITHIN FREQUENCY SPECIFICATIONS OF DEVICE UNDER TEST.

I_{DD} vs. FREQUENCY

AC ELECTRICAL CHARACTERISTICS[1, 2]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency			1.2	16	MHz
t_{LHLL}	1	ALE pulse width	85		$2t_{CLCL}–40$		ns
t_{AVLL}	1	Address valid to ALE low	8		$t_{CLCL}–55$		ns
t_{LLAX}	1	Address hold after ALE low	28		$t_{CLCL}–35$		ns
t_{LLIV}	1	ALE low to valid instruction in		150		$4t_{CLCL}–100$	ns
t_{LLPL}	1	ALE low to $\overline{\text{PSEN}}$ low	23		$t_{CLCL}–40$		ns
t_{PLPH}	1	$\overline{\text{PSEN}}$ pulse width	143		$3t_{CLCL}–45$		ns
t_{PLIV}	1	$\overline{\text{PSEN}}$ low to valid instruction in		83		$3t_{CLCL}–105$	ns
t_{PXIX}	1	Input instruction hold after $\overline{\text{PSEN}}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{\text{PSEN}}$		38		$t_{CLCL}–25$	ns
t_{AVIV}	1	Address to valid instruction in		208		$5t_{CLCL}–105$	ns
t_{PLAZ}	1	$\overline{\text{PSEN}}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{\text{RD}}$ pulse width	275		$6t_{CLCL}–100$		ns
t_{WLWH}	2, 3	$\overline{\text{WR}}$ pulse width	275		$6t_{CLCL}–100$		ns
t_{RLDV}	2, 3	$\overline{\text{RD}}$ low to valid data in		148		$5t_{CLCL}–165$	ns
t_{RHDX}	2, 3	Data hold after $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{\text{RD}}$		55		$2t_{CLCL}–70$	ns
t_{LLDV}	2, 3	ALE low to valid data in		350		$8t_{CLCL}–150$	ns
t_{AVDV}	2, 3	Address to valid data in		398		$9t_{CLCL}–165$	ns
t_{LLWL}	2, 3	ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	138	238	$3t_{CLCL}–50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low	120		$4t_{CLCL}–130$		ns
t_{QVWX}	2, 3	Data valid to $\overline{\text{WR}}$ transition	3		$t_{CLCL}–60$		ns
t_{WHQX}	2, 3	Data hold after $\overline{\text{WR}}$	13		$t_{CLCL}–50$		ns
t_{RLAZ}	2, 3	$\overline{\text{RD}}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high	23	103	$t_{CLCL}–40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	6	High time	20		20		ns
t_{CLCX}	6	Low time	20		20		ns
t_{CLCH}	6	Rise time		20		20	ns
t_{CHCL}	6	Fall time		20		20	ns
Shift Register							
t_{XLXL}	4	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	4	Output data setup to clock rising edge	492		$10t_{CLCL}–133$		ns
t_{XHQX}	4	Output data hold after clock rising edge	8		$2t_{CLCL}–117$		ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	4	Clock rising edge to input data valid		492		$10t_{CLCL}–133$	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{\text{PSEN}}$ = 100pF, load capacitance for all other outputs = 80pF.

AC ELECTRICAL CHARACTERISTICS – I^{2}C INTERFACE

SYMBOL	PARAMETER	INPUT	OUTPUT	I^{2}C SPECIFICATION
SCL TIMING CHARACTERISTICS				
$t_{HD;STA}$	START condition hold time	$\geq 14\ t_{CLCL}$[1]	Note 2	$\geq 4.0\mu s$
t_{LOW}	SCL LOW time	$\geq 16\ t_{CLCL}$	Note 2	$\geq 4.7\mu s$
t_{HIGH}	SCL HIGH time	$\geq 14\ t_{CLCL}$[1]	$\geq 80\ t_{CLCL}$[3]	$\geq 4.0\mu s$
t_{RC}	SCL rise time	$\leq 1\mu s$[4]	Note 5	$\leq 1.0\mu s$
t_{FC}	SCL fall time	$\leq 0.3\mu s$[4]	$\leq 0.3\mu s$ [6]	$\leq 0.3\mu s$
SDA TIMING CHARACTERISTICS				
$t_{SU;DAT1}$	Data set-up time	$\geq 250ns$	Note 2	$\geq 250ns$
$t_{HD;DAT}$	Data hold time	$\geq 0ns$	Note 2	$\geq 0ns$
$t_{SU;STA}$	Repeated START set-up time	$\geq 14\ t_{CLCL}$[1]	Note 2	$\geq 4.7\mu s$
$t_{SU;STO}$	STOP condition set-up time	$\geq 14\ t_{CLCL}$[1]	Note 2	$\geq 4.0\mu s$
t_{BUF}	Bus free time	$\geq 14\ t_{CLCL}$[1]	Note 2	$\geq 4.7\mu s$
t_{RD}	SDA rise time	$\leq 1\mu s$[4]	Note 5	$\leq 1.0\mu s$
t_{FD}	SDA fall time	$\leq 0.3\mu s$[4]	$\leq 0.3\mu s$ [6]	$\leq 0.3\mu s$

NOTES:

1. At f_{CLK} = 3.5MHz, this evaluates to 14 × 286ns = 4µs, i.e., the bit-level I^{2}C interface can respond to the I^{2}C protocol for $f_{CLK} \geq 3.5MHz$.
2. This parameter is determined by the user software, it has to comply with the I^{2}C.
3. This value gives the autoclock pulse length which meets the I^{2}C specification for the specified XTAL clock frequency range. Alternatively, the SCL pulse may be timed by software.
4. Spikes on SDA and SCL lines with a duration of less than $4 \times f_{CLK}$ will be filtered out.
5. The rise time is determined by the external bus line capacitance and pull-up resistor, it must be ≤ 1µs.
6. The maximum capacitance on bus lines SDA and SCL is 400pF.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always ‘t’ (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t – Time
V – Valid
W – $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

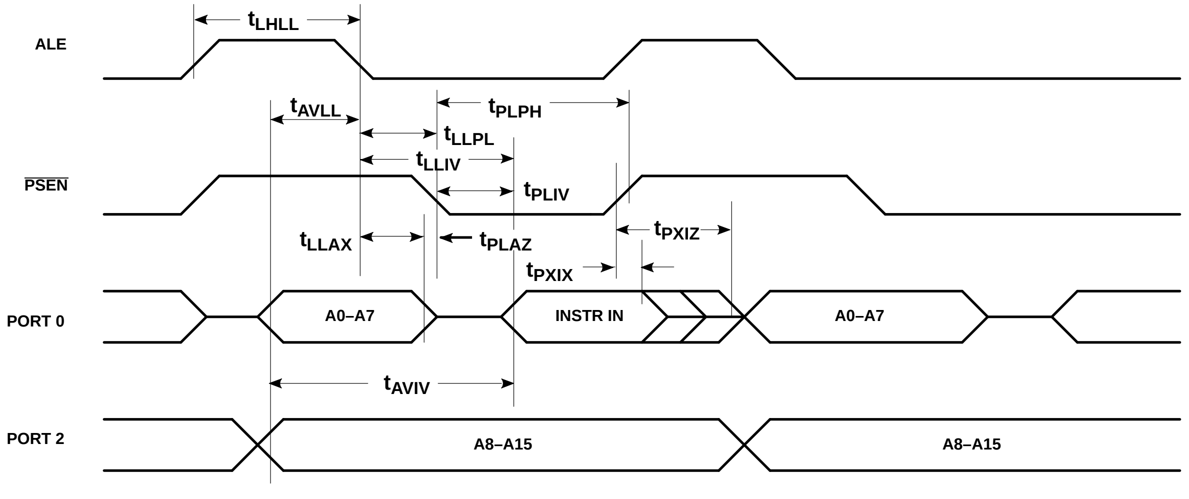


Figure 1. External Program Memory Read Cycle

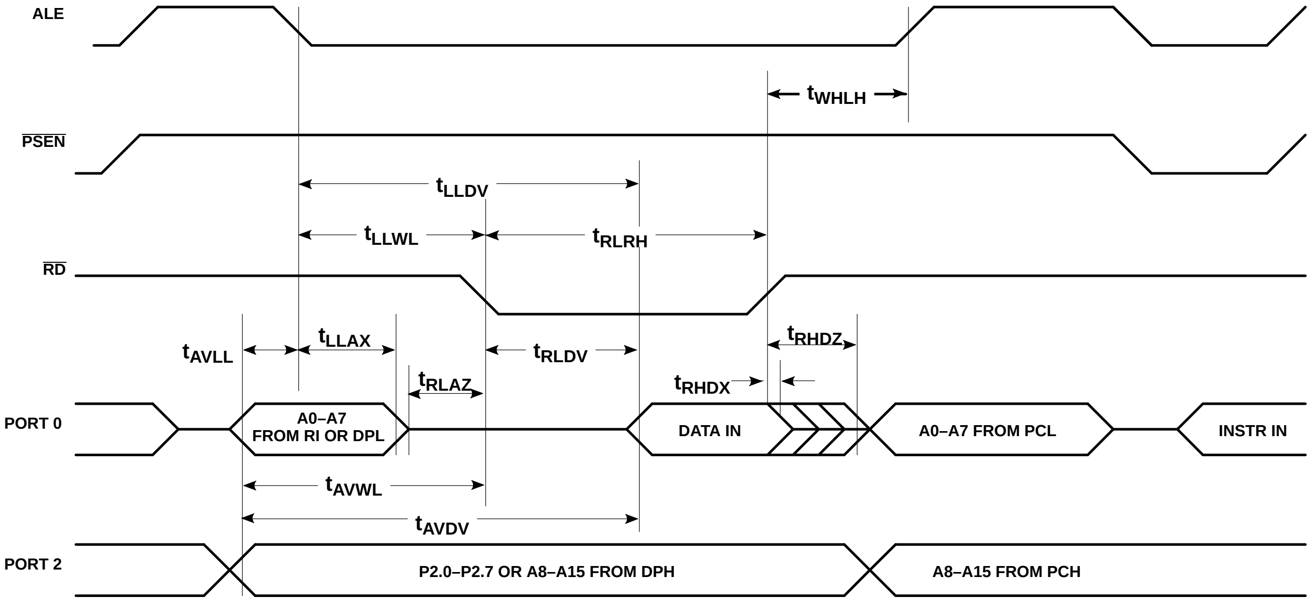


Figure 2. External Data Memory Read Cycle

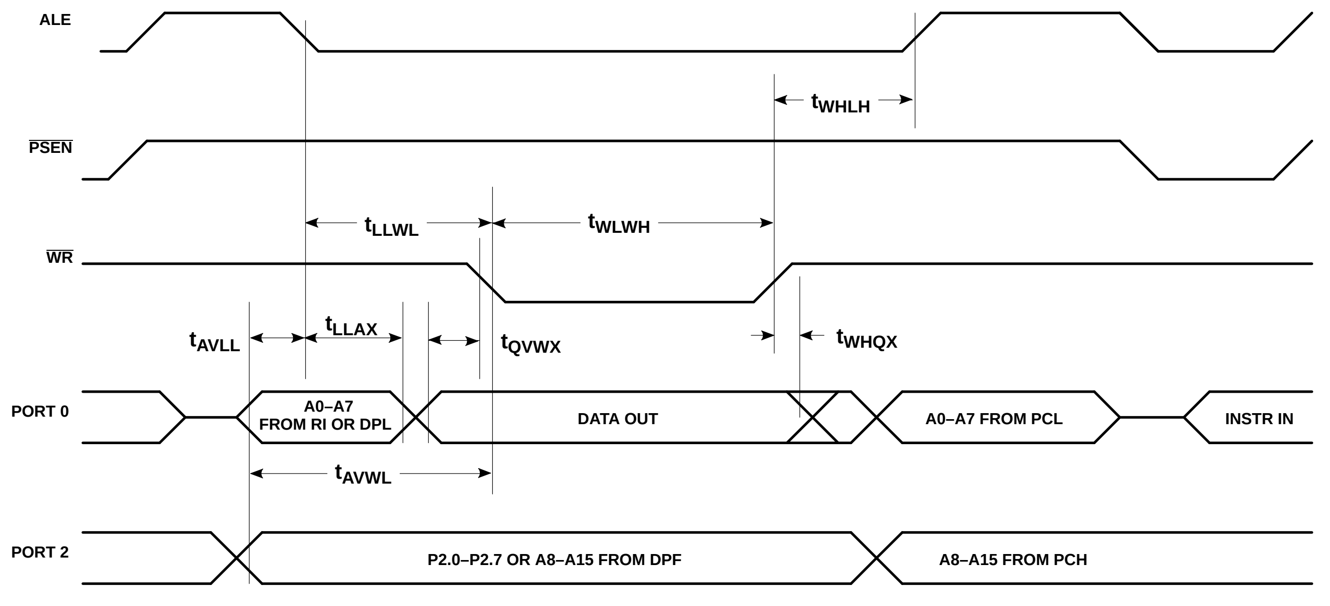


Figure 3. External Data Memory Write Cycle

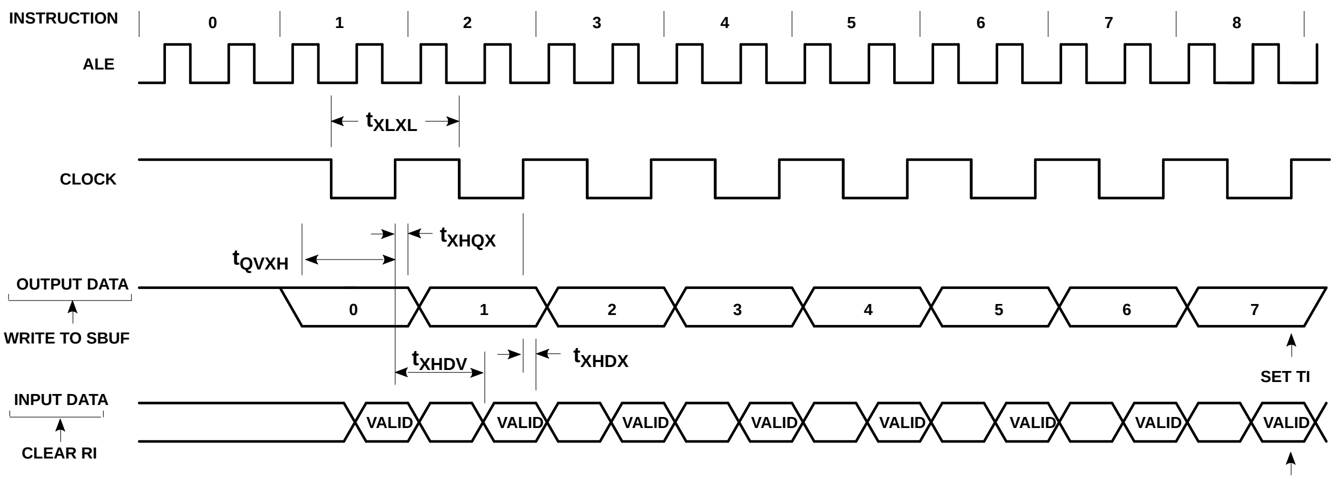


Figure 4. Shift Register Mode Timing

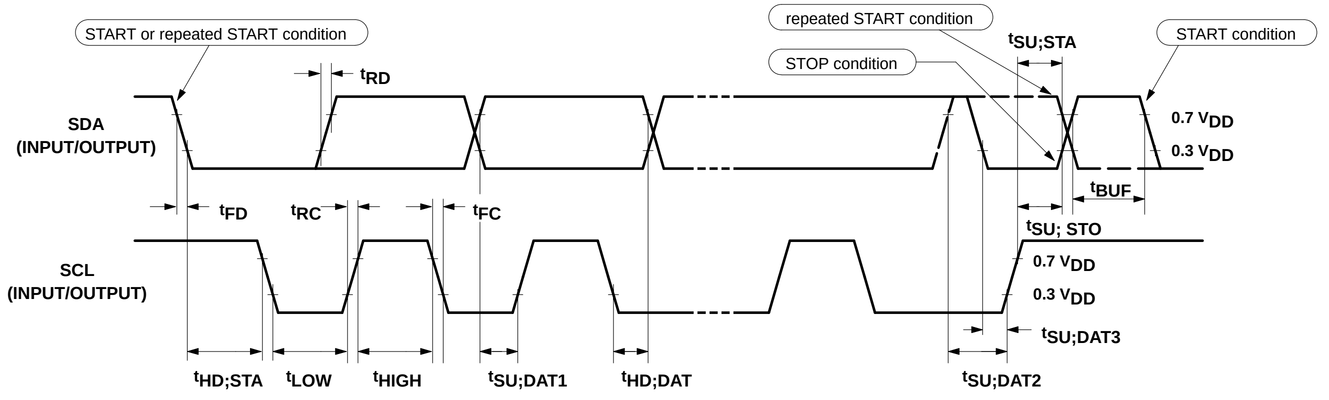


Figure 5. Timing SIO1 (I^2C) Interface

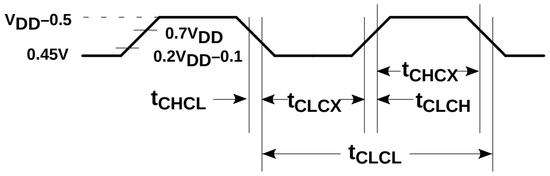
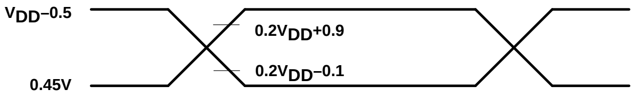
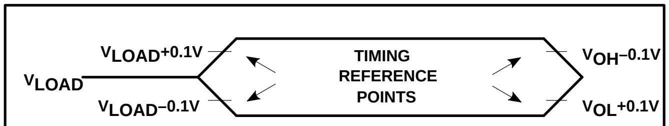


Figure 6. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{DD} –0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} for a logic '0'.

Figure 7. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

Figure 8. Float Waveform

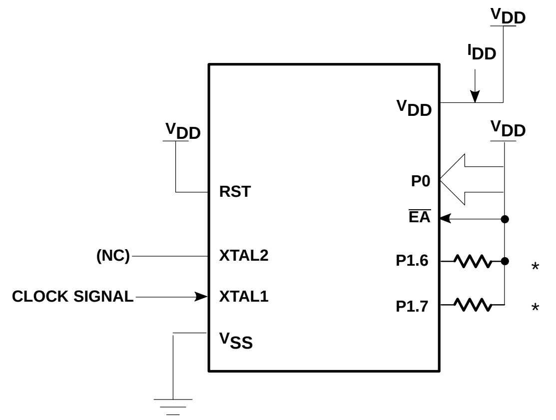


Figure 9. I_{DD} **Test Condition, Active Mode**
All other pins are disconnected

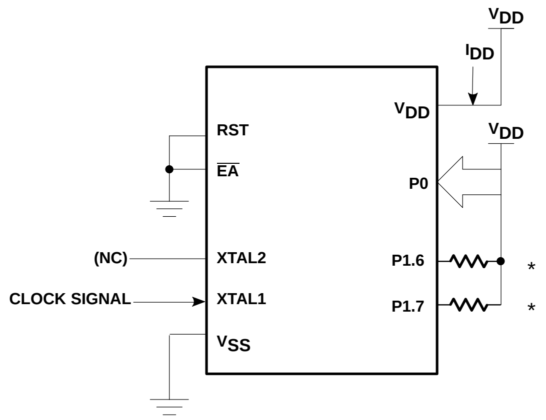


Figure 10. I_{DD} **Test Condition, Idle Mode**
All other pins are disconnected

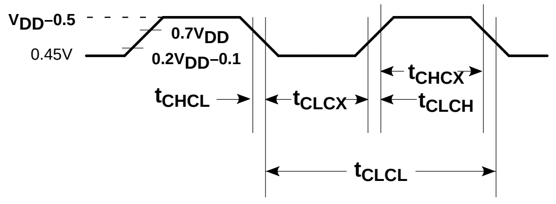


Figure 11. Clock Signal Waveform for
I_{DD} **Tests in Active and Idle Modes**
$t_{CLCH} = t_{CHCL} = 5ns$

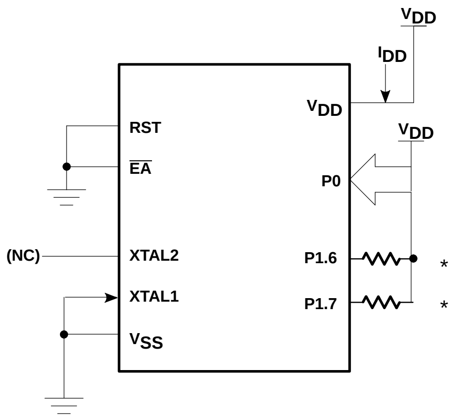


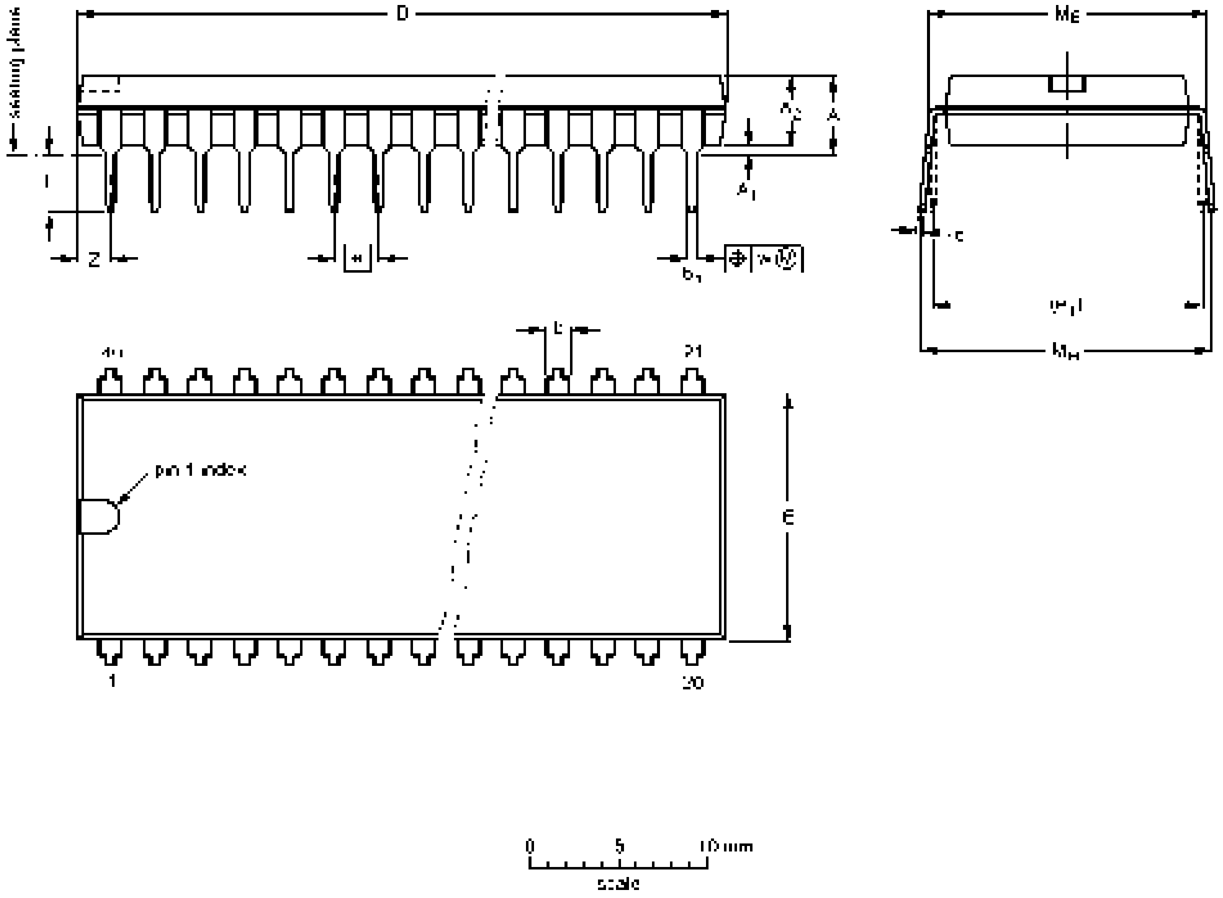
Figure 12. I_{DD} **Test Condition, Power Down Mode**
All other pins are disconnected. V_{DD} **= 2V to 5.5V**

NOTE:

* Ports 1.6 and 1.6 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specifications.

Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

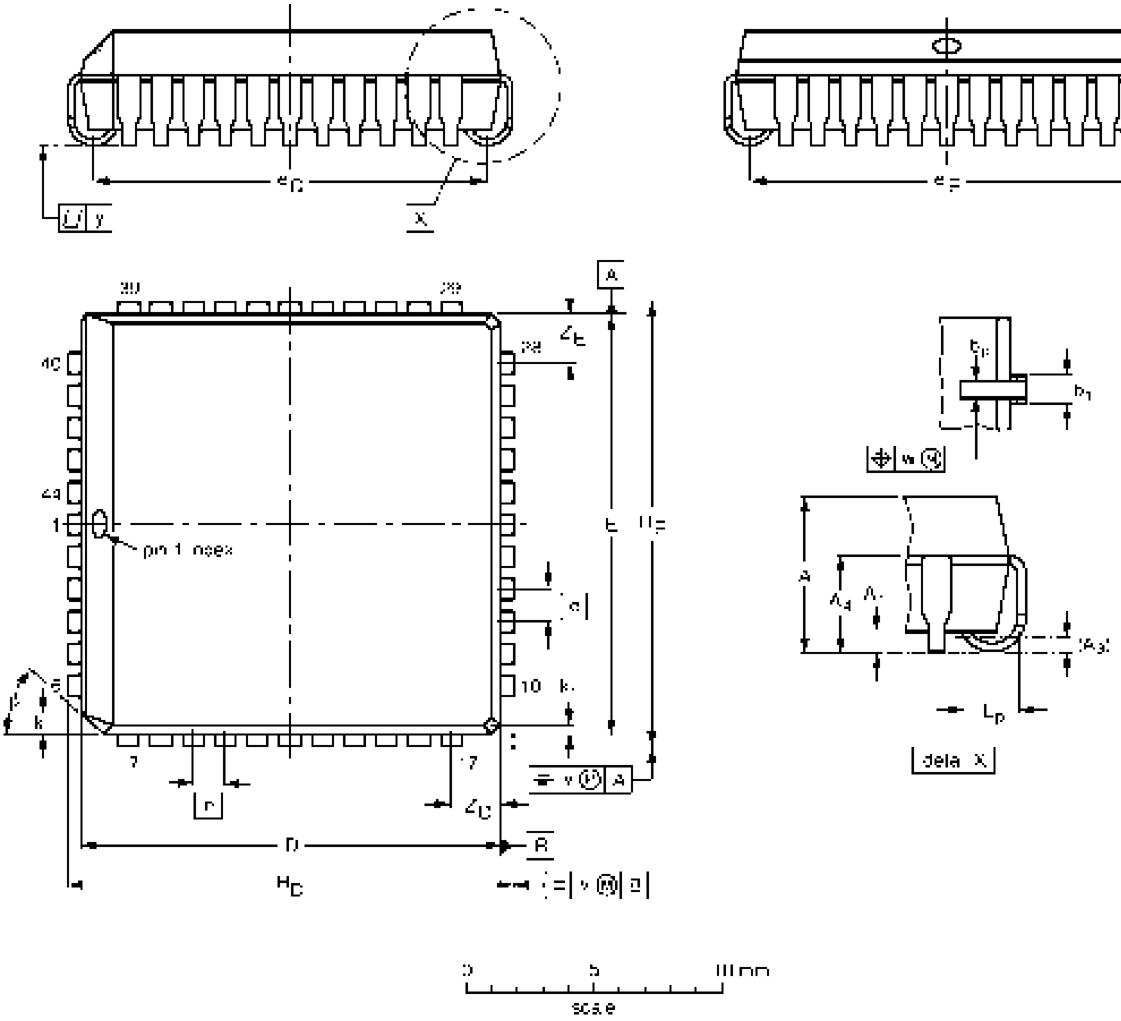
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

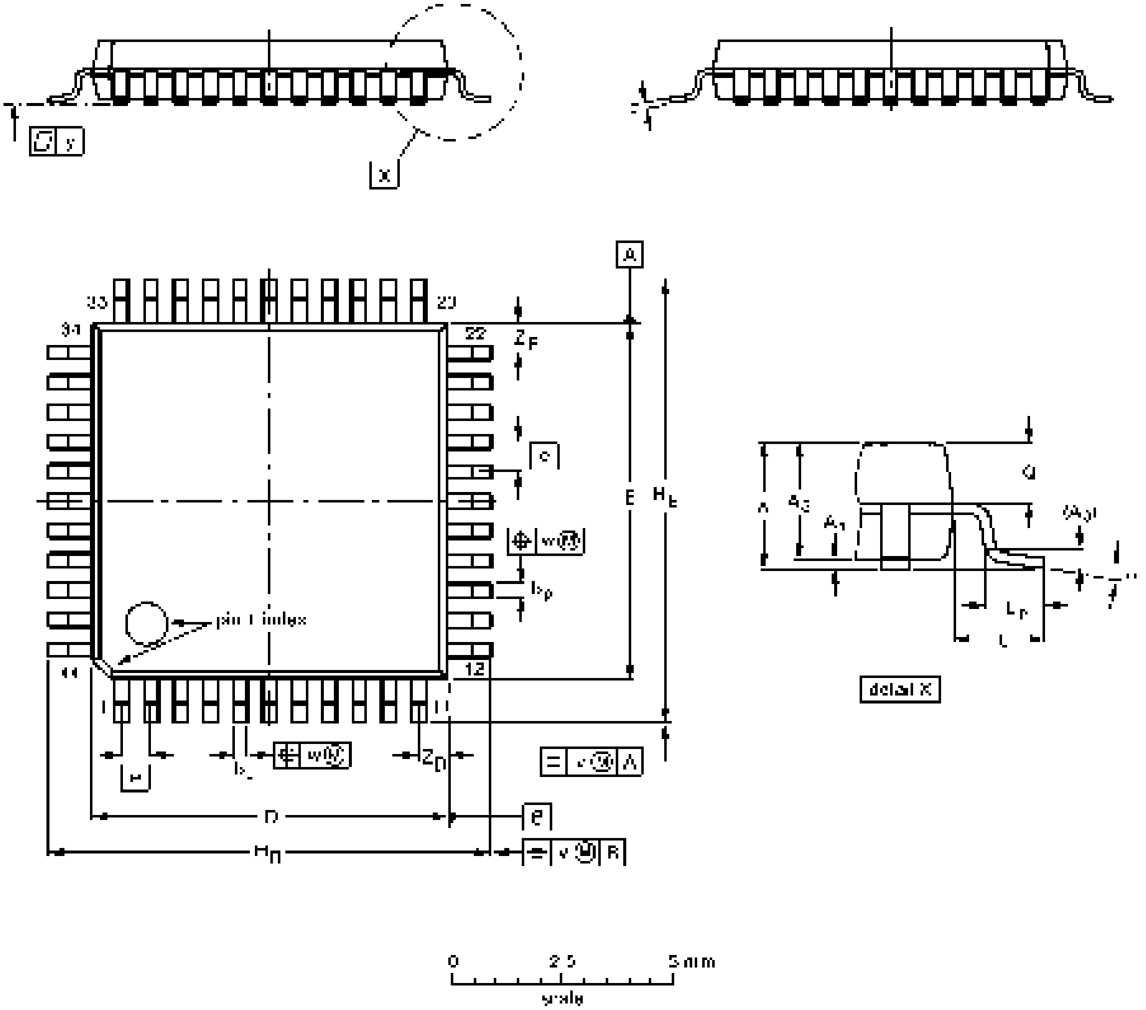
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.046 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC			⊏⊐ ◎	92-11-17 95-02-25

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

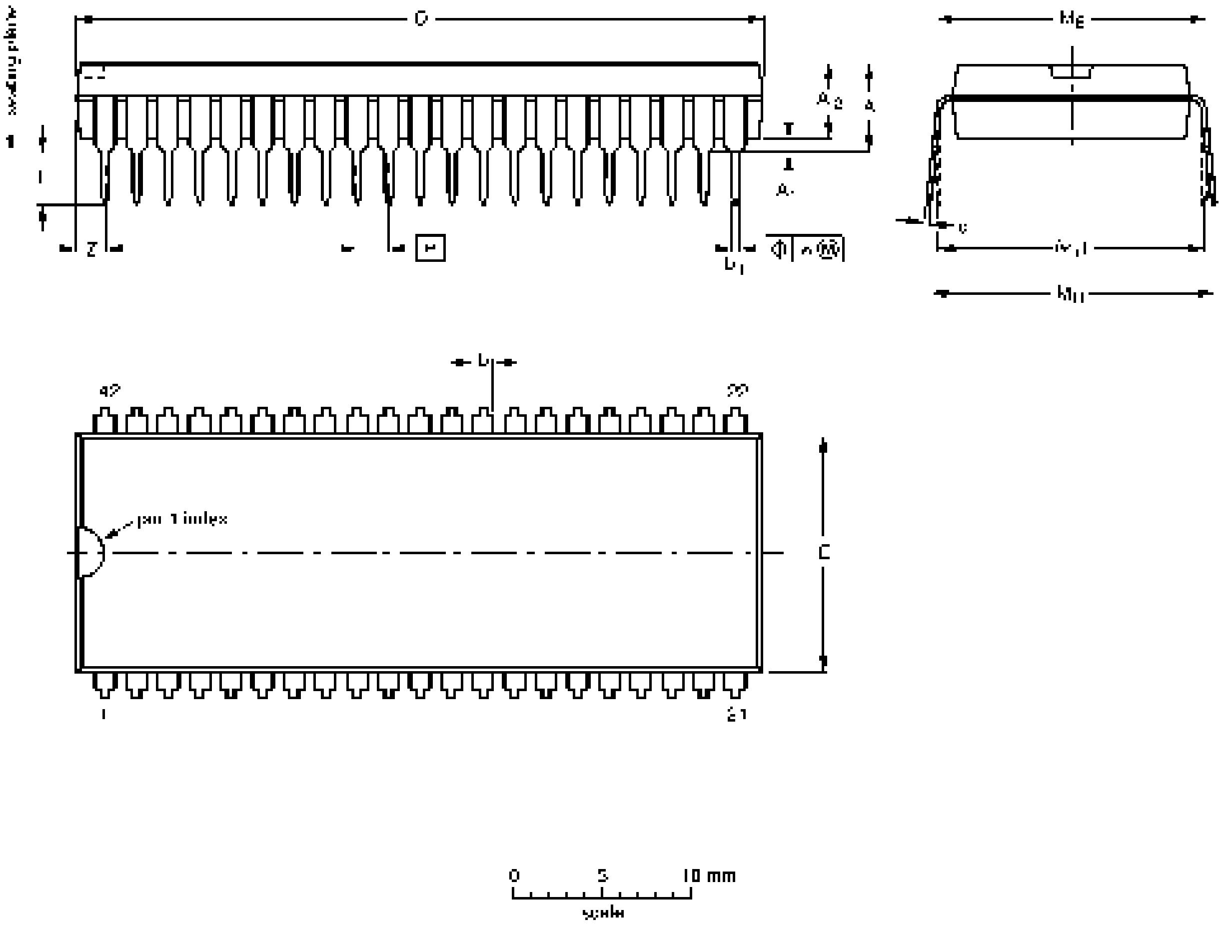
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.9	1.2 0.9	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT307-2					92-11-17 95-02-04

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) SOT270-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

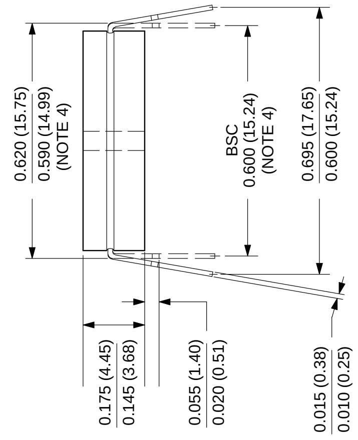
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

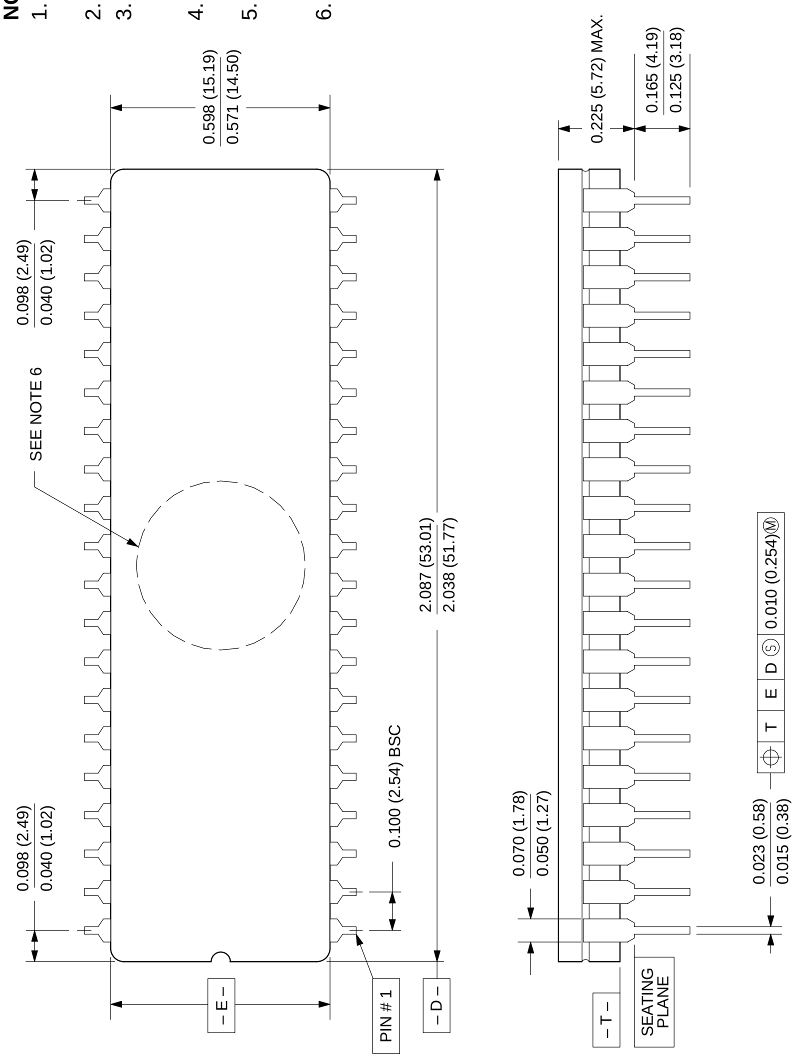
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT270-1				⌖	90-02-13 95-02-04

0590B 40-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)

NOTES:

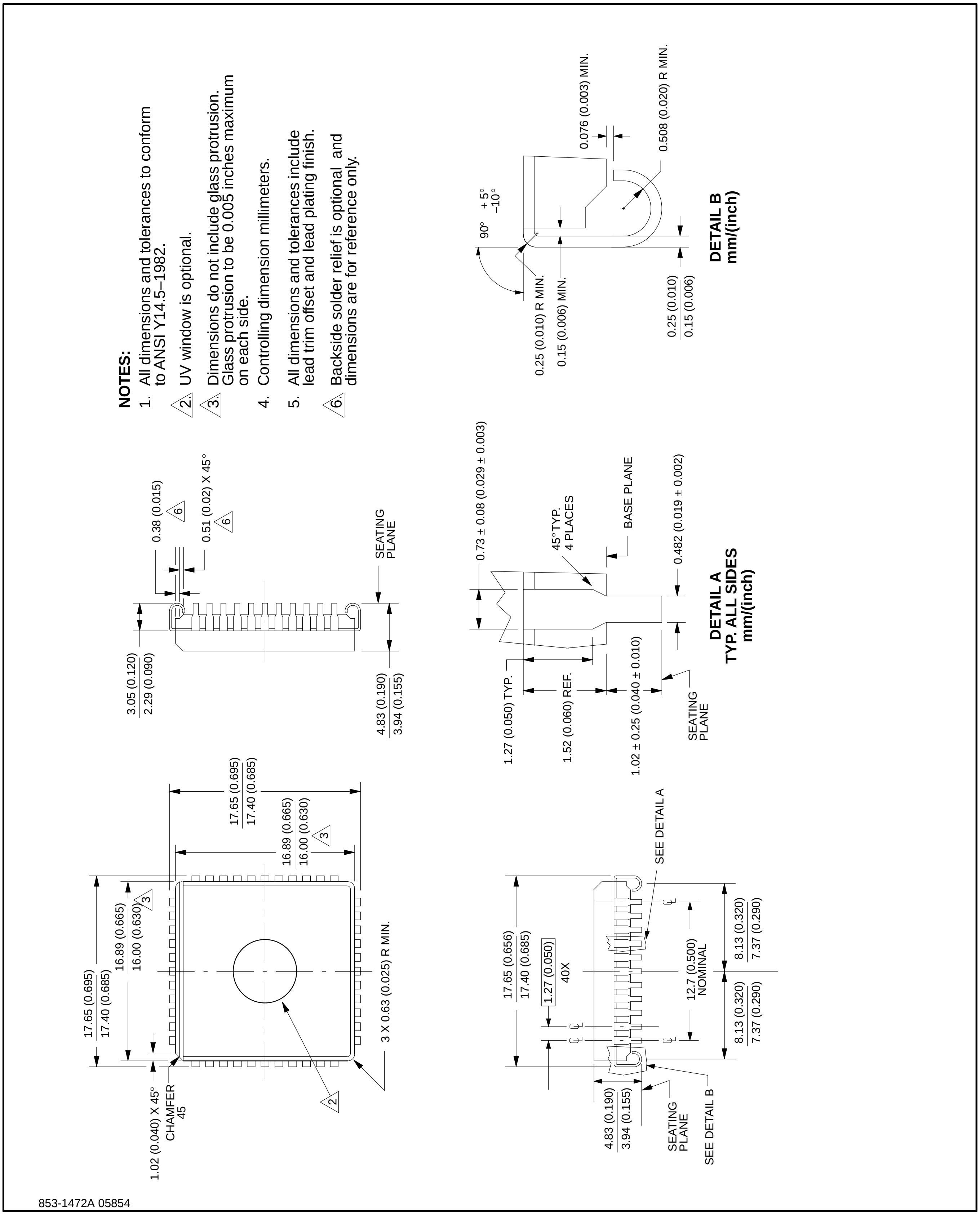
1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. “T”, “D”, and “E” are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #40 when viewed from the top.
6. Denotes window location for EPROM products.





853–0590B 06688

1472A 44-PIN CERQUAD J-BEND (K) PACKAGE



NOTES:

1. All dimensions and tolerances to conform to ANSI Y14.5–1982.
2. UV window is optional.
3. Dimensions do not include glass protrusion. Glass protrusion to be 0.005 inches maximum on each side.
4. Controlling dimension millimeters.
5. All dimensions and tolerances include lead trim offset and lead plating finish.
6. Backside solder relief is optional and dimensions are for reference only.

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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