



8470 TRIPLE 3-INPUT NAND GATE 8480 QUAD 2-INPUT NAND GATE 8490 HEX INVERTER

The 8470 Triple 3-Input NAND Gate and the 8480 Quad 2-Input NAND Gate implement the NAND function for positive logic (highest voltage level = "1") and the NOR function for negative logic (lowest voltage level = "1").

The 8490 Hex Inverter is an addition to the 8470/8480 group of NAND gates.

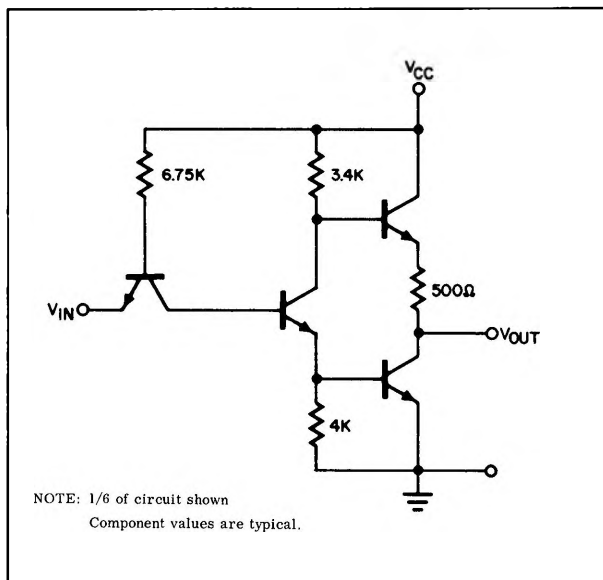
The active output structure of these elements provides high AC noise immunity due to its low output impedance in both the "1" and "0" output states. This output configuration is particularly suited for driving high capacitive loads such as those encountered in high fan-out situations and line driving applications.

Output short circuit protection is provided by a current limiting resistor.

The values chosen for the collector and emitter resistors of the phase-splitter transistor ensure optimum on-off relationships of the totem-pole output pair.

Section 4 of this handbook contains helpful usage rules and applications for the 8470 and 8480.

BASIC CIRCUIT SCHEMATIC



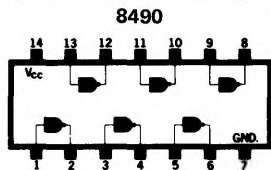
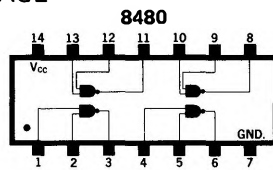
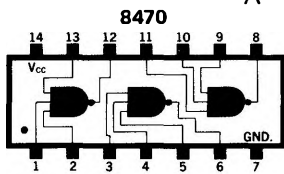
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 12)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8470 S8480	TEMP. N8470 N8480	V _{CC}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	3.4			V	-55°C	0°C	4.75V	0.7V		-225μA	8
A-3		3.6			V	+25°C	+25°C	5.0V	0.7V		-225μA	8
A-4		3.4			V	+125°C	+75°C	4.75V	0.7V		-225μA	8
A-5	"0" OUTPUT VOLTAGE			0.35	V	-55°C	0°C	4.75V	2.0V	2.0V	7.2mA	9
A-3				0.35	V	+25°C	+25°C	5.0V	2.0V	2.0V	7.2mA	9
A-4				0.35	V	+125°C	+75°C	4.75V	2.0V	2.0V	7.2mA	9
C-1	"0" INPUT CURRENT	-0.1		-0.8	mA	-55°C	0°C	5.25	0.35V	5.25V		
A-3		-0.1		-0.8	mA	+25°C	+25°C	5.25V	0.35V	5.25V		
C-1		-0.1		-0.8	mA	+125°C	+75°C	5.25V	0.35V	5.25V		
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		
A-6	PAIR DELAY	25		95	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	OUTPUT FALL TIME			75	ns	-55°C	0°C	4.75V			A.C.F.O. = 2	11, 13
C-2	TURN-ON DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 9	10, 13
C-2	TURN-OFF DELAY			40	ns	+25°C	+25°C	5.0V			D.C.F.O. = 1	10, 13
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			16.8	mW	+25°C	+25°C	5.25V				
	(Per Gate) OUTPUT "1"			5.2	mW	+25°C	+25°C	5.25V	0V			
A-2	INPUT VOLTAGE RATING	5.5			V	+25°C	+25°C	5.0V	50μA	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT	-4.0		-12.0	mA	+25°C	+25°C	5.0V	0V		0V	

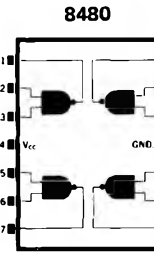
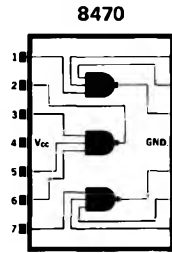
NOTES:

- All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current flow is defined as into the terminal referenced.
- Positive NAND Logic Definition: "UP" Level = "1", "DOWN" Level = "0".
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
- Measurements apply to each gate element independently.
- Capacitance as measured on Bonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. $f = 1\text{MHz}$, $V_{AC} = 25\text{mV}_{RMS}$. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- One DC fan-out is defined as 0.8mA.
- One AC fan-out is defined as 50pf.
- Manufacturer reserves the right to make design and process changes and improvements.
- Detailed test conditions for AC testing are in Section 3.

A PACKAGE



J PACKAGE



8470
8480
8490

