87C196KT Advanced 16-BIT CHMOS Microcontroller

Automotive

Production Datasheet

Product Features

- Powerdown and Idle Modes
- –40°C to +125°C Ambient
- High Performance CHMOS 16-Bit CPU
- Up to 32 Kbytes of On-Chip EPROM
- Up to 1 Kbyte of On-Chip Register RAM
- Up to 512 Bytes of Additional RAM (Code RAM)
- Register-Register Architecture
- 8 Channel/10-Bit A/D with Sample/Hold
- Programmable A/D Conversion and S/H Times
- 37 Prioritized Interrupts
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port
- Dedicated Baud Rate Generator
- Synchronous/Asynchronous Serial I/O Port (with Dedicated 16-Bit Baud Rate Generator)
- Interprocessor Communication Slave Port
- Selectable Bus Timing Modes for Flexible Interfacing
- Oscillator Fail Detection Circuitry
- Total Utilization of ALL Available Pins (I/O Mux'd with Control)
- High Speed Peripheral Transaction Server (PTS)
- Two Dedicated 16-Bit High-Speed Compare Registers
- 10 High Speed Capture/Compare (EPA)
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Two Flexible 16-Bit Timer Counters
- Flexible 8-/16-Bit External Bus (Programmable)
- “Windowing” Allows 8-Bit Addressing to some 16-Bit Addresses
- Programmable Bus (HLD/HLDA)
- 1.4 µs 16 x 16 Multiply
- 2.4 µs 32/16 Divide
- 68-Pin PLCC Package
- 16 MHz Operation

Order No: 273178-001
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1.0 Introduction

The 87C196Kx devices represents the 4th generation of MCS® 96 microcontroller products implemented on Intel's advanced 1 micron process technology. These products are based on the 80C196KB device with enhancements ideal for automotive applications. The instruction set is a true super set of the 80C196KB with a few new instructions.

Additional SFR space is allocated for the EPA and can be "windowed" into the lower Register RAM area.

Table 1. Device Overview

Device	Pins/Package	EPROM	Reg RAM	Code RAM	I/O	EPA	SIO	SSIO	A/D
87C196KT	68-Pin PLCC	32 K	1 K	512b	56	10	Y	Y	8

1.1 New Instructions

XCH/XCHB	Exchange the contents of two locations, either Word or Byte is supported.
BMOVI	Interruptable Block Move Instruction, allows the user to be interrupted during long executing Block Moves.
TIJMP	Table Indirect JUMP. This instruction incorporates a way to do complex CASE level branches through one instruction. An example of such code savings: several interrupt sources and only one interrupt vector. The TIJMP instruction will sort through the sources and branch to the appropriate subcode level in one instruction. This instruction was added especially for the EPA structure, but has other code saving advantages.
EPTS/DPTS	Enable and Disable PTS Interrupts (Works like EI and DI).

1.1.1 SFR Operations

A total of 1 Kbyte of Register RAM is implemented on the 87C196KT 16 MHz device. These locations support the on-chip peripherals that the 87C196KT 16 MHz has (SFR's), as well as offering a data storage area. These locations are all 8-bit directly addressable by use of the windowing technique. Any 32-, 64- or 128- byte section can be relocated into the upper 32-, 64- or 128-byte area of the Register RAM area 080H–0FFH.

2.0 Block Diagram

The MCS 96 microcontroller family members are all high performance microcontrollers with a 16-bit CPU. The 87C196KT is composed of the high speed (16 MHz) KX macrocore as well as the following peripherals: Up to 32 Kbytes of Program EPROM, up to 1 Kbytes of Register RAM (00-3FFH including SFRs), up to 512 bytes of code RAM (16-bit addressing modes) with the ability to execute from this RAM space, an eight channel-10 Bit ±3LSB analog to digital converter with programmable S/H times with conversion times < 20 µs at 16 MHz, an asynchronous/synchronous serial I/O port (8096 compatable) with a dedicated 16-bit baud rate generator, an additional synchronous serial I/O port with full duplex master/slave transceivers, a flexible timer/counter structure with prescaler, cascading, and quadrature capabilities, 10 modularized multiplexed high speed I/O for capture and compare (called Event Processor Array) with 200 ns resolution and double buffered inputs, and a sophisticated prioritized interrupt structure with programmable Peripheral Transaction Server (PTS). The PTS has several channel modes, including single/burst block transfers from any memory location to any memory location, a PWM and PWM toggle mode to be used in conjunction with the EPA, and an A/D scan mode.

Figure 1. 87C196KT Block Diagram

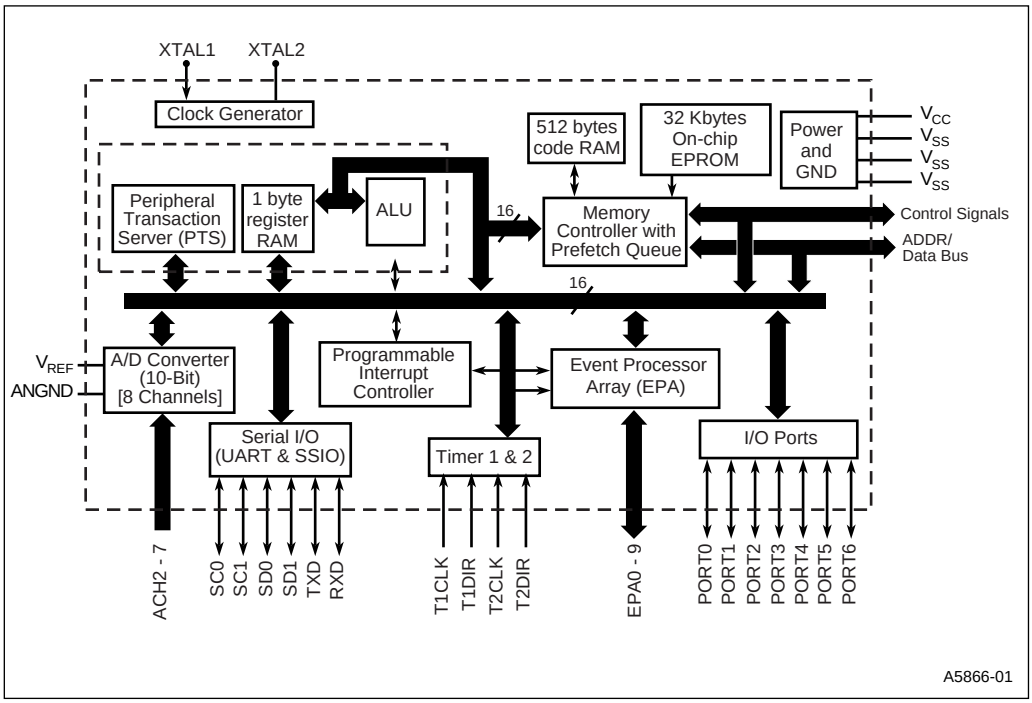
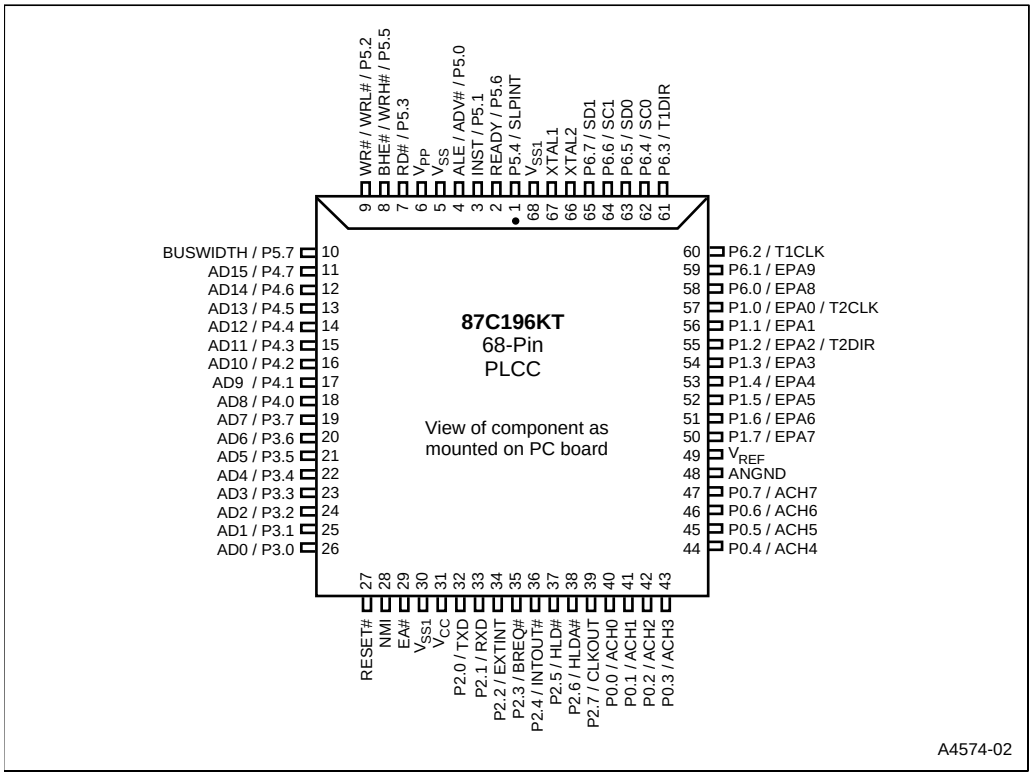


Figure 2. 68-Pin PLCC 87C196KT 16 MHz Diagram



3.0 Pin Description

Table 1. Pin Descriptions (Sheet 1 of 2)

Name	Description
V_{CC}	Main supply voltage (+5 V).
V_{SS}, V_{SS1}	Digital circuit ground (0 V). There are three V_{SS} pins, all of which MUST be connected.
V_{REF}	Reference for the A/D converter (+5 V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5 V for programming. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 µF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin.
RESET#	Reset input to the chip. Input low for at least 16 state times resets the chip. The subsequent low-to-high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, bytes are read from 2018H and 201AH loading the CCBs, and a jump to location 2080H is executed. Input high for normal operation. RESET# has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dynamically controls the Buswidth of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs, if BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is “0” and CCR1 bit 2 is “1”, all bus cycles are 8-bit, if CCR bit 1 is “1” and CCR1 bit 2 is “0”, all bus cycles are 16-bit. CCR bit 1 = “0” and CCR1 bit 2 = “0” is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH.
P5.1/INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches, during internal EPROM fetches INST is held low. Also LSIO when not INST.
EA#	Input for memory select (External Access). EA# equal to a high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip EPROM/ROM. EA# equal to a low causes accesses to these locations to be directed to off- chip memory. EA# = +12.5 V causes execution to begin in the Programming Mode. EA# latched at reset.
P5.0/ALE/ADV#	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is ADV#, it goes inactive (high) at the end of the bus cycle. ADV# can be used as a chip select for external memory. ALE/ADV# is active only during external memory accesses. Also LSIO when not used as ALE.
P5.3/RD#	Read signal output to external memory. RD# is active only during external memory reads or LSIO when not used as RD#.
P5.2/WR#/WRL#	Write and Write Low output to external memory, as selected by the CCR, WR# goes low for every external write, while WRL# goes low only for external writes where an even byte is being written. WR#/WRL# is active during external memory writes. Also an LSIO pin when not used as WR#/WRL#.

Table 1. Pin Descriptions (Sheet 2 of 2)

Name	Description
P5.5/BHE#/WRH#	Byte High Enable or Write High output, as selected by the CCR. BHE# = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, BHE# = 1), to the high byte only (A0 = 1, BHE# = 0) or both bytes (A0 = 0, BHE# = 0). If the WRH# function is selected, the pin goes low if the bus cycle is writing to an odd memory location. BHE#/WRH# is only valid during 16-bit external memory write cycle. Also an LSIO pin when not BHE#/WRH#.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual-function I/O pin. As a bidirectional port pin or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual-function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Clock input. The TIMER1 increments or decrements on both positive and negative edges of this pin.
P6.3/T1DIR	Dual-function I/O pin. Primary function is that of a bidirectional I/O pin, however, it may also be used as a TIMER1 Direction input. The TIMER1 increments when this pin is high and decrements when this pin is low.
PORT 1/EPA0–7 P6.0–6.1/EPA8–9	Dual-function I/O port pins. Primary function is that of bidirectional I/O. System function is that of High Speed capture and compare. EPA0 and EPA2 have another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH0–7	8-bit high-impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.3-6.7/SSIO	Dual-function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

Figure 3. Chip Configuration Registers

CCB (2018H : Byte)

0	PD	=	"1" Enables Powerdown
1	BW0	=	See Table
2	WR	=	"1" = WR#/BHE# - "0" = WRL#/WRH#
3	ALE	=	
4	IRC0	=	"1" = ALE - "0" = ADV#
5	IRC1	=	} See Table
6	LOC0	=	
7	LOC1	=	

CCB (201AH : Byte)

0	0	=	Reserved, must be "0"
1	IRC2	=	See Table
2	BW1	=	See Table
3	WDE	=	"0" = Always Enabled
4	1	=	} Reserved, must be "01"
5	0	=	
6	MSEL0	=	} See Table
7	MSEL1	=	

LOC1	LOC0	Function
0	0	Read and Write Protected
0	1	Write Protected Only
1	0	Read Protected Only
1	1	No Protection

IRC2	IRC1	IRC0	Max Wait States
0	0	0	Zero Wait States
1	0	0	1 Wait State
1	0	1	2 Wait States
1	1	0	3 Wait States
1	1	1	INFINITE

MSEL1	MSEL0	Bus Timing Mode
0	0	Mode 0 (1-Wait KR)
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3 (KR)

BW1	BW0	Bus Width
0	0	ILLEGAL
0	1	16-Bit Only
1	0	8-Bit Only
1	1	BW Pin Controlled

Mode 0 (1-Wait KR): Designed to be similar to the 87C196KR bus timing with 1 automatic wait state.

See AC Timings section for actual timings data.

Mode 1
RD#, WR, advanced 1 T_{OSC}
ALE advanced 0.5 T_{OSC}
ALE pulse width remains 1 T_{OSC}

Mode 2
RD#21, WR, advanced 1 T_{OSC}
ALE advanced 0.5 T_{OSC}
ALE pulse width remains 1 T_{OSC}
Address advanced 0.5 T_{OSC}

Mode 3 (KR): Designed to be similar to the 87C196KR bus timing.

See AC Timings section for actual timings data.

4.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature –60°C to +150°C

Voltage from V_{PP} or EA# to V_{SS} or ANGND..... –0.5 V to +13 V

Voltage from any other pin to V_{SS} or ANGND..... –0.5 V to +7 V
This includes V_{PP} on ROM and CPU devices.

Power Dissipation ..... 0.5 W

OPERATING CONDITIONS

T_A (Ambient Temperature Under Bias).....–40°C to +125°C

V_{CC} (Digital Supply Voltage) 4.5 V to 5.5 V

V_{REF} (Analog Supply Voltage) 4.5 V to 5.5 V

F_{OSC} (Oscillator Frequency ..... 4 MHz to 16 MHz

NOTE: ANGND and V_{SS} should be nominally at the same potential.

NOTICE: This is a production data sheet. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.1 DC Characteristics

Table 2. DC Characteristics (Under Listed Operating Conditions) (Sheet 1 of 2)

Sym	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CC}	V_{CC} Supply Current (–40°C to +125°C Ambient)			82	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF}$= 5.5 V (While Device in Reset)
I_{REF}	A/D Reference Supply Current			5	mA	
I_{IDLE}	Idle Mode Current			40	mA	XTAL1 = 16 MHz $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V
I_{PD}	Powerdown Mode Current		50		µA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V (5,8)
V_{IL}	Input Low Voltage (All Pins)	–0.5		0.3 V_{CC}	V	For PORT0 (7)
V_{IH}	Input High Voltage	0.7 V_{CC}		V_{CC} + 0.5	V	For PORT0 (7)
V_{IH1}	Input High Voltage XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	XTAL1 Input Pin Only

NOTES:
1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5 and Port6 except SLPINT (P5.4) and HLDA# (P2.6).
2. Standard Input pins include XTAL1, EA#, RESET# and Port 1/2/5/6 when setup as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC}$ = 5 V.
6. Violating these specifications in reset may cause the device to enter test mode (P5.4 and P2.6).
7. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
8. For temperatures < 100°C typical is 10 µA.
9. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

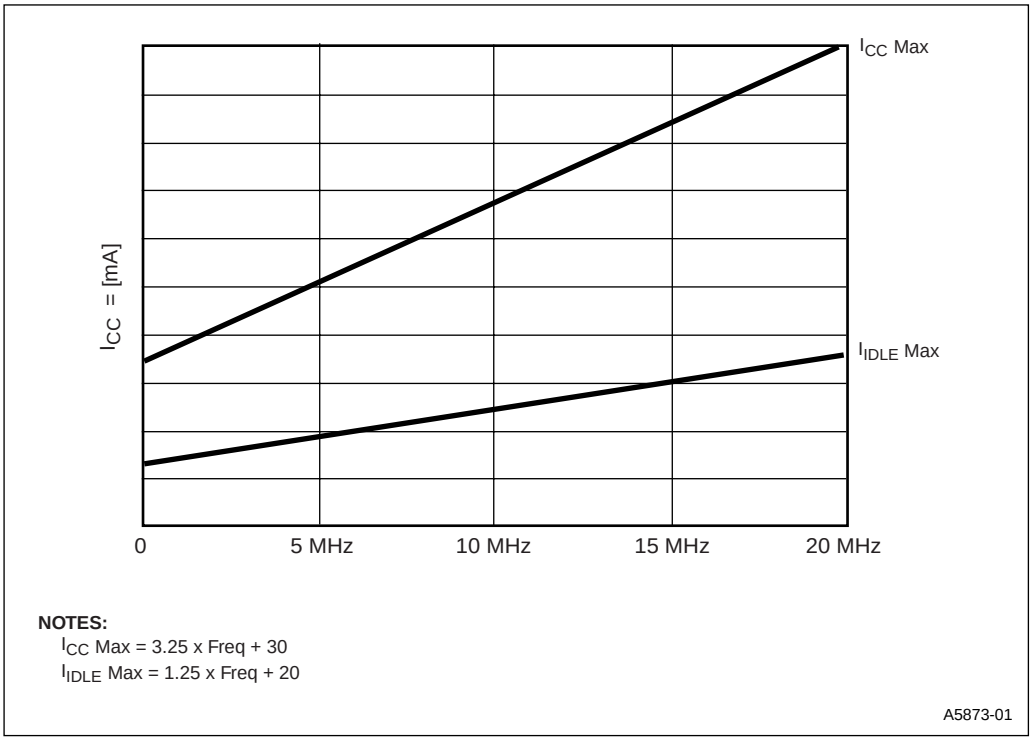
Table 2. DC Characteristics (Under Listed Operating Conditions) (Sheet 2 of 2)

Sym	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH2}	Input High Voltage on RESET#	0.7 V_{CC}		V_{CC} + 0.5	V	RESET# Input Pin Only
V_{OL}	Output Low Voltage (Outputs Configured as Complementary)			0.3 0.45 1.5	V	I_{OL} = 200 µA (3) I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage (Output Configured as Complementary)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = –200 µA (3) I_{OH} = –3.2 mA I_{OH} = –7 mA
I_{LI}	Input Leakage Current (Standard Inputs)			±10	µA	$V_{SS} < V_{IN} < V_{CC}$
I_{LI1}	Input Leakage Current (Port 0)			±1.5	µA	$V_{SS} < V_{IN} < V_{REF}$
V_{OH1}	SLPINT (P5.4) and HLDA# (P2.6) Output High Voltage in RESET#	2			V	I_{OH} = 0.8 mA (6)
V_{OH2}	Output High Voltage in RESET#	V_{CC} – 1			V	I_{OH} = –15 µA (1,7)
I_{OH2}	Output High Current in RESET#	– 30 – 75 – 90		– 120 – 240 – 280	µA	V_{OH2}= V_{CC} –1 V (9) V_{OH2}= V_{CC} –2.5 V V_{OH2}= V_{CC} –4 V
V_{OL3}	Output Low Voltage in RESET# (RESET# Pin Only)			0.3 0.5 0.8	V	I_{OL3}= 4 mA (9) I_{OL3}= 6 mA I_{OL3}= 8 mA
C_S	Pin Capacitance (Any Pin to V_{SS})		10		pF	F_{TEST} = 1 MHz (5)
R_{WPU}	Weak Pullup Resistance		150 K		Ω	(5)
R_{RST}	RESET# Pullup Resistor	65 K		180 K	Ω	

NOTES:

1. All BD (bidirectional) pins except INST and CLKOUT. INST and CLKOUT are excluded due to not being weakly pulled high in reset. BD pins include Port1, Port2, Port3, Port4, Port5 and Port6 except SLPINT (P5.4) and HLDA# (P2.6).
2. Standard Input pins include XTAL1, EA#, RESET# and Port 1/2/5/6 when setup as inputs.
3. All Bidirectional I/O pins when configured as Outputs (Push/Pull).
4. Device is Static and should operate below 1 Hz, but only tested down to 4 MHz.
5. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and V_{REF} = V_{CC} = 5 V.
6. Violating these specifications in reset may cause the device to enter test mode (P5.4 and P2.6).
7. When P0 is used as analog inputs, refer to A/D specifications for this characteristic.
8. For temperatures < 100°C typical is 10 µA.
9. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.

Figure 4. I_{CC} vs Frequency



NOTES:
I_{CC} Max = 3.25 x Freq + 30
I_{IDLE} Max = 1.25 x Freq + 20

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4.2 AC Characteristics

(Over Specified Operating Conditions)

4.2.1 Test Conditions

- Capacitive load on all pins = 100 pF
- Rise and Fall Times = 10 ns

Table 3. Specifications Met by the 87C196KT (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	4	16	MHz (1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns
T_{OFD}	Clock Failure to Reset Pulled Low	4	40	µs
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns (2)
T_{CHCL}	CLKOUT High Period	T_{OSC}–10	T_{OSC}+30	ns
T_{CLLH}	CLKOUT Low to ALE/ADV# High	–10	15	ns
T_{LLCH}	ALE/ADV# Low to CLKOUT High	–25	15	ns
T_{LHLH}	ALE/ADV# Cycle Time	4 T_{OSC}		ns (2,5)
T_{LHLL}	ALE/ADV# High Time	T_{OSC}–10	T_{OSC}+10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC}–15		ns
T_{LLAX}	Address Hold after ALE/ADV# Low	T_{OSC}–40		ns
T_{LLRL}	ALE/ADV# Low to RD# Low	T_{OSC}–40		ns
T_{RLCL}	RD# Low to CLKOUT Low	–5	35	ns
T_{RLRH}	RD# Low Period	T_{OSC}–5		ns (5)
T_{RHLH}	RD# High to ALE/ADV# High	T_{OSC}	T_{OSC}+25	ns (3)
T_{RLAZ}	RD# Low to Address Float		5	ns
T_{LLWL}	ALE/ADV# Low to WR# Low	T_{OSC}–10		ns
T_{CLWL}	CLKOUT Low to WR# Low	–10	25	ns
T_{QVWH}	Data Valid before WR# High	T_{OSC}–23		ns
T_{CHWH}	CLKOUT High to WR# High	–10	15	ns
T_{WLWH}	WR# Low Period	T_{OSC}–30		ns (5)

NOTES:
1. Testing performed at 4 MHz, however, the device is static by design and typically operates below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} x n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. KT customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

Table 3. Specifications Met by the 87C196KT (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units
T_{WHQX}	Data Hold after WR# High	T_{OSC}–30		ns
T_{WHLH}	WR# High to ALE/ADV# High	T_{OSC}–10	T_{OSC}+15	ns (3)
T_{WHBX}	BHE#, INST Hold after WR# High	T_{OSC}–10		ns
T_{WHAX}	AD8-15 Hold after WR# High	T_{OSC}–30		ns (4)
T_{RHBX}	BHE#/INST Hold after RD# High	T_{OSC}–10		ns
T_{RHAX}	AD8-15 Hold after RD# High	T_{OSC}–30		ns (4)

NOTES:
1. Testing performed at 4 MHz, however, the device is static by design and typically operates below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} x n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.
6. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure. The OFD circuitry is enabled by programming the UPROM location 0778H with the value 0004H. KT customer QROM codes need to equate location 2016H to the value 0CDEH if the oscillator fail detect (OFD) function is desired. Intel manufacturing uses location 2016H as a flag to determine whether or not to program the Clock Detect Enable (CDE) bit. Programming the CDE bit enables oscillator fail detection.

Table 4. Require System Specifications for 87C196KT

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2 T_{OSC}–75	ns (3)
T_{LLYV}	ALE Low to READY Setup		T_{OSC}–70	ns (3)
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC}–30	ns (1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2 T_{OSC}–75	ns (2,3)
T_{LLGV}	ALE Low to BUSWIDTH Setup		T_{OSC}–60	ns (2,3)
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC}–55	ns (2)
T_{RLDV}	RD# Active to Input Data Value		T_{OSC}–30	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC}–60	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD# High	0		ns

NOTES:
1. If Max is exceeded, additional wait states occur.
2. If wait states are used, add 2 T_{OSC} x n, where n = number of wait states.
3. If mode 0 is selected, one wait state minimum is always added. If additional wait states are required, add 2 Tosc to the specification.

Figure 5. 87C196KT System Bus Timing

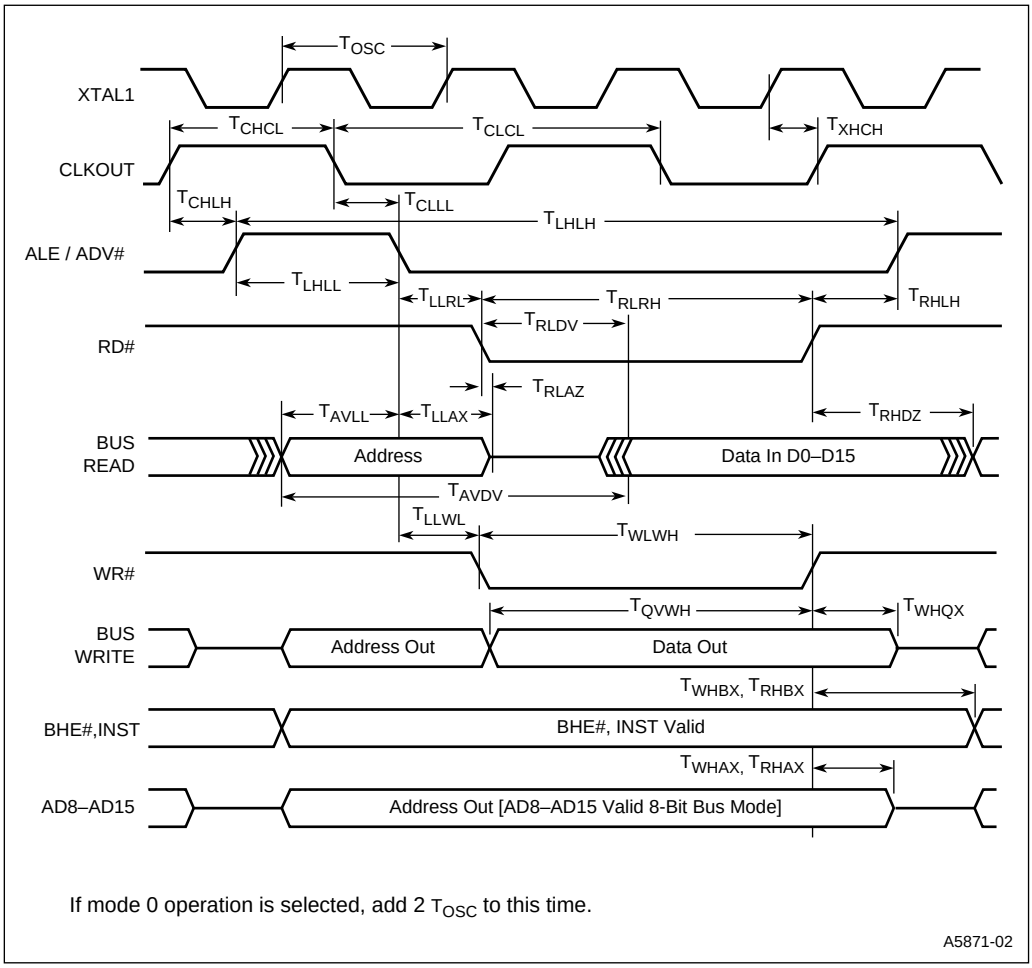
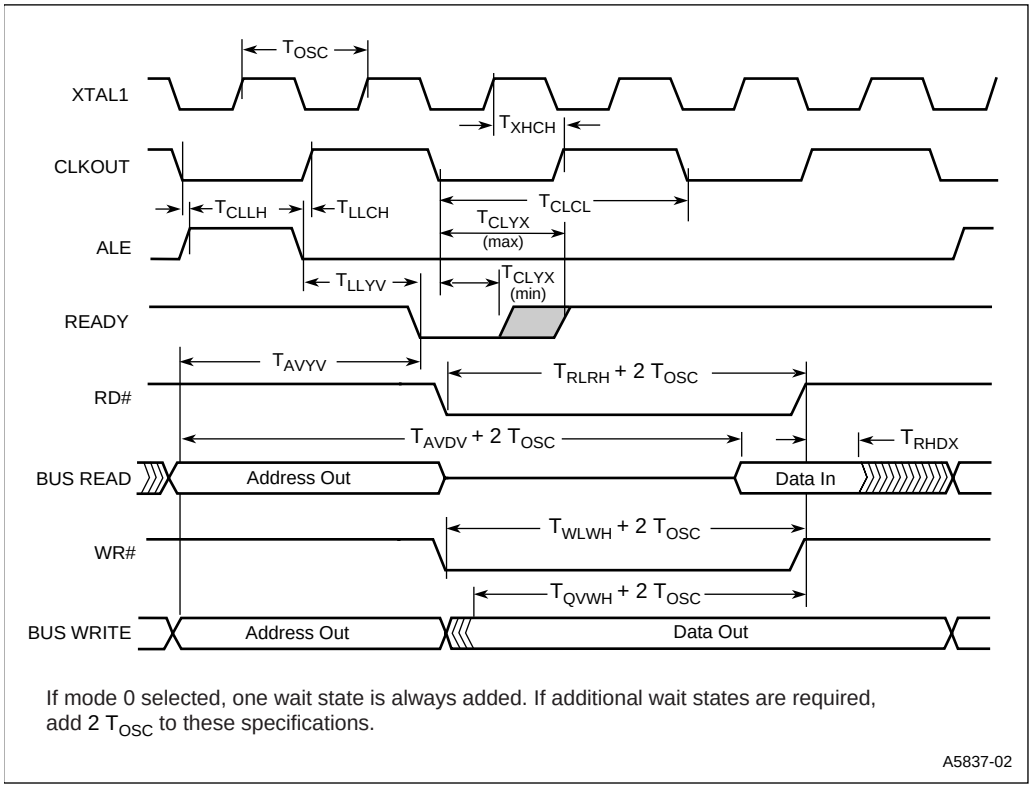


Figure 6. 87C196KT Ready Timings (One Wait State)



If mode 0 selected, one wait state is always added. If additional wait states are required, add 2 T_{OSC} to these specifications.

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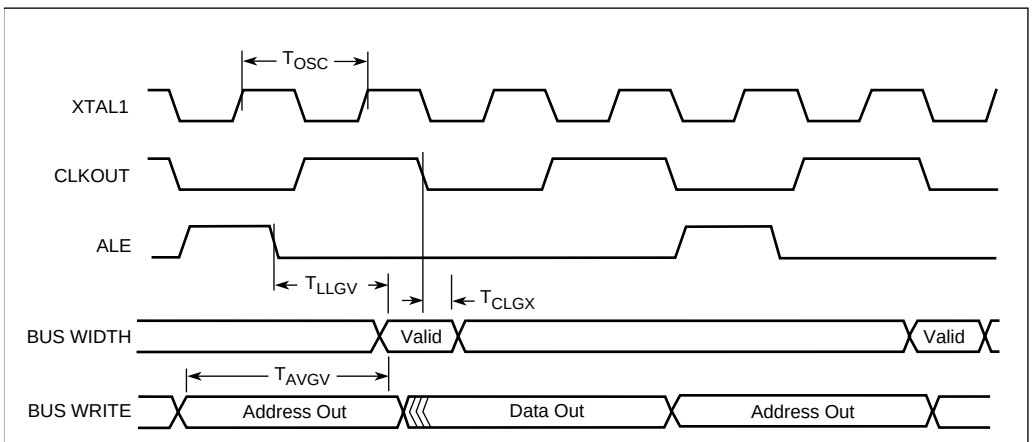
Figure 7. 87C196KT Buswidth Timings



If mode 0 selected, add 2 T_{OSC} to these specifications.

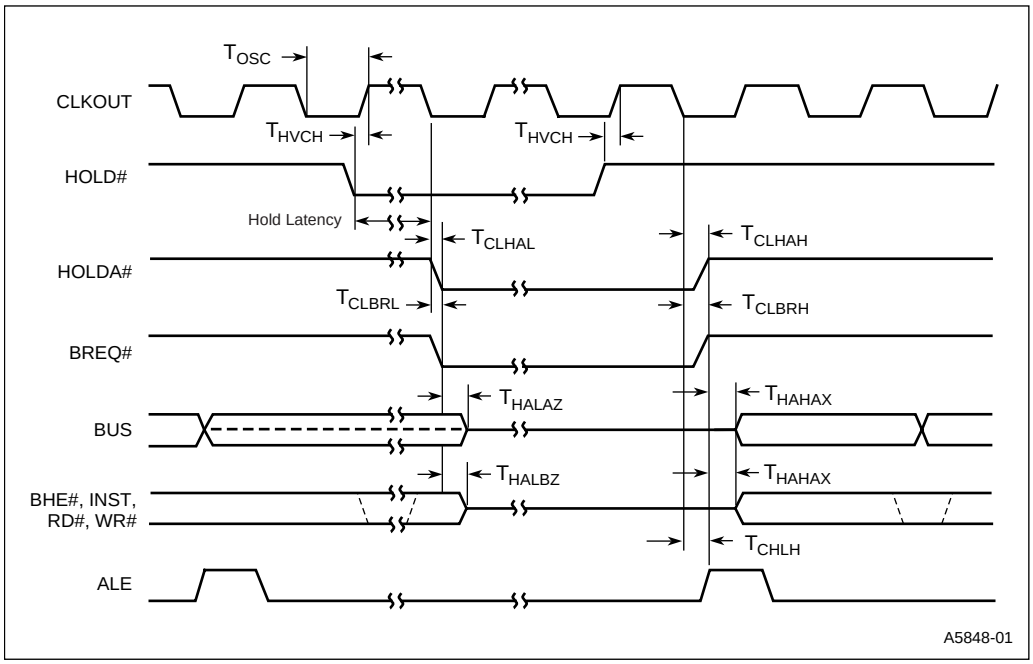
A5861-02

Table 5. 87C196KT HOLD#/HOLDA# Timings (Over Specified Operation Conditions)

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup Time	65		ns (1)
T_{CLHAL}	CLKOUT Low to HLDA# Low	–15	15	ns
T_{CLBRL}	CLKOUT Low to BREQ# Low	–15	15	ns
T_{AZHAL}	HLDA# Low to Address Float		20	ns
T_{BZHAL}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	–25	15	ns
T_{CLBRH}	CLKOUT Low to BREQ# High	–25	25	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	–15		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	–10	15	ns

NOTE:
1. To guarantee recognition at next clock.

Figure 8. 87C196KT HOLD#/HOLDA# Timings



4.3 Bus Mode 1 - AC Characteristics

(Over Specified Operating Conditions)

4.3.1 Test Conditions:

- Capacitance Load on All Pins = 100 pF
- Rise and Fall Times = 10 ns

Table 6. Bus Mode 1 - Specifications Met by the 87C196KT

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8	16	MHz (1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+20	110	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} – 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/ADV# High	0.5 T_{OSC} – 15	0.5 T_{OSC} + 20	ns
T_{CLLL}	CLKOUT LOW to ALE/ADV# Low	0.5 T_{OSC} – 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/ADV# Cycle Time	4 T_{OSC}		ns (5)
T_{LHLL}	ALE/ADV# High Time	T_{OSC} – 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	0.5 T_{OSC} – 15		ns
T_{LLAX}	Address Hold After ALE/ADV# Low	0.5 T_{OSC} – 20		ns
T_{LLRL}	ALE/ADV# Low to RD# Low	0.5 T_{OSC} – 30		ns
T_{RLCL}	RD# Low to CLKOUT Low	T_{OSC} – 10	T_{OSC} + 30	ns
T_{RLRH}	RD# Low Period	2 T_{OSC} – 20		ns (5)
T_{RHLH}	RD# High to ALE/ADV# High	0.5 T_{OSC}	0.5 T_{OSC} + 25	ns (3)
T_{RLAZ}	RD# Low to Address Float		+ 5	ns
T_{LLWL}	ALE/ADV# Low to WR# Low	0.5 T_{OSC} – 10		ns
T_{CLWL}	CLKOUT Low to WR# Low	T_{OSC} – 15	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR# High	2 T_{OSC} – 23		ns
T_{CHWH}	CLKOUT High to WR# High	– 10	+ 15	ns
T_{WLWH}	WR# Low Period	2 T_{OSC} – 15		ns (5)
T_{WHQX}	Data Hold after WR# High	0.5 T_{OSC} – 25		ns
T_{WHLH}	WR# High to ALE/ADV# High	0.5 T_{OSC} – 10	0.5 T_{OSC} + 15	ns (3)
T_{WHBX}	BHE# Hold after WR# High	T_{OSC} – 15		ns
T_{WHIX}	INST Hold after WR# High	0.5 T_{OSC} – 15		
T_{WHAX}	AD8±15 Hold after WR# High	0.5 T_{OSC} – 30		ns (4)
T_{RHBX}	BHE# Hold after RD# High	T_{OSC} – 32		ns
T_{RHAX}	AD8–15 Hold after RD# High	0.5 T_{OSC} – 32		
T_{RHAX}	AD8–15 Hold after RD# High	0.5 T_{OSC} – 30		ns (4)

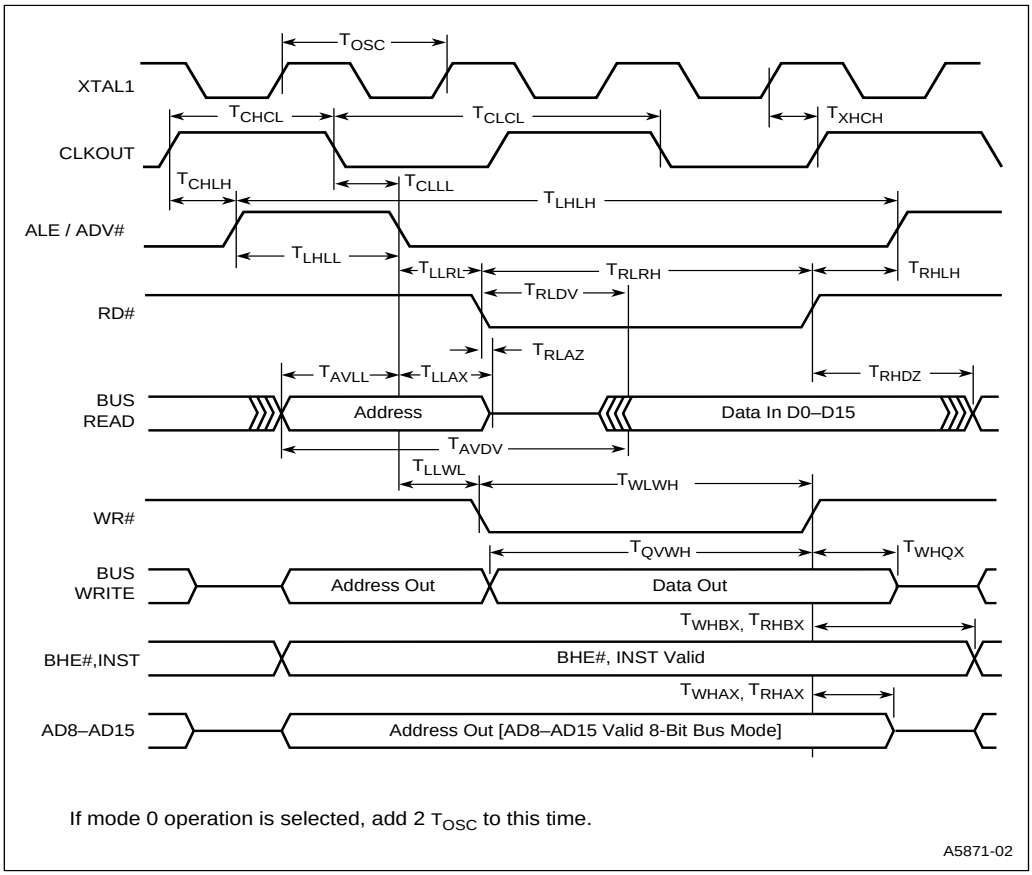
NOTES:
1. Testing performed at 8 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 TOSC x n, where n = number of wait states.

Table 7. Bus Mode 1 - Required System Specifications for 87C196KT

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2 T_{OSC} – 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} – 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} – 30	ns (1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2 T_{OSC} – 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} – 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} – 65	ns (2)
T_{RLDV}	RD# active to input Data Valid		2 T_{OSC} – 44	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} – 60	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{OSC}	ns
T_{RHDX}	Data Hold after RD# High	0		ns

NOTES:
1. If Max is exceeded, additional wait states occur.
2. If wait states are used, add 2 T_{OSC} x n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

Figure 9. Mode 1 - 87C196KT System Bus Timings



4.4 Bus Mode 1 - HOLD#/HOLDA# Timings

(Over Specified Operation Conditions)

4.4.1 Test Conditions:

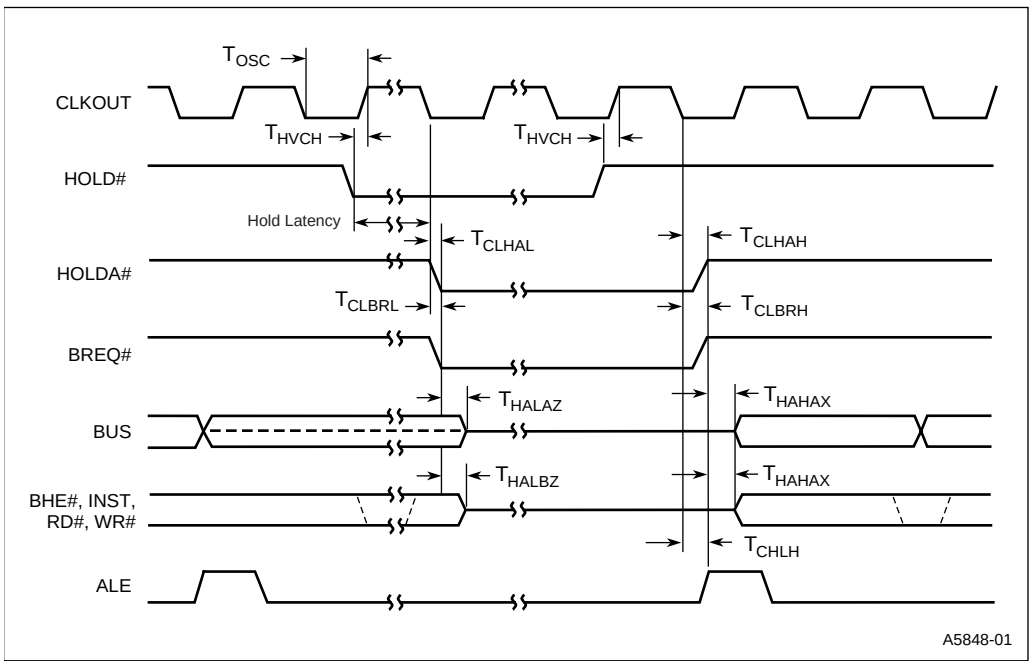
- Capacitance Load on All Pins = 100 pF
- Rise and Fall Times = 10 ns

Table 8. Bus Mode 1 - HOLD#/HOLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD Setup Time	+ 65		ns (1)
T_{CLHAL}	CLKOUT Low to HLDA Low	– 15	+ 15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	– 15	+ 15	ns
T_{AZHAL}	HLDA Low to Address Float		+ 25	ns
T_{BZHAL}	HLDA Low to BHE#, INST, RD#, WR# Weakly Driven		+ 25	ns
T_{CLHAH}	CLKOUT Low to HLDA High	– 25	+ 15	ns
T_{CLBRH}	CLKOUT Low to BREQ High – 25	– 25	+ 15	ns
T_{HAHAX}	HLDA High to Address No Longer Float	– 15		ns
T_{HAHBV}	HLDA High to BHE#, INST, R#D, WR# Valid	– 10		ns

NOTE:
1. To guarantee recognition at next clock.

Figure 10. Mode 1 - 8XC196KT HOLD#/HOLDA# Timings



4.5 Bus Mode 2 - AC Characteristics

(Over Specified Operating Conditions)

4.5.1 Test Conditions:

- Capacitance Load on All Pins = 100 pF
- Rise and Fall Times = 10 ns

Table 9. Bus Mode 2 - Specifications Met by the 87C196KT

Symbol	Parameter	Min	Max	Units
F_{XTAL}	Frequency on XTAL1	8	16	MHz (1)
T_{OSC}	XTAL1 Period ($1/F_{XTAL}$)	62.5	125	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	+ 20	+ 85	ns
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} – 10	T_{OSC} + 27	ns
T_{CHLH}	CLKOUT HIGH to ALE/ADV# High	0.5 T_{OSC} – 15	0.5 T_{OSC} + 20	ns
T_{CLLL}	CLKOUT LOW to ALE/ADV# Low	0.5 T_{OSC} – 25	0.5 T_{OSC} + 15	ns
T_{LHLH}	ALE/ADV# Cycle Time	4 T_{OSC}		ns (5)
T_{LHLL}	ALE/ADV# High Time	T_{OSC} – 10	T_{OSC} + 10	ns
T_{AVLL}	Address Valid to ALE Low	T_{OSC} – 15		ns
T_{LLAX}	Address Hold After ALE/ADV# Low	0.5 T_{OSC} – 20		ns
T_{LLRL}	ALE/ADV# Low to R#D Low	0.5 T_{OSC} – 30		ns
T_{RLCL}	RD# Low to CLKOUT Low	T_{OSC} – 10	T_{OSC} + 30	
T_{RLRH}	RD# Low Period	2 T_{OSC} – 20		ns (5)
T_{RHLH}	RD# High to ALE/ADV# High	0.5 T_{OSC} – 5	0.5 T_{OSC} + 25	ns (3)
T_{RLAZ}	RD# Low to Address Float		+ 5	ns
T_{LLWL}	ALE/ADV# Low to WR# Low	0.5 T_{OSC} – 10		ns
T_{CLWL}	CLKOUT Low to WR# Low	T_{OSC} – 22	T_{OSC} + 25	ns
T_{QVWH}	Data Valid before WR# High	2 T_{OSC} – 25		ns
T_{CHWH}	CLKOUT High to WR# High	– 10	+ 15	ns
T_{WLWH}	WR# Low Period	2 T_{OSC} – 20		ns (5)
T_{WHQX}	Data Hold after WR# High	0.5 T_{OSC} – 25		ns
T_{WHLH}	WR# High to ALE/ADV# High	0.5 T_{OSC} – 10	0.5 T_{OSC} + 10	ns (3)
T_{WHBX}	BHE# Hold after WR# High	T_{OSC} – 15		ns
T_{WHIX}	INST Hold after WR# High	0.5 T_{OSC} – 15		
T_{WHAX}	AD8–15 Hold after WR# High	0.5 T_{OSC} – 30		ns (4)
T_{RHBX}	BHE# Hold after RD# High	T_{OSC} – 32		ns
T_{RHIX}	INST Hold after RD# High	0.5 T_{OSC} – 32		
T_{RHAX}	AD8–15 Hold after RD# High	0.5 T_{OSC} – 30		ns (4)

NOTES:
1. Testing performed at 8 MHz, however, the device is static by design and will typically operate below 1 Hz.
2. Typical specifications, not guaranteed.
3. Assuming back-to-back bus cycles.
4. 8-bit bus only.
5. If wait states are used, add 2 T_{OSC} x n, where n e number of wait states.

Table 10. Bus Mode 2 - Required System Specifications for 87C196KT

Symbol	Parameter	Min	Max	Units
T_{AVYV}	Address Valid to Ready Setup		2.5 T_{OSC} – 75	ns
T_{LLYV}	ALE Low to READY Setup		1.5 T_{OSC} – 70	ns
T_{YLYH}	Non READY Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} – 30	ns (1)
T_{AVGV}	Address Valid to BUSWIDTH Setup		2.5 T_{OSC} – 75	ns
T_{LLGV}	ALE Low to BUSWIDTH Setup		1.5 T_{OSC} – 60	ns
T_{CLGX}	BUSWIDTH Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3.5 T_{OSC} – 60	ns (2)
T_{RLDV}	RD# active to Input Data Valid		2 T_{OSC} – 44	ns (2)
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} – 60	ns
T_{RHDZ}	End of RD# to Input Data Float		0.5 T_{OSC}	ns
T_{RHDX}	Data Hold after RD# High	0		ns

NOTES:
1. If Max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T_{OSC} x n, where n = number of wait states. If mode 0 (1 automatic wait state added) operation is selected, add 2 T_{OSC} to specification.

Figure 11. Mode 2 - 87C196KT System Bus Timings

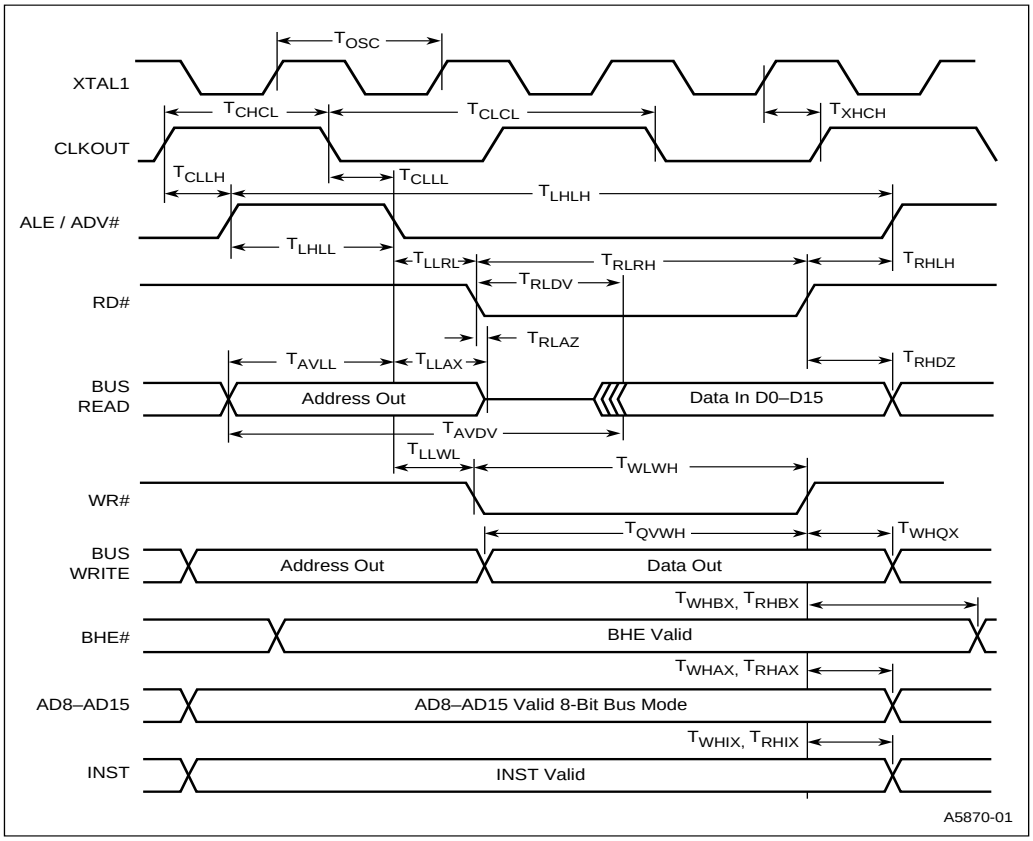


Figure 12. Mode 2 - 87C196KT READY Timings (One Wait State)

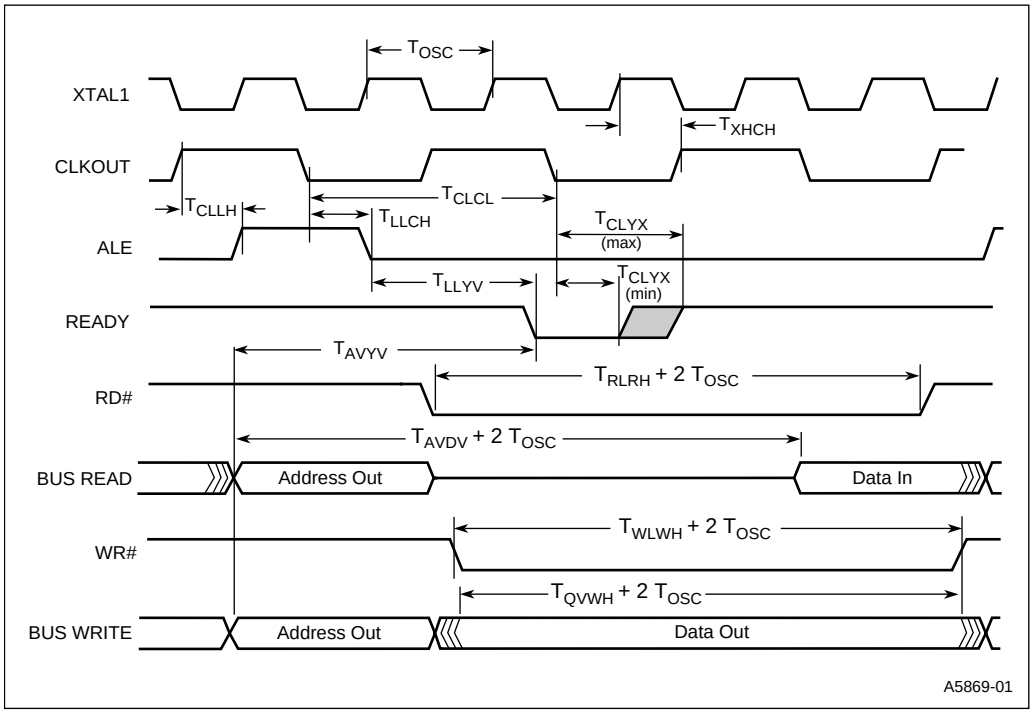
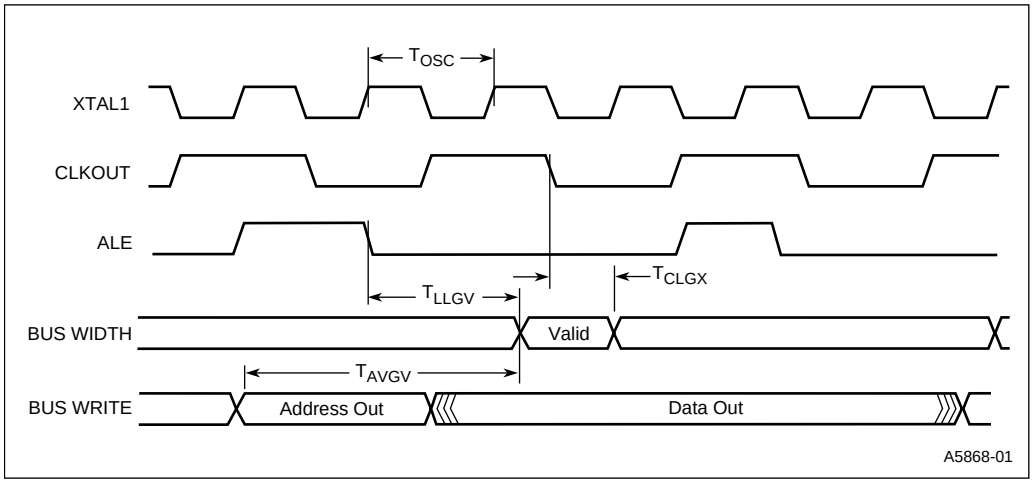


Figure 13. Mode 2 - 87C196KT BUSWIDTH Timings



4.6 Bus Mode 2 - HOLD#/HOLDA# Timings

(Over Specified Operation Conditions)

4.6.1 Test Conditions:

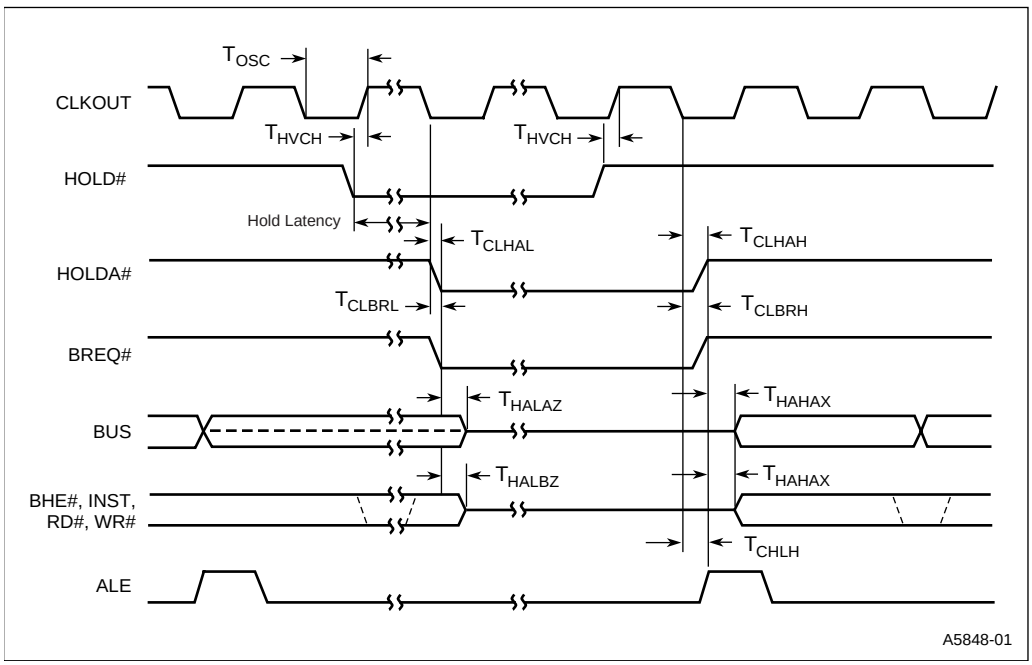
- Capacitance Load on All Pins = 100 pF
- Rise and Fall Times = 10 ns.

Table 11. Bus Mode 2 - HOLD#/HOLDA# Timings

Symbol	Parameter	Min	Max	Units
T_{HVCH}	HOLD# Setup Time	+ 65		ns (1)
T_{CLHAL}	CLKOUT Low to HLDA# Low	– 15	+ 15	ns
T_{CLBRL}	CLKOUT Low to BREQ Low	– 15	+ 15	ns
T_{AZHAL}	HLDA# Low to Address Float		+ 25	ns
T_{BZHAL}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		+ 25	ns
T_{CLHAH}	CLKOUT Low to HLDA# High	– 25	+ 15	ns
T_{CLBRH}	CLKOUT Low to BREQ High	– 25	+ 15	ns
T_{HAHAX}	HLDA# High to Address No Longer Float	– 15		ns
T_{HAHBV}	HLDA# High to BHE#, INST, RD#, WR# Valid	– 10		ns

NOTE:
1. To guarantee recognition at next clock.

Figure 14. Mode 2 - 8XC196KT HOLD#/HOLDA# Timings



4.6.2 AC Characteristics - Slave Port

Figure 15. Slave Port Waveform - (SLPL = 0)

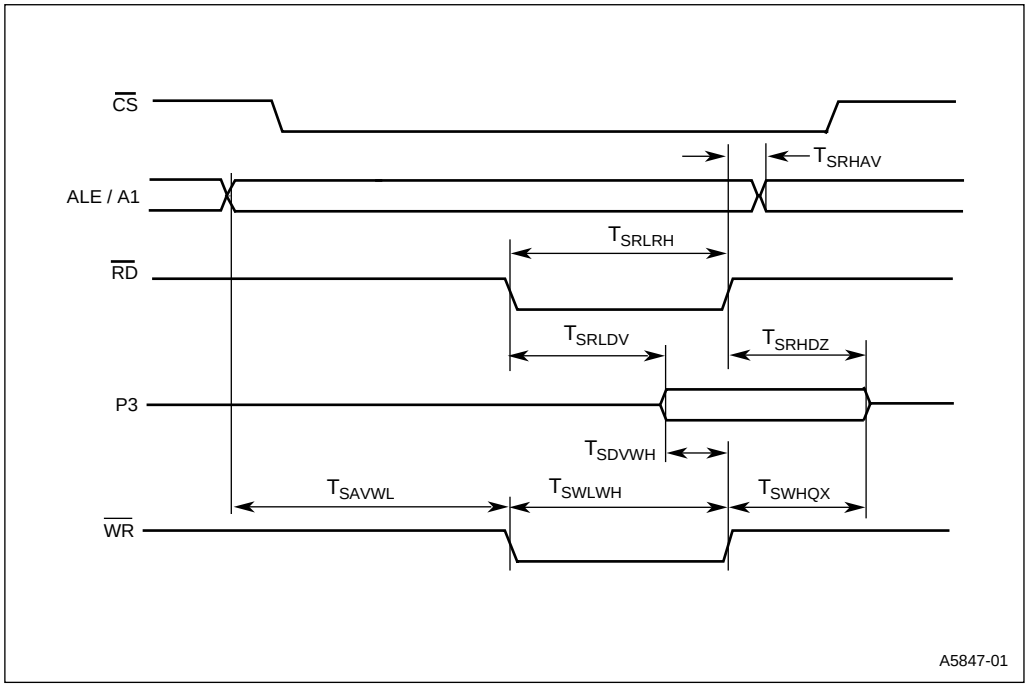


Table 12. Slave Port Timing - (SLPL = 0, 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to WR# Low	50		ns
T_{SRHAV}	RD# High to Address Valid	60		ns
T_{SRLRH}	RD# Low Period	T_{OSC}		ns
T_{SWLWH}	WR# Low Period	T_{OSC}		ns
T_{SRLDV}	RD# Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to WR# High	20		ns
T_{SWHQX}	WR# High to Data Invalid	30		ns
T_{SRHDZ}	RD# High to Data Float	15		ns

NOTE:
1. Test Conditions:
   - F_{OSC} = 16 MHz
   - T_{OSC} = 60 ns
   - Rise/Fall Time = 10 ns
   - Capacitive Pin Load = 100 pF
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.

Figure 16. Slave Port Waveform - (SLPL = 1)

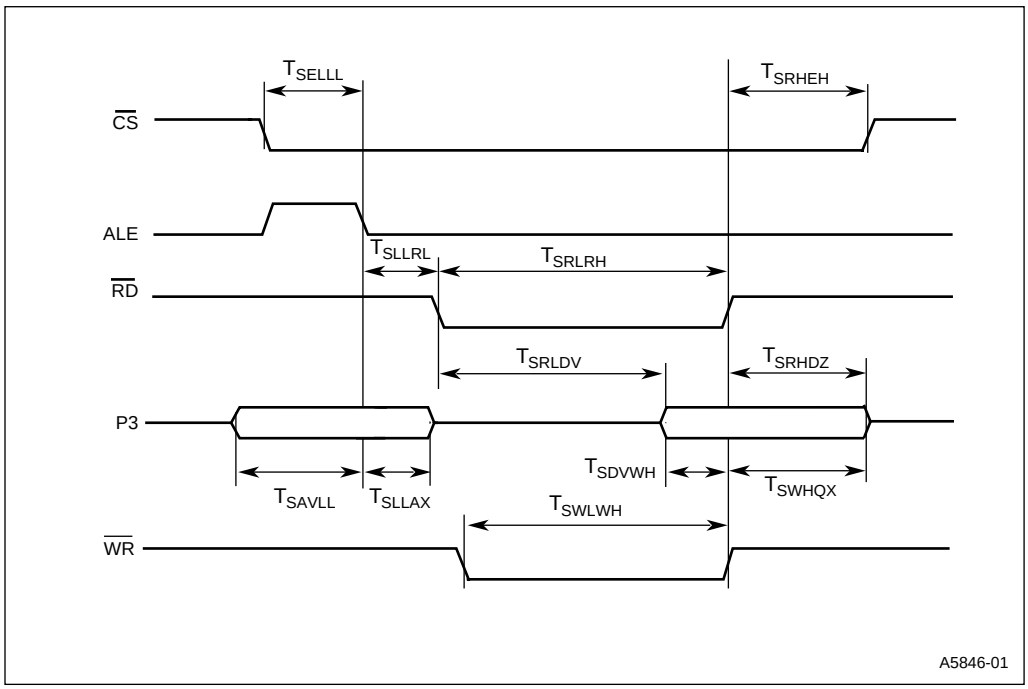


Table 13. Slave Port Timing - (SLPL = 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SELLL}	CS# Low to ALE Low	20		ns
T_{SRHEH}	RD# or WR# High to CS# High	60		ns
T_{SLLRL}	ALE Low to RD# Low	T_{OSC}		ns
T_{SRLRH}	RD# Low Period	T_{OSC}		ns
T_{SWLWH}	WR# Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	RD# Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to WR# High	20		ns
T_{SWHQX}	WR# High to Data Invalid	30		ns
T_{SRHDZ}	RD# High to Data Float	15		ns

NOTE:

1. Test Conditions:
   - F_{OSC} = 16 MHz
   - T_{OSC} = 60 ns
   - Rise/Fall Time = 10 ns
   - Capacitive Pin Load = 100 pF
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.

Table 14. External Clock Drive

Symbol	Parameter	Min (1)	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High TIme	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise TIme		10	ns
T_{XHXL}	Fall Time		10	ns

Figure 17. External Clock Drive Waveforms

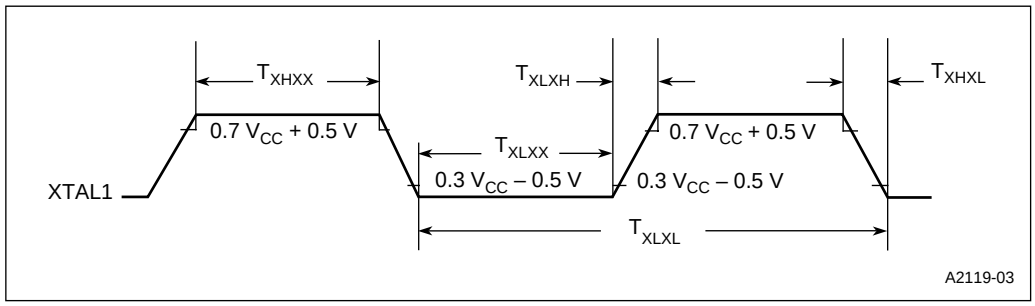
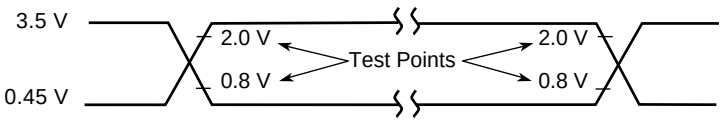


Figure 18. Input/Output Test Conditions



Note:
AC testing inputs are driven at 3.5 V for a logic " 1" and 0.45 V for a logic " 0" . Timing measurements are made at 2.0 V for a logic " 1" and 0.8 V for a logic " 0".

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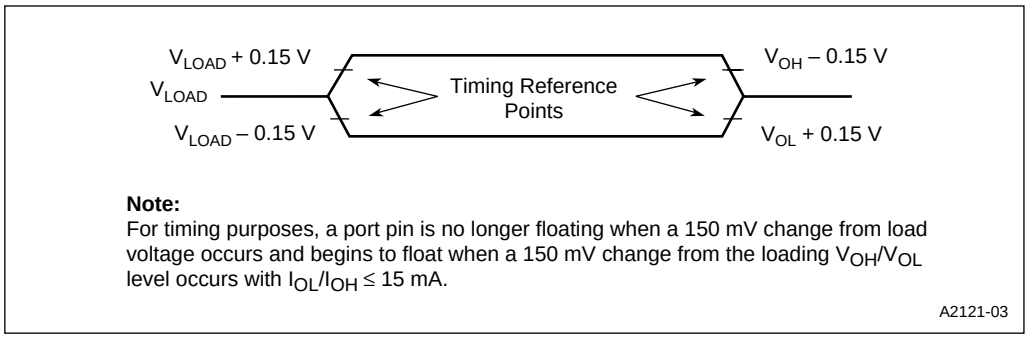
Figure 19. Float Test Conditions



Note:
For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A2121-03

Table 15. Thermal Characteristics

Device and Package	Θ_{JA}	Θ_{JC}
AN87C196KT 16 MHz (68-Lead PLCC)	36.5°C/W	13°C/W

NOTES:
1. Θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 ft. away from case in air flow environment.
   Θ_{JC} = Thermal resistance between junction and package surface (case).
2. All values of Θ_{JA} and Θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ± 2°C/W.
3. Values listed are at a maximum power dissipation of 0.5 W.

4.6.3 Explanation of AC Symbols

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Table 16. Explanation of AC Symbols

Conditions	Signals	
H – High	A – Address	HA – HLDA#
L – Low	B – BHE#	L – ALE/ADV#
V – Valid	BR – BREQ#	Q – Data Out
X – No Longer Valid	C – CLKOUT	R – RD#
Z – Floating	D – DATA	W – WR#/WRH#/WRI#
	G – Buswidth	X – XTAL1
	H – HOLD#	Y – READY

4.7 EPROM Specifications

4.7.1 AC EPROM Programming Characteristics

Operating Conditions:

- Load Capacitance = 150 pF
- T_C = 25°C ± 5°C
- V_{REF} = 5.0 V ± 0.5 V
- V_{CC} = 5.0 V ±0.5 V
- ANGND = 0 V
- V_{PP} = 12.5 V ± 0.25 V
- V_{SS} = 0 V
- EA# = 12.5 V ± 0.25 V
- F_{OSC} = 5.0 MHz

Table 17. AC EPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	PALE# Pulse Width	50		T_{OSC}
T_{PLPH}	PROG# Pulse Width	50		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PHLL}	PROG# High to Next PALE# Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	PROG# High to Next PROG# Low	220		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PLDV}	PROG# Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	RESET# High to First PALE# Low	1100		T_{OSC}
T_{PHIL}	PROG# High to AINC# Low	0		T_{OSC}
T_{ILIH}	AINC# Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after AINC# Low	50		T_{OSC}
T_{ILPL}	AINC# Low to PROG# Low	170		T_{OSC}
T_{PHVL}	PROG# High to PVER# Valid		220	T_{OSC}

NOTES:
1. Run time programming is done with F_{OSC} = 6 MHz to 10 MHz, V_{CC}, V_{PD}, V_{REF} = 5 V ±0.5 V, T_C = 25°C ±5°C and V_{PP} = 12.5 V ± 0.25 V.
2. Programming Specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses use 300 T_{OSC} + 100 µs.

Table 18. DC EPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		200	mA

NOTE: V_{PP} must be within 1 V of V_{CC} while V_{CC} < 4.5 V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5 V.

4.7.2 EPROM Programming Waveforms

Figure 20. Slave Programming Mode Data Program Mode with Single Program Pulse

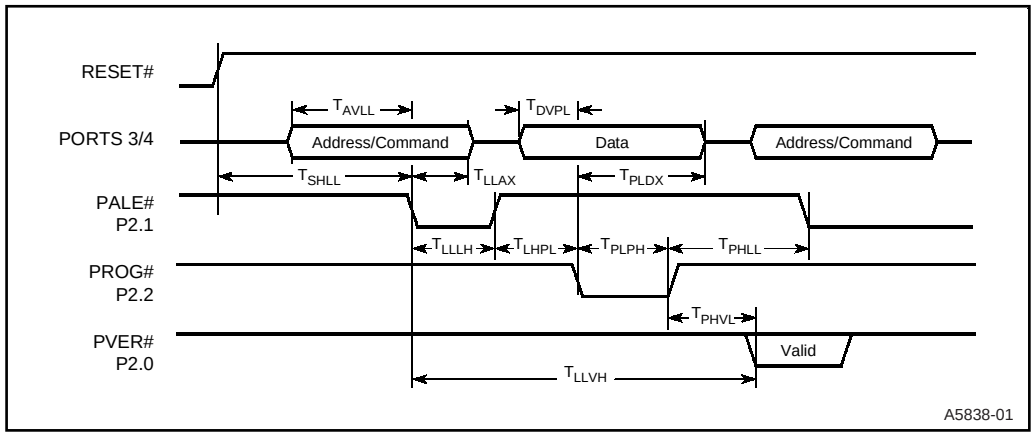


Figure 21. Slave Programming Mode in Word Dump or Data Verify Mode with Auto Increment

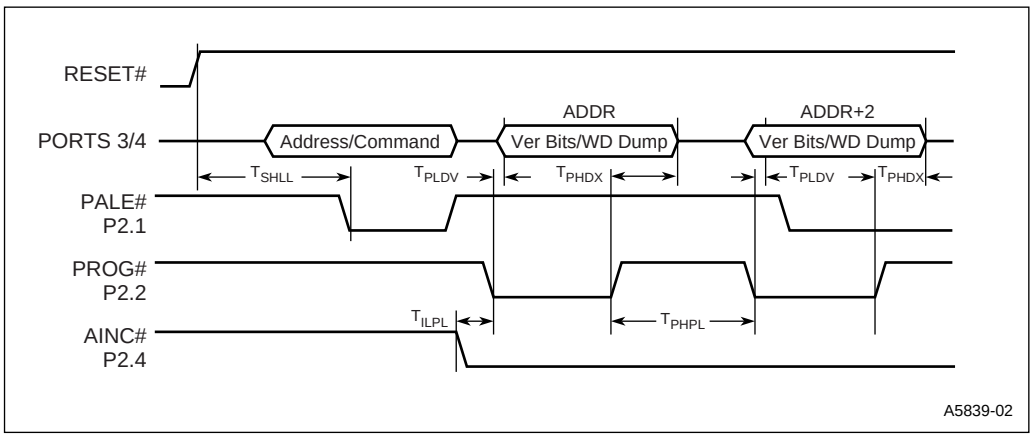
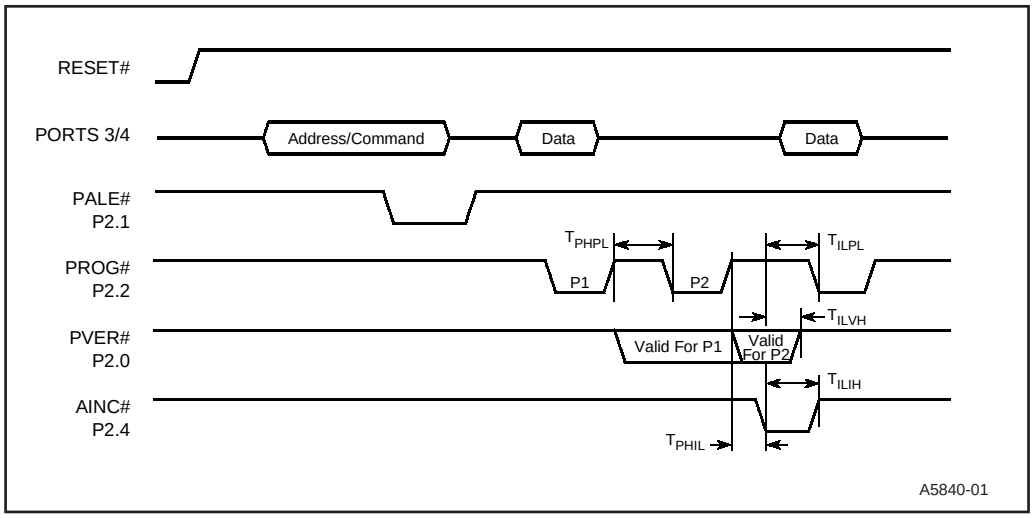


Figure 22. Slave Programming Mode Timing in Data Program Mode with Repeated Program Pulse and Auto Increment



4.8 AC Characteristics - Serial Port - Shift Register Mode

Operating Conditions:

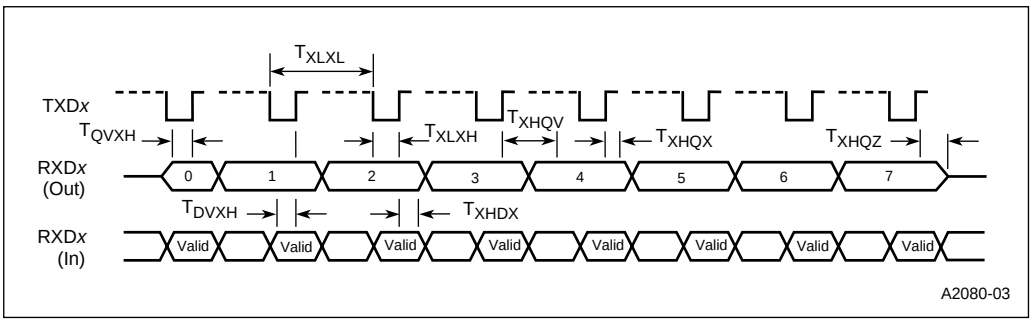
- T_A = –40°C +125°C
- V_{SS} = 0.0 V
- V_{CC} = 5.0 V ±10%
- Load Capacitance = 100 pF

Table 19. Serial Port Timing - Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} – 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} – 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTE:
1. Parameters not tested.

Figure 23. Waveform - Serial Port - Shift Register Mode

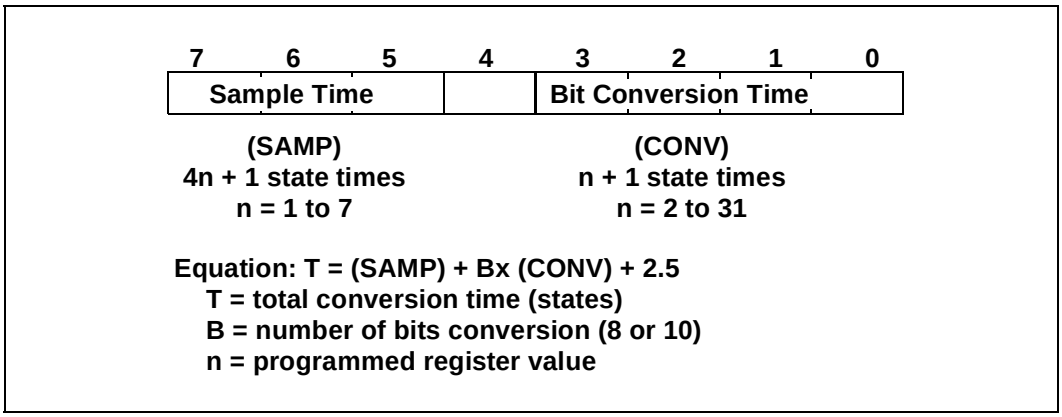


4.8.1 A/D Characteristics

The sample and conversion time of the A/D converter in the 8-bit or 10-bit modes is programmed by loading a byte into the AD_TIME Special Function Register. This allows optimizing the A/D operation for specific applications. The AD_TIME register is functional for all possible values, but the accuracy of the A/D converter is only guaranteed for the times specified in the operating conditions table.

The value loaded into AD_TIME bits 5, 6, 7 determines the sample time, SAMP. The value loaded into AD_TIME bits 0, 1, 2, 3 and 4 determines the bit conversion time, CONV. These bits, as well as the equation for calculating the total conversion time, T, are shown in Figure 24.

Figure 24. AD_TIME 1FAFH:Byte



The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}. V_{REF} must be close to V_{CC} since it supplies both the resistor ladder and the analog portion of the converter and input port pins. There is also an AD_TEST SFR that allows for conversion on ANGND and V_{REF} as well as adjusting the zero offset. The absolute error listed is without doing any adjustments.

4.8.1.1 A/D Converter Specification

The specifications given assume adherence to the operating conditions section of this data sheet. Testing is performed with V_{REF} = 5.12 V and 16 MHz operating frequency. After a conversion is started, the device is placed in IDLE mode until the conversion is complete.

Table 20. 10-Bit Mode A/D Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	–40	125	°C
V_{CC}	Digital Supply Voltage	4.5	5.5	V
V_{REF}	Analog Supply Voltage	4.5	5.5	V (1)
T_{SAM}	Sample Time	2		µs (2)
T_{CONV}	Conversion Time	12	15	µs (2)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. V_{REF} must be within +0.5 V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

Table 21. 10-Bit Mode A/D Characteristics (Using Above Operating Conditions)

Parameter	Typical (2,3)	Min	Max	Units (4)	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	± 3	LSBs	
Full-scale Error	0.25 ± 0.5			LSBs	
Zero Offset Error	0.25 ± 0.5			LSBs	
Non-Linearity	1 ± 2		± 3	LSBs	
Differential Non-Linearity		– 0.75	0.75	LSBs	
Channel-to-Channel Matching	± 0.1	0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	(2)
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	0.009			LSB/C	(2)
Off Isolation		– 60		dB	(2,5,6)
Feedthrough	– 60			dB	(2,5)
V_{CC} Power Supply Rejection	– 60			dB	(2,5)
Input Resistance		750	1.2 K	Ω	(7)
DC Input Leakage	± 1	– 1.5	1.5	µA	
Sampling Capacitor	3			pF	

NOTES:
1. All conversions performed with processor in IDLE mode.
2. These values are expected for most parts at 25°C but are not tested or guaranteed.
3. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
4. An “LSB”, as used here, has a value of approximately 5 mV
5. DC to 100 KHz
6. Multiplexer Break-Before-Make Guaranteed.
7. Resistance from device pin, through internal MUX, to sample capacitor.

Table 22. 8-Bit Mode A/D Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	–40	125	°C
V_{CC}	Digital Supply Voltage	4.5	5.5	V
V_{REF}	Analog Supply Voltage	4.5	5.5	V (1)
T_{SAM}	Sample Time	2		µs (2)
T_{CONV}	Conversion Time	12	15	µs (2)
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. V_{REF} must be within+0.5 V of V_{CC}.
2. The value of AD_TIME is selected to meet these specifications.

Table 23. 8-Bit Mode A/D Characteristics (Using Above Operating Conditions) (1)

Parameter	Typical (2,3)	Min	Max	Units (4)	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	± 1	LSBs	
Full-scale Error	± 0.5			LSBs	
Zero Offset Error	± 0.5			LSBs	
Non-Linearity		0	± 1	LSBs	
Differential Non-Linearity		– 0.5	+ 0.5	LSBs	
Channel-to-Channel Matching		0	± 1	LSBs	
Repeatability	± 0.25	0		LSBs	(2)
Temperature Coefficients: Offset Fullscale Differential Non-Linearity	0.003			LSB/C	(2)
Off Isolation		– 60		dB	(2,5,6)
Feedthrough	– 60			dB	(2,5)
V_{CC} Power Supply Rejection	– 60			dB	(2,5)
Input Resistance		750	1.2 K	Ω	(7)
DC Input Leakage	± 1	– 1.5	1.5	µA	
Sampling Capacitor	3			pF	

NOTES:
1. All conversions performed with processor in IDLE mode.
2. These values are expected for most parts at 25°C but are not tested or guaranteed.
3. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
4. An “LSB”, as used here, has a value of approximately 5 mV
5. DC to 100 KHz
6. Multiplexer Break-Before-Make Guaranteed.
7. Resistance from device pin, through internal MUX, to sample capacitor.

4.8.2 87C196KT 16 MHz Errata

The following is a list of all known functional deviations for 87C196KT 16 MHz device. B-step and later devices can be identified by a special mark following the eight digit FPO number on the top of the package. For C-step devices, this mark is a “C”.

1. HOLD# OR READY DURING DIVIDE; (A-step):

   There is a bug in the DIV and DIVB (signed divide) instructions such that if the following 2 conditions are met, there may be an error of 1 in the quotient:

   a. HOLD# or READY is asserted during the first state of execution of the DIV and DIVB instruction.

   b. HOLD# or READY duration is 16 state times for the DIVB or 24 state times for a DIV instruction.

2. P2.7 (CLKOUT); (A-step):

   Port 2.7 (CLKOUT) does not operate in open drain mode.

3. P2_REG.7 AND P6_REG.4 THROUGH P6_REG.7 CLEARED: (A-step):

   P2_REG.7 is cleared when P2_SSEL.7 bit is changed from a 1 to a 0 (special function to LSIO). P6_Reg.4–.7 is cleared when the corresponding P6_SSEL.4–.7 is changed from a 1 to a 0.

4. INDIRECT SHIFT INSTRUCTION; (A-step):

   The upper three bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 x n, where n = 1, 3, 5 or 7, the operand wil be shifted 32 times. The above condition results in NO shift taking place.

5. INTERNAL RAM POWERDOWN LEAKAGE; (A-step):

   If an invalid address is applied to the internal RAM during powerdown, the address lines float. This can cause increased current consumption during powerdown. To insure a valid address on the internal RAM, execute the idle/power-down instruction from internal RAM.

6. INST PIN; (A-step):

   On A-step devices, the INST pin is pulled medium low for approx. 200 ns after RESET and then pulled weakly HIGH until P5SSEL is written to. This is corrected on B-step devices where the INST pin is pulled medium low for approx. 200 ns after RESET and is then pulled weakly LOW until P5SSEL is written to.

7. REGISTER RAM OVERWRITE; (A-step, B-step):

   If a write is performed to a byte/word location within the SFR range of 1F60h to 1FFFh, the data to be written is also written to a correspondding location located within the REGISTER RAM space 360h to 3FFh. To determine the address of the REGISTER RAM location that is overwritten, an offset of 1C00h can be subtracted from the byte/word addressed in the SFR range.

8. 8. BUS TIMING MODES 1 AND 2 (A-step, B-step):

   Bus timing modes 1 and 2 are not featured or specified on A-step and B-step parts. On C-step parts Mode 1 is selected by setting bits MSEL1 e 0 and MSEL0 e 1 in the CCB1 register. Mode 2 is similarly selected by setting MSEL1 e 1 and MSEL0 e 0. Timings are altered by Mode 1 and Mode 2 as follows (for actual values see the Bus Mode 1 and Bus Mode 2 AC haracteristics in this data sheet):

   Mode 1: RD#, WR# advanced 1 T_{OSC}
   ALE advanced 0.5 T_{OSC}
   ALE pulse width remains 1 T_{OSC}
   Mode 2: RD#, WR# advanced 1 T_{OSC}
   ALE advanced 0.5 T_{OSC}
   ALE pulse width remains 1 T_{OSC}
   Address advanced 0.5 T_{OSC}

9. V_{OH2} (A-step, b-step):

   A- and B-step parts are capable of $V_{OH2} = V_{CC} – 1$ V with $I_{OH} = –6\mu A$. C-step devices meet the target values of $V_{OH2} = V_{CC} – 1$ V with $I_{OH} = –15$ µA.

10. . CLKOUT DURING RESET (A-step, B-step, C-step):

    For all steppings of the 87C196KT, the CLKOUT function during RESET (P2.7) differs from the 87C196KR C-step. During RESET on the 87C196KT, CLKOUT does not toggle and remains in the high state. During RESET on the 87C196KR C-step CLKOUT countinues to toggle.

4.8.3 87C196KT 16 MHz Design Considerations

1. EPA TIMER RESET/WRITE CONFLICT

   If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

2. VALID TIME MATCHES

   The timer must increment/decrement to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

3. P6_PIN.4-.7 NOT UPDATED IMMEDIATELY

   Values written to P6_REG are temporarily held in a buffer. If P6_MODE is cleared, the buffer is loaded into P6_REG.x If P6_MODE is set, the value stays in the buffer and is loaded into P6_REG.x when P6_MODE.x is cleared. Since reading P6_REG returns the current value in P6_REG and not the buffer, changes to P6_REG cannot be read until/unless P6_MODE.x is cleared.

4. WRITE CYCLE DURING RESET

   If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

5. INDIRECT SHIFT INSTRUCTION

   The upper 3 bits of the byte register holding the shift count are not masked completely. If the

shift count register has the value 32 x n, where n = 1, 3, 5, or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

6. EPA Overruns

   EPA “lock-up” can occur if overruns are not handled correctly, refer to Intel Techbit #DB0459 “Understanding EPA Capture Overruns”, date 12-9-93. Applies to EPA channels with interrupts and overruns enabled (ON/RT bit set to 1).

7. Indirect Addressing with Auto-Increment

   For the special case of a pointer pointing to itself using auto-increment, an incorrect access of the incremented pointer address will occur instead of an access to the original pointer address. All other indirect auto-increment accesses will not be affected. Please refer to Techbit #MCO593.

Incorrect sequence:	Results in ax being incremented by 1 and the contents of the address pointed to by ax+1 to be loaded into bx.

```
ld   ax,#ax
ldb  bx,[ax]+
```

Suggested sequence:	Results in the contents of the address pointed to by ax to be loaded into bx and ax incremented by 1.

```
ld   ax,#bx; where ax does not equal
bx
ldb  cx,[ax]+
```

5.0 Datasheet Revision History

This is the (-008) version of the 87C196KT 16 MHz datasheet. The following differences exist between the -007 revision and the -008 revision. (Sheet 1 of 2)

Item	Revision
Template	Converted to new template.
Editing	Corrected spelling and grammar errors.
Product Features	Combined product features on cover page with old CPU and Peripheral Features sections.
Section 1.0, “Introduction” on page 1	Combined old cover page text and old Architecture section into new Introduction section.
Section 2.0, “Block Diagram” on page 2	Added text from old cover page.
Figure 2 “68-Pin PLCC 87C196KT 16 MHz Diagram” on page 3	Removed KS designation.
Figure 3 “Chip Configuration Registers” on page 6	Added Figure Title CCB (201AH:Byte): • Changed “WR#” to “BW1” • Revised definitions
Table 2 “DC Characteristics (Under Listed Operating Conditions)” on page 7	I_{PD}: • Max - Deleted TBD V_{IL} - Test Conditions - Changed “Note 8” to “Note 7” V_{IH} - Test Conditions - Changed “Note 8” to “Note 7” V_{OL} and V_{OH} - Test Conditions - Deleted “Note 5”. V_{OH1} - Test Conditions - Changed “Note 7” to “Note 6”. V_{OH2} - Test Conditions - Changed “Note 8” to “Note 7”. C_S - Test Conditions - Changed “Note 6” to “Note 5”. V_{OL3} - Test Conditions - Changed “Note 10” to “Note 9”. RWPU - Test Conditions - Changed “Note 6” to “Note 5”. NOTES: • “Note 5” Deleted
Table 3 “Specifications Met by the 87C196KT” on page 10	Note 6: Removed “KS” designation.
Table 4 “Require System Specifications for 87C196KT” on page 11	T_{RHDZ} - Parameter - Changed “Valid” to “Float”.
Figure 12 “Slave Port Timing - (SLPL = 0, 1, 2, 3)” on page 22	Deleted “Note 3”.
Figure 13 “Slave Port Timing - (SLPL = 1, 2, 3)” on page 23	Deleted “Note 3”.
Figure 18 “Input/Output Test Conditions” on page 24	Added “Output” to title.
Figure 19 “Float Test Conditions” on page 25	Changed “Output” to “Float” in title.
Figure 15 “Thermal Characteristics” on page 25	Removed “KS” designation.
Section 4.8.1.1, “A/D Converter Specification” on page 31	Deleted (italic) - “conversion is *staerted, the device is placed in IDLE mode until the conversion is* completed”.

This is the (-008) version of the 87C196KT 16 MHz datasheet. The following differences exist between the -007 revision and the -008 revision. (Sheet 2 of 2)

Item	Revision
Section 21, “10-Bit Mode A/D Characteristics (Using Above Operating Conditions)” on page 31	Removed “Note” designation from heading. Added “Notes” column. Off Isolation - Changed “Notes 1,2,3” to “2,5,6”. Feedthrough - Changed “Notes 1,2” to “2,5”. V_{CC} Power Supply... - Changed “Notes 1,2” to “2,5”. Input Resistance - Changed “Notes 4” to “7”. Added “Note 7”.
Section 22, “8-Bit Mode A/D Operating Conditions” on page 32	V_{CC} and V_{REF} - Min - Changed “4.5” to “4.75”. V_{CC} and V_{REF} - Max - Changed “5.5” to “5.25”.
Section 23, “8-Bit Mode A/D Characteristics (Using Above Operating Conditions) (1)” on page 32	Added “Notes” column. Off Isolation - Changed “Notes 1,2,3” to “2,5,6”. Feedthrough - Changed “Notes 1,2” to “2,5”. V_{CC} Power Supply... - Changed “Notes 1,2” to “2,5”. Input Resistance - Changed “Notes 4” to “7”. DC Input Leakage: • Min - Changed “0” to “-1.5” • Max - Deleted “+/-”. Added “Note 7”.
Section 4.8.2, “87C196KT 16 MHz Errata” on page 33	Removed “KS” designation from heading.
Section 4.8.3, “87C196KT 16 MHz Design Considerations” on page 34	Removed “KS” designation from heading. Deleted “PORT4 - Address Behavior” section.
Section 5.0, “Datasheet Revision History” on page 36	Updated with revision changes.