SIGNETICS DCL INTEGRATED CIRCUITS

PRELIMINARY SPECIFICATIONS

8821 DUAL MASTER-SLAVE J-K BINARY
8822 DUAL MASTER-SLAVE J-K BINARY
8824 DUAL MASTER-SLAVE J-K BINARY

The 8821, 8822 and 8824 Dual Master-Slave J-K Binaries provide pin configuration and logic input variations of the same basic device to obtain maximum board layout convenience and design flexibility.

The 8821, available in the J package only, provides common clock and $\overline{R}_D$ inputs and separate $\overline{S}_D$ inputs. This configuration is especially useful in synchronous counter and shift register applications. Where a dual in-line package is required, the 8824 is recommended.

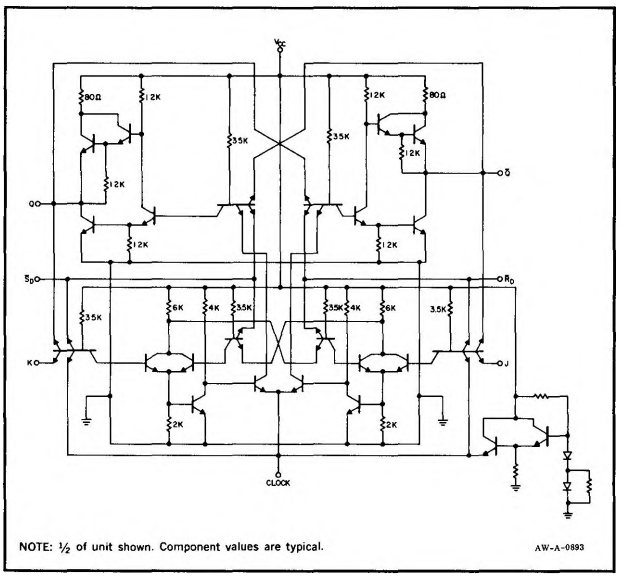
The 8822 provides separate clock and separate $\overline{R}_D$ inputs and is in the dual in-line (A) package and has V_{CC} at pin 14 and ground at pin 7 for consistency with other dual in-line pin configurations. This pin configuration can significantly simplify board layout. The 8822 is also available in the J package.

The 8824 is available in the 16 pin dual in-line (B) package. This unit provides two separate binaries with full synchronous and asynchronous access. The 8824 provides V_{CC} and ground pin orientation which is consistent with other dual in-line devices and thus simplifies board layout.

Triggering is accomplished on the negative transition (falling edge) of the clock pulse. Set up time must be greater than or equal to the clock pulse width. There is no hold time requirement for the inputs. Set up time is defined as the time prior to a negative transition of the clock line.

For optimum reliability, all three devices are fabricated from a single monolithic die.

BASIC CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

AW-A-0893

TRUTH TABLES

8821 AND 8824

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$\overline{S}_D$	$\overline{R}_D$	Q
0	0	†
1	0	0
0	1	1
1	1	Q

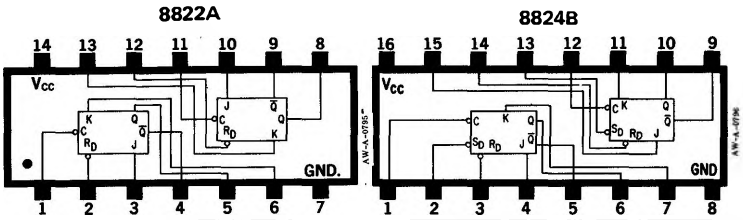
† $Q = \overline{Q} = 1$

8822

J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

$\overline{R}_D = 0 \Rightarrow Q = 0$

A PACKAGE B PACKAGE



8821
8822
8824

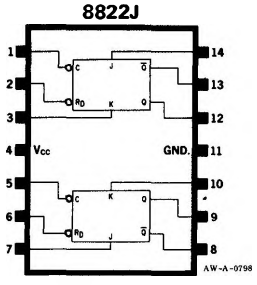
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 15)

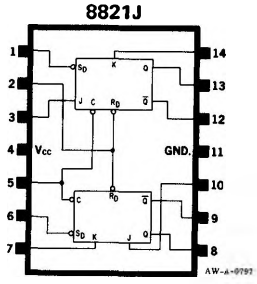
ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS										
		MIN.	TYP.	MAX.	UNITS	TEMP. S8821 S8822 S8824	TEMP. N8821 N8822 N8824	V_{cc}	SET	RESET	DRIVEN INPUT	J	K	CLOCK	OUTPUT	NOTES
A-4	"1" OUTPUT VOLTAGE (Q)	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V					-500μA	8, 16
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V	2.0V					-500μA	8, 16
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V					-500μA	8, 16
A-5	"1" OUTPUT VOLTAGE ($\overline{Q}$)	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V					-500μA	8
A-3		2.8			V	+25°C	+25°C	5.0V	2.0V	0.8V					-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V					-500μA	8
A-5	"0" OUTPUT VOLTAGE (Q)			0.4	V	-55°C	0°C	4.75V	2.0V	0.8V					16mA	9
A-3				0.4	V	+25°C	+25°C	5.0V	2.0V	0.8V					16mA	9
A-4				0.4	V	+125°C	+75°C	4.75V	2.0V	0.8V					16mA	9
A-5	"0" OUTPUT VOLTAGE ($\overline{Q}$)			0.4	V	-55°C	0°C	4.75V	0.8V	2.0V					16mA	9, 16
A-3				0.4	V	+25°C	+25°C	5.0V	0.8V	2.0V					16mA	9, 16
A-4				0.4	V	+125°C	+75°C	4.75V	0.8V	2.0V					16mA	9, 16
C-1	"0" INPUT CURRENT (J,K)			-1.6	mA	-55°C	0°C	5.25V			0.4V					
A-3				-1.6	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.4V					
C-1	"0" INPUT CURRENT			-3.2	mA	-55°C	0°C	5.25V			0.4V					
A-3	(CLOCK, S_D, R_D)			-3.2	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-3.2	mA	+125°C	+75°C	5.25V			0.4V					
C-1	"0" INPUT CURRENT			-6.4	mA	-55°C	0°C	5.25V			0.4V					
A-3	(CLOCK, R_D, 8821 only)			-6.4	mA	+25°C	+25°C	5.25V			0.4V					
C-1				-6.4	mA	+125°C	+75°C	5.25V			0.4V					
A-4	"1" INPUT CURRENT (J,K)			25	μA	+125°C	+75°C	5.0V			4.5V			0V		17
A-4	(CLOCK, S_D, R_D)			50	μA	+125°C	+75°C	5.0V			4.5V					
A-4	(CLOCK, R_D, 8821 only)			100	μA	+125°C	+75°C	5.0V			4.5V	0V	0V			
A-2	POWER CONSUMPTION (Per Binary)			72	mW	+25°C	+25°C	5.25V								
	OUTPUT SHORT CIRCUIT CURRENT															
A-2	Q (except 8822)	-20		-70	mA	+25°C	+25°C	5.0V	0V						0V	
A-2	$\overline{Q}$	-20		-70	mA	+25°C	+25°C	5.0V		0V					0V	
C-1	INPUT LATCH VOLTAGE (All Inputs)	5.5			V	+25°C	+25°C	5.0V			10mA					12, 17
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V							A.C.F.O. = 6	11, 14
A-6	CLOCKED MODE TURN-ON DELAY	10	25	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10, 14
A-6	CLOCKED MODE TURN-OFF DELAY	7	15	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10, 14
A-6	DIRECT MODE TURN-ON DELAY		25	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10, 14
A-6	DIRECT MODE TURN-OFF DELAY		15	50	ns	+25°C	+25°C	5.0V							D.C.F.O. = 20	10, 14
A-6	TOGGLE RATE	10	25		MHz	+25°C	+25°C	5.0V								14
	INPUT CAPACITANCE															
C-2	(J, K)			3.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(R_D, S_D)			6.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(R_D, 8821 only)			12	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(CLOCK)			8.0	pf	+25°C	+25°C	5.0V			2.0V					7
C-2	(CLOCK, 8821 only)			16	pf	+25°C	+25°C	5.0V			2.0V					7

NOTES:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mVrms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
13. Manufacturer reserves the right to make design and process changes and improvements.
14. Detailed test conditions for AC testing are in Section 3.
15. Test conditions and limits for the Set input are not applicable to the 8822.
16. For 8822, momentarily apply zero volts to $\overline{Q}$ and V_{cc} to Q to ensure state of the binary element prior to test measurement.
17. For clock tests, ground J and K. For J,K and S_D tests, ground clock. For R_D tests, ground J on 8821 and clock on 8822 and 8824.

J PACKAGE





R PACKAGE