SIGNETICS

DCL

INTEGRATED CIRCUITS

8828 DUAL D BINARY

The 8828 is a Dual Delay (D) Binary which responds to the positive-going transition of the clock pulse. Each binary has one synchronous logic input (D), a clock line, complementary outputs, and asynchronous set and reset lines. The logic level defined at the D input, prior to activation of the clock, appears at the Q output upon activation of the clock.

The delay binary is ideally suited for general application in shift registers and ripple counters.

Detailed usage rules and suggested applications for the 8828 may be found in Section 4 of the handbook.

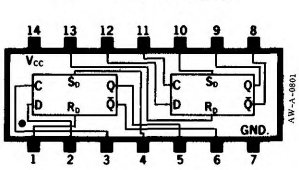
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 13)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS								
		MIN.	TYP.	MAX.	UNITS	TEMP. S8828	TEMP. N8828	V_{cc}	RESET	SET	CLOCK	D	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE (Q_1, Q_2)	2.6	2.8		V	-55°C	0°C	4.75V	2.0V	0.8V			-500μA	7
A-3		2.8	3.1		V	+25°C	+25°C	5.0V	2.0V	0.8V			-500μA	7
A-4		2.6	3.4		V	+125°C	+75°C	4.75V	2.0V	0.8V			-500μA	7
A-5	"1" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)	2.6	2.8		V	-55°C	0°C	4.75V	0.8V	2.0V			-500μA	7
A-3		2.8	3.1		V	+25°C	+25°C	5.0V	0.8V	2.0V			-500μA	7
A-4		2.6	3.4		V	+125°C	+75°C	4.75V	0.8V	2.0V			-500μA	7
A-5	"0" OUTPUT VOLTAGE (Q_1, Q_2)		0.30	0.40	V	-55°C	0°C	4.75V	0.8V	2.0V			16mA	8
A-3			0.30	0.40	V	+25°C	+25°C	5.0V	0.8V	2.0V			16mA	8
A-4			0.30	0.40	V	+125°C	+75°C	4.75V	0,8V	2.0V			16mA	8
A-5	"0" OUTPUT VOLTAGE ($\bar{Q}_1$, $\bar{Q}_2$)		0.30	0.40	V	-55°C	0°C	4.75V	2.0V	0.8V			16mA	8
A-3			0.30	0.40	V	+25°C	+25°C	5.0V	2.0V	0.8V			16mA	8
A-4			0.30	0.40	V	+125°C	+75°C	4.75V	2.0V	0.8V			16mA	8
C-1	"0" INPUT CURRENT (D_1, D_2)	-0.1	-1.3	-1.6	mA	-55°C	0°C	5.25V			0V	0.40V		
A-3		-0.1	-1.3	-1.6	mA	+25°C	+25°C	5.25V			0V	0.40V		
C-1		-0.1	-1.3	-1.6	mA	+125°C	+75°C	5.25V			0V	0.40V		
C-1	"0" INPUT CURRENT	-0.1	-2.5	-3.2	mA	-55°C	0°C	5.25V	0V	0.40V				9
A-3	(SET_1, SET_2)	-0.1	-2.5	-3.2	mA	+25°C	+25°C	5.25V	0V	0.40V				9
C-1		-0.1	-2.5	-3.2	mA	+125°C	+75°C	5.25V	0V	0.40V				9
C-1	"0" INPUT CURRENT	-0.1	-2.5	-3.2	mA	-55°C	0°C	5.25V			0.40V			
A-3	($CLOCK_1$, $CLOCK_2$)	-0.1	-2.5	-3.2	mA	+25°C	+25°C	5.25V			0.40V			
C-1		-0.1	-2.5	-3.2	mA	+125°C	+75°C	5.25V			0.40V			
C-1	"0" INPUT CURRENT	-0.1	-3.3	-4.8	mA	-55°C	0°C	5.25V	0.40V	0V				10
A-3	($RESET_1$, $RESET_2$)	-0.1	-3.3	-4.8	mA	+25°C	+25°C	5.25V	0.40V	0V				10
C-1		-0.1	-3.3	-4.8	mA	+125°C	+75°C	5.25V	0.40V	0V				10
C-1	"1" INPUT CURRENT		10	25	μA	-55°C	0°C	5.0V	0V			4.5V		
C-1	(D_1, D_2)		10	25	μA	+25°C	+25°C	5.0V	0V			4.5V		
A-4			10	25	μA	+125°C	+75°C	5.0V	0V			4.5V		
C-1	"1" INPUT CURRENT		20	50	μA	-55°C	0°C	5.0V		4.5V				11
C-1	(SET_1, SET_2)		20	50	μA	+25°C	+25°C	5.0V		4.5V				11
A-4			20	50	μA	+125°C	+75°C	5.0V		4.5V				11
C-1	"1" INPUT CURRENT		20	50	μA	-55°C	0°C	5.0V	0V		4.5V			
C-1	($CLOCK_1$, $CLOCK_2$)		20	50	μA	+25°C	+25°C	5.0V	0V		4.5V			
A-4			20	50	μA	+125°C	+75°C	5.0V	0V		4.5V			
C-1	"1" INPUT CURRENT		30	75	μA	-55°C	0°C	5.0V	4.5V		0V	0V		12
C-1	($RESET_1$, $RESET_2$)		30	75	μA	+25°C	+25°C	5.0V	4.5V		0V	0V		12
A-4			30	75	μA	+125°C	+75°C	5.0V	4.5V		0V	0V		12
A-2	POWER CONSUMPTION (Per Binary)			610	mW	+25°C	+25°C	5.25V			0V	0V		
A-2	OUTPUT SHORT CIRCUIT CURRENT (Q_1, Q_2)	-10		-55	mA	+25°C	+25°C	5.0V		0V			0V	
A-2	OUTPUT SHORT CIRCUIT CURRENT ($\bar{Q}_1$, $\bar{Q}_2$)	-10		-55	mA	+25°C	+25°C	5.0V	0V				0V	
C-1	INPUT LATCH VOLTAGE (D_1, D_2, $CLOCK_1$, $CLOCK_2$, $CLEAR_1$, $CLEAR_2$, $PRESET_1$, $PRESET_2$)	5.5			V	+25°C	+25°C	5.0V	10mA	10mA	10mA	10mA		13
A-6	TURN-ON DELAY		28	50	ns	+25°C	+25°C	5.0V					D.C. F.O.=20	14, 16
A-6	TURN-OFF DELAY		20	35	ns	+25°C	+25°C	5.0V					D.C. F.O.=20	14, 16
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V					A.C. F.O.=6	16, 17

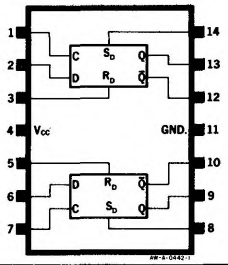
Notes:

1. All voltage and capcitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electricallv open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{cc}.
9. The SET input is specified at two standard loads because if $\bar{Q}$ = "1" when SET goes to "0", the output driving the SET line must be capable of sinking the current from 4 standard loads to make the flip-flop change state. Once the binary state is changed, less than 4 loads will be seen by the driving gate; i.e., when Q = "0".
10. This test simulates worst case transient condition. If SET, RESET, DATA, CLOCK and Q = "1" prior to activating the RESET line, the gate driving RESET must be capable of sinking the current from 6 standard loads. Once the flip-flop changes state, i.e., Q = "0", less than 6 standard loads will be seen by the driving gate.
11. To test "1" Input Current for SET input, momentarily ground SET to ensure Q = "1" and $\bar{Q}$ = "0".
12. To test "1" Input Current for RESET input, momentarily ground RESET to ensure Q = "0".
13. This test guarantees operation free of input latch-up over the specified operating power supply range.
14. One DC fan-out is defined as 0.8mA.
15. Manufacturer reserves the right to make design and process changes and improvements.
16. Detailed test conditions for AC testing are in Section 3.
17. One AC fan-out is defined as 50pf.

A PACKAGE



J PACKAGE



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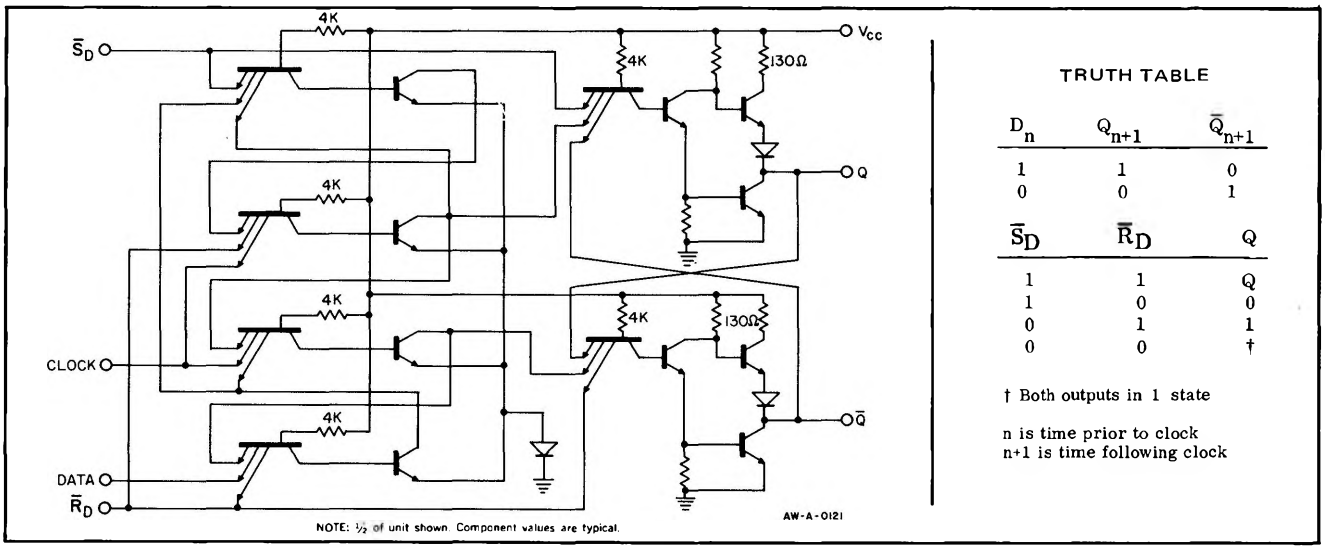
BASIC CIRCUIT SCHEMATIC



TRUTH TABLE

D_n	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	0
0	0	1

$\bar{S}_D$	$\bar{R}_D$	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock
n+1 is time following clock