SIGNETICS DCL INTEGRATED CIRCUITS

8848 EXPANDABLE AND-OR-INVERT GATE

The 8848 Expandable AND-OR-INVERT Gate is designed for the highest switching speed while maintaining high fan-out and noise margin.

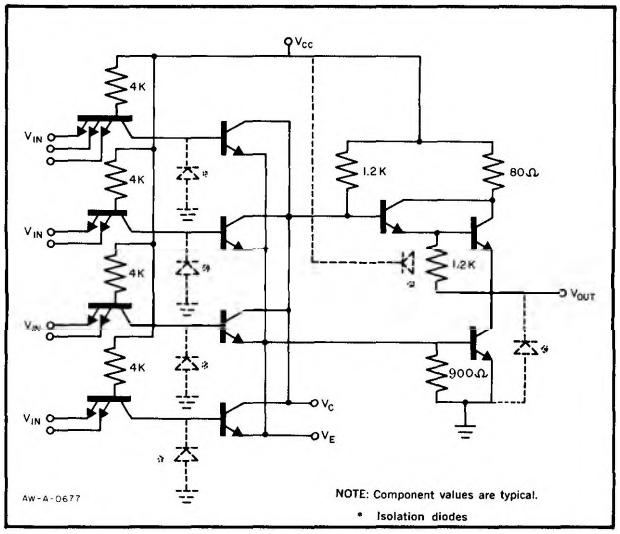
Nodes are provided at the collector and emitter of the second stage. This allows expansion of the number of input AND terms and hence increased system usefulness.

The compatibly characterized 8806 expander is recommended for expansion of the 8848. See correlation table, opposite page.

Low output impedance in the "1" and "0" output states ensures maximum AC noise immunity at the output. General areas of application for the 8848 include half and full adders, digital comparators and AND-OR control logic for inputs to binary clock steering lines.

Detailed usage rules and specific applications are provided in Section 4 of this handbook.

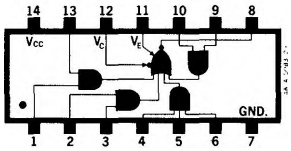
BASIC CIRCUIT SCHEMATIC



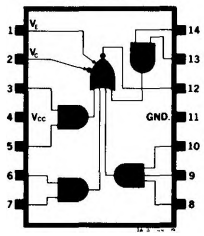
ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 19)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS						
		MIN.	TYP.	MAX.	UNITS	TEMP. S8848	TEMP. N8848	V_{cc}	DRIVEN AND INPUTS	OTHER AND INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V		-500μA	8, 14, 21
A-3		2.8			V	+25°C	+25°C	5.0V	0.8V		-500μA	8, 14, 21
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V		-500μA	8, 14, 21
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
A-3				0.40	V	+25°C	+25°C	5.0V	2.0V	2.0V	16mA	9, 12, 14
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	2.0V	16mA	9, 12, 14
C-1	"0" INPUT CURRENT	-0.1		-1.6	mA	-55°C	0°C	5.25V	0.40V			13, 14
A-3		-0.1		-1.6	mA	+25°C	+25°C	5.25V	0.40V			13, 14
C-1		-0.1		-1.6	mA	+125°C	+75°C	5.25V	0.40V			13, 14
A-4	"1" INPUT CURRENT			25	μA	+125°C	+75°C	5.0V	4.5V	0V		14, 15
A-6	TURN-ON DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 22
A-6	TURN-OFF DELAY			13	ns	+25°C	+25°C	5.0V			D.C. F.O. = 20	10, 22
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V			A.C. F.O. = 6	11, 22
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	+25°C	5.0V	2.0V			7
A-2	POWER CONSUMPTION OUTPUT "0"			48.8	mW	+25°C	+25°C	5.25V				
A-2	(Per Gate) OUTPUT "1"			35.7	mW	+25°C	+25°C	5.25V	0V			14, 16
C-1	INPUT LATCH VOLTAGE RATING	6.0			V	+25°C	+25°C	5.0V	10mA	0V		14, 17, 18
A-2	OUTPUT SHORT CIRCUIT CURRENT	-20		-70	mA	+25°C	+25°C	5.0V	0V		0V	

A PACKAGE



J PACKAGE



8848

CORRELATION TABLE (8806)

ACCEPTANCE TEST SUB-GROUP	TEST NO.	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
			MIN.	TYP.	MAX.	UNITS	TEMP. S8806 N8806	V_{cc}	V_C	V_E	OUTPUTS	NOTES
A-2	1	"0" INPUT CURRENT AT V_C	-2.2		-3.65	mA	+25°C	4.75V	1.25V			20
A-2	2	TURN-ON VOLTAGE AT V_E			0.85	V	+25°C	4.75V	1.25V	2.5mA	16mA	9, 21
A-2	3	"0" OUTPUT VOLTAGE			0.40	V	+25°C	4.75V	1.25V	2.5mA	16mA	9, 20
A-2	4	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	-500μA	-500μA	8, 21
A-2	5	"1" OUTPUT VOLTAGE	2.8			V	+25°C	5.0V	-200μA	0.59V	-500μA	8, 21

Notes:

1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{ac} = 25mV_{rms}. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to V_{cc}.
10. One DC fan-out is defined as 0.8mA.
11. 1 AC fan-out is defined as 50pf.
12. To measure "0" output voltage, apply 2.0V to the input terminals of one of the input AND gates and apply zero volts to the input terminals of the associated input AND gates. Reverse the input conditions and repeat the measurement.
13. To test "0" input current apply 0.4V to terminal under test and apply 5.25V to the remaining terminal of that input AND gate. Apply 5.25V to the input terminals of the associated input AND gates.
14. Expander terminals are left electrically open.
15. To test "1" input current apply 4.5V to one input terminal of the input AND gate and apply zero volts to the other input terminal of that input AND gate. Apply 0V to to the input terminals of the associated input AND gates.
16. To test output "1" power consumption, apply zero volts to both input terminals of each input AND gates.
17. To test input latch voltage rating, apply 10mA to one input terminal of the input AND gate and apply zero volts to the other input terminal of the input AND gate. Apply zero volts to the input terminals of the associated input AND gates.
18. This test guarantees operation free of input latch-up over the specified operating voltage supply range.
19. Manufacturer reserves the right to make design and process changes and improvements.
20. Apply zero volts to the input terminals of the associated input AND gates.
21. Apply 0.8V to the input terminals of the associated input AND gates.
22. Detailed test conditions for AC testing are in Section 3.