BIDIRECTIONAL ONE SHOT

8T20

DIGITAL 8000 SERIES TTL/MSI

DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between ±4mV with respect to the input reference level which may range from -3.2V to +4.2V. For input frequencies up to 8MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_W) is defined by the relationship $t_W = C_X R_X \text{ Log}_e 2$. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

ABSOLUTE MAX RATINGS

Input Voltage

V_{CC}: +7

V_{EE}: -7

APPLICATIONS

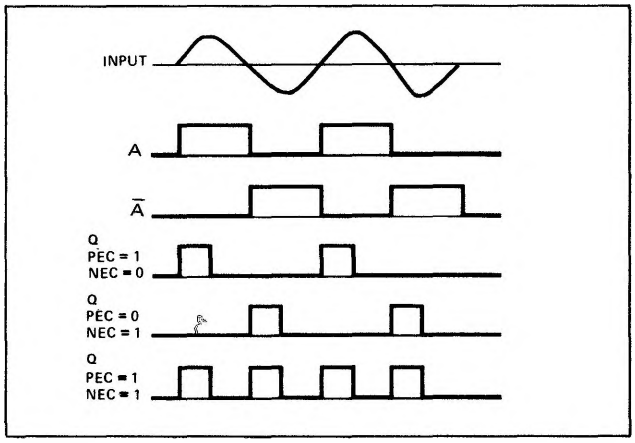
DISC, TAPE AND DRUM READERS

DIGITAL COMMUNICATIONS RECEIVERS

SIGNAL CONDITIONERS

TRANSITION DETECTORS

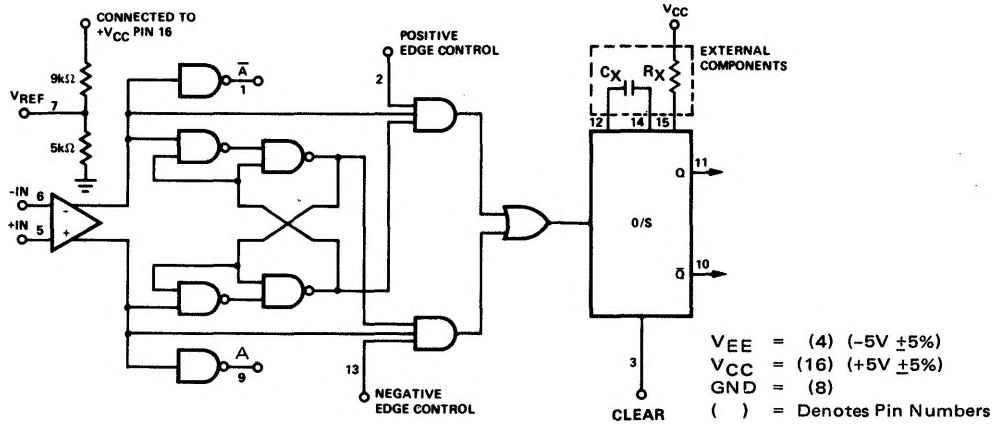
INPUT/OUTPUT WAVEFORMS



FEATURES

- **DIFFERENTIAL INPUT THRESHOLD = ±4mV**
- **PULSE POSITION ERROR = TYPICALLY <3ns**
- **MAX. INPUT FREQUENCY = 8 MHz**
- **TRIGGERS ON POSITIVE AND/OR NEGATIVE TRANSITIONS**

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Temperature Range and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
"1" Output Voltage (All Outputs)	2.6			V	I_{out} = -800uA	7
"0" Output Voltage (All Outputs)			0.4	V	I_{out} = +16mA	8
DIFFERENTIAL INPUTS						
Input Threshold Voltage (V_T)			±4	mV		10
Input Bias Current			125	uA	Figure 5	
Input Offset Current		2		uA		
Common Mode Input Volt, Range	-3.2		+4.2	V		12
DIGITAL INPUTS						
"1" Input Current			40	uA	V_{in} = 4.5V	
"0" Input Current						
PEC. NEC			-2.4	mA	V_{in} = 0.4V	
Clear			-1.6	mA	V_{in} = 0.4V	
Input Latch Voltage	5.5			V	I_{in} = 10mA	9
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6	
Output Pulse Width, Fig. 1	10		40	ns	Rx = 10K, Cx = Open	11
Output Pulse Width, Fig. 3	600		800	ns	Rx = 10K, Cx = 100pf	11
Power Supply Current						
I_{CC}			55	mA	Vcc = +5.25V	
I_{EE}			-20	mA	Vcc = -5.25V	
Short Circuit Current (I_{SO})	-20		-70	mA		

T_A = 25°C, V_{CC} = +5.00V, V_{EE} = -5.00V

CHARACTERISTICS		LIMITS			TEST CONDITIONS	NOTES
	MIN.	TYP.	MAX.	UNITS		
Output Frequency	16			MHz	Fig. 1, f_{in} = 8 MHz	11
Propagation Delay (ton, toff)						
Input to Q, $\overline{Q}$		30	50	ns	Fig. 2	11
Input to A, $\overline{A}$		30	50	ns	Fig. 4	11
Clear to Q, $\overline{Q}$		20	30	ns		

NOTE:

1. All Voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward based.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Output source current is applied through a resistor to ground.
8. Output sink current is supplied through a resistor to Vcc.
9. This test guarantees operation free of Input latch up over the specified operating supply voltage range.
10. The differential input threshold voltage (V_T) is defined as the maximum DC voltage deviation from the reference level necessary to trigger the one-shot.
11. Refer to AC test circuits.
12. Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.

AC TEST CIRCUITS

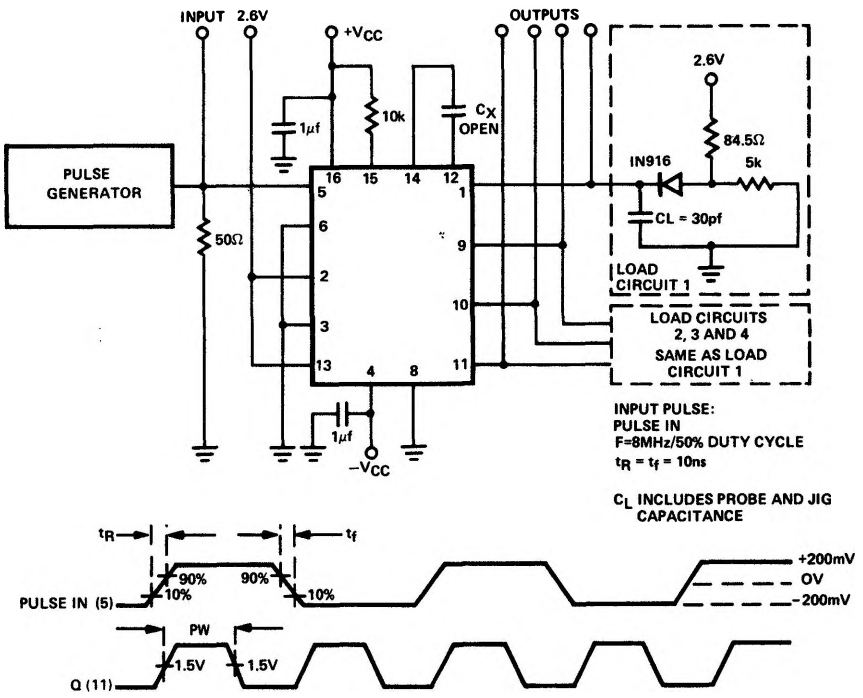


FIGURE 1

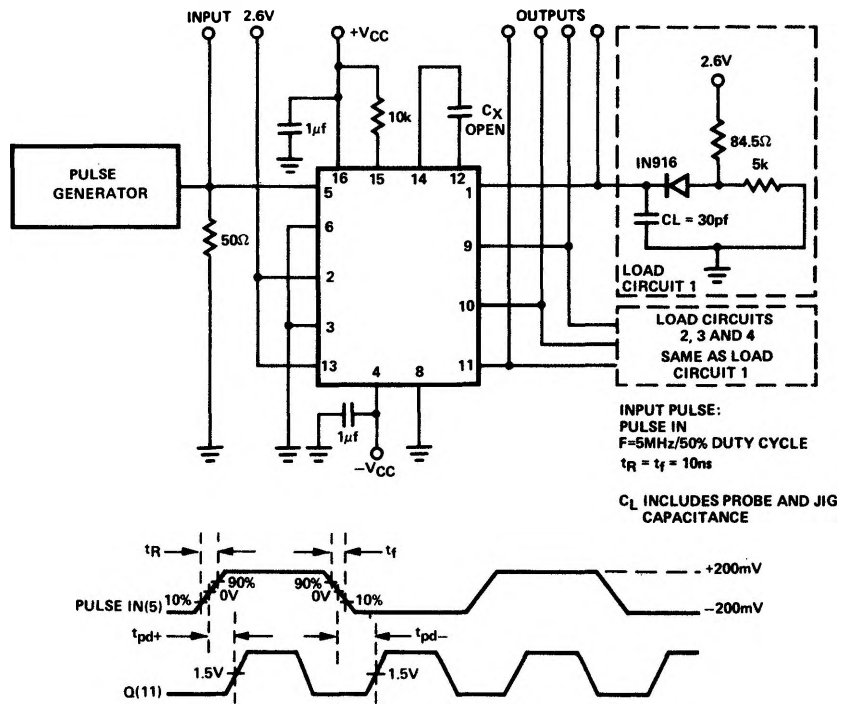


FIGURE 2

AC TEST CIRCUITS (Cont'd)

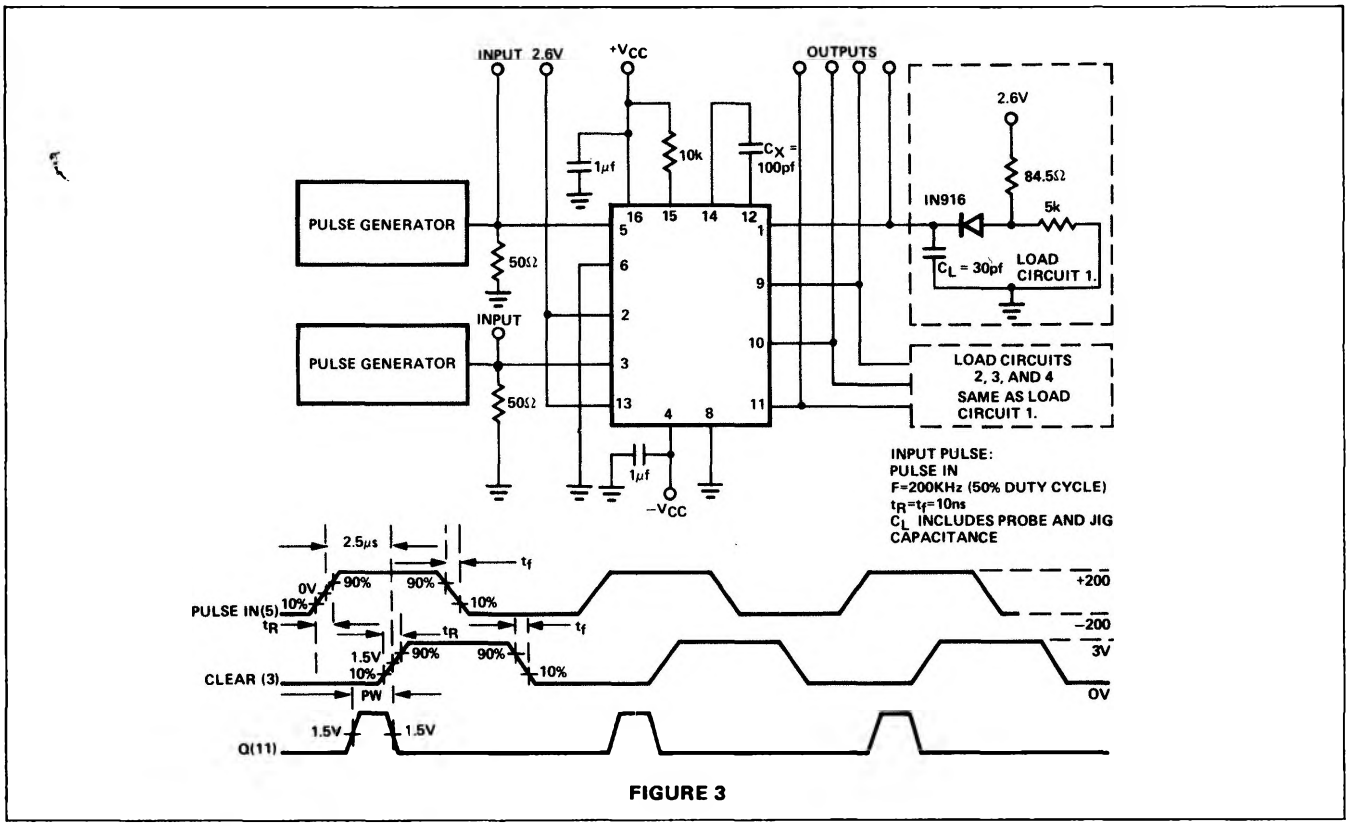


FIGURE 3

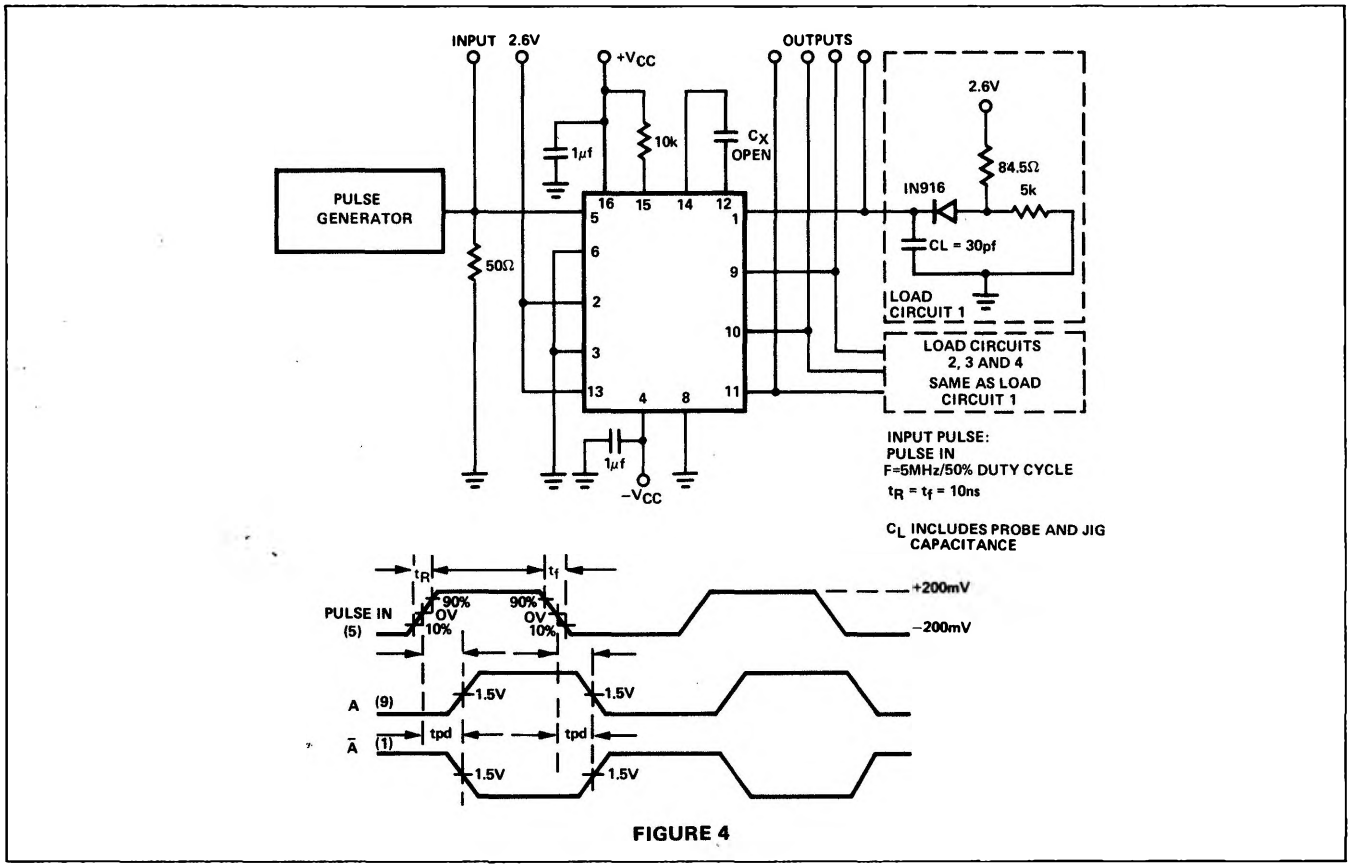


FIGURE 4

INPUT BIAS CURRENT TEST CIRCUIT

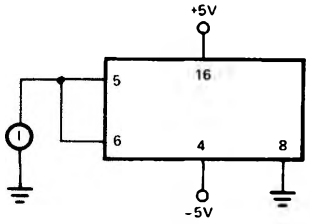


FIGURE 5