OBJECTIVE SPECIFICATION 8X01-A,F

DESCRIPTION

The CRC Generator/Checker circuit is used to provide an error detection capability for serial digital data handling system. The serial data stream is divided by a selected polynomial and the division remainder is transmitted at the end of the data stream, as a Cyclic Redundancy check character (CRCC). When the data is received, the same calculation is performed. If the received message is error-free, the calculated remainder should satisfy a predetermined pattern. In most cases, the remainder is zero except in the case where Synchronous Data Link Control type protocols are used whereby the correct remainder is checked for 1111000010111000 ($x^0 - x^{15}$).

8 polynomials are provided and can be selected via a 3-bit control bus. Popular polynomials such as CRC-16 and CCITT are implemented. Polynomials can be programmed to start with either all zeros or all ones.

Automatic right justification for polynomials of degree less than 16 is provided.

FUNCTIONAL DESCRIPTION

The CRC Generator/Checker circuit provides a means of detecting errors in a serial data communications environment. A binary message can be interpreted as a binary polynomial H(x). This polynomial can be divided by a generator polynomial P(x) such that $H(x) = P(x)\,Q(x) + R(x)$ whereby Q(x) is the quotient and P(x) is the remainder. During transmission, the remainder is appended to the end of the message as check bits. For a given message, a unique remainder is generated. Hardware implementation of division is simply a feedback shift register with Exclusive-OR gating. Subtraction and addition in modulo 2 is implemented by the Exclusive-OR function. The number of shift register stages is equal to the degree of the divisor polynomial.

Table 1 shows the polynomials implemented in the CRC circuit. Each polynomial can be selected via the 3-bit polynomial control inputs S_0, S_1 and S_2. To generate the check bits, the data stream is entered via the Data (D) input, using the high to low transition of the Clock (CP) input. This data is gated with the most significant output (Q) of the register, and controls the exclusive OR gates. The Check Word Enable (CWE) must be held high while the data is being entered. After the last data bit is entered, the CWE is brought low and the check bits are shifted out of the register and appended to the data bits using external gating.

FEATURES

- **I^2L technology**
- **TTL inputs/outputs**
- **10MHz (max) data rate**
- **Total power dissipation = 175mw (max)**
- **V_{CC} = 5.0V**
- **V_{JJ} = 1.0V**
- **Separate preset and reset controls**
- **SDLC specified pattern match**
- **Automatic right justification**

TYPICAL APPLICATIONS

- **Floppy and other disc systems**
- **Digital cassette and cartridge systems**
- **Data communication systems**

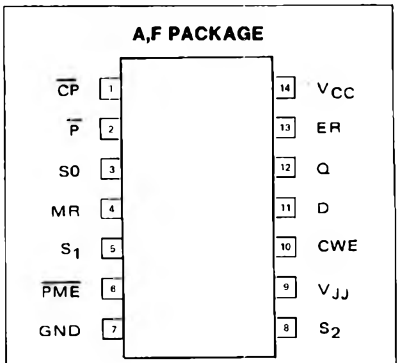
To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held high. The 8X01 is not in the data path, but only monitors the message. The Error output becomes valid after the last check bit has been entered into the 8X01 by a high to low transition of CP. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all low and the Error output (ER) is low. If a detectable error has occurred, ER is high. ER remains valid until the next high to low transition of CP or until the device has been preset or reset. PME must be high if ER output is used to reflect all zero result.

For data communications using the Synchronous Data Link Control protocol (SDLC), the 8X01 is first preset to all ones before any accumulation is done. This applies to both transmitter and receiver.

A special pattern of 1111000010111000 ($x^0 - x^{15}$) is used in place of ali zeros during receiving for valid message check. PME is incorporated to select this option. If PME is low during the last bit time of the message, ER output is low if result matches this special pattern. When ER is high, error has occurred.

PIN CONFIGURATION

A,F PACKAGE



PIN DESIGNATION

PIN NO.	FUNCTION
S_0, S_1, S_2	Polynominal Select inputs
D	Data input
$\overline{CP}$	Clock (operates on high to low transition) input
CWE	Check Word Enable
$\overline{P}$	Preset (active low) input
MR	Master Reset (active high) input
Q	Data output
ER	Error (active high) output
$\overline{PME}$	Pattern match enable (active low)

A high level on the Master Reset (MR) input asynchronously clears the register. A low level on the Preset (P) input asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of the 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

For SDLC, the user must invert the check sum shifted out of the 8X01.

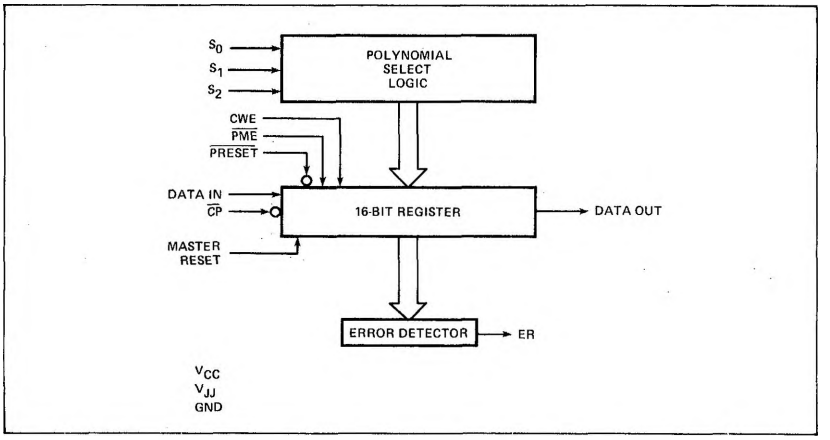
RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{JJ}	Supply current	40		100	mA
$\overline{CP}$	Clock input	0		5	MHz

TRUTH TABLE

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

LOGIC DIAGRAM

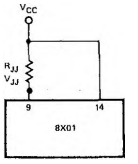


DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp diode voltage	V_{CC} = MIN, I_{IN} = -18mA			-1.5	V
V_{OH}	Output high voltage	V_{CC} = MIN, I_{OH} = -400μA, I_{JJ} = MIN	2.7			V
V_{OL}	Output low voltage	V_{CC} = MIN, I_{OL} = 8mA, I_{JJ} = MIN			0.5	V
I_{IL}	Input low current	V_{CC} = MAX, V_{IN} = 0.4V			-0.36	mA
I_{IH}	Input high current	V_{CC} = MAX, V_{IN} = 2.7V			20	μA
I_{IH}	Max. input current	V_{CC} = MAX			0.1	mA
I_{OS}	Output short circuit current	V_{CC} = MAX, V_{OUT} = OV, I_{JJ} = MIN	-10		-42	mA
I_{CC}	Supply current	V_{CC} = MAX, inputs open	10		18	mA
I_{JJ}	Injection current	V_{CC} = MAX, inputs open	60		100	mA

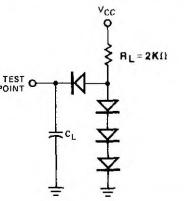
I^2L INJECTOR CURRENT SOURCE



$$R_{JJ} = \frac{V_{CC} - V_{JJ}}{I_{ij}} = \frac{(5.0 - 0.8)\ V}{60mA}$$

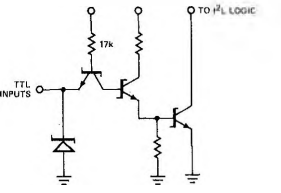
$$= \frac{4.20V}{60mA} = 70\Omega$$

TEST CIRCUIT

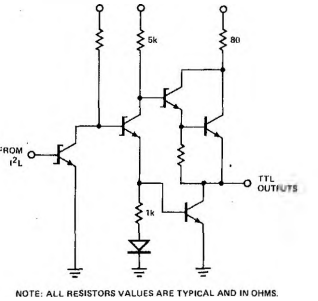


INPUT/OUTPUT CIRCUITS

INPUT STRUCTURE



OUTPUT STRUCTURE



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{max}	Maximum clock frequency				5	7		MHz
	Pulse width							ns
$t_w CP(L)$	Clock low			See Figure 2	100			
$t_w P(L)$	Preset low			See Figure 3	120			
$t_w MR(H)$	Master reset high			See Figure 4	150			
	Setup and hold time							ns
$t_s D$	Setup time	Clock	Data			120	150	
$t_s CWE$	Setup time	Clock	CWE	See Figure 5		75	100	
t_h	Hold time	Clock	Data, CWE		0	-30	0	
	Propagation delay							ns
t_{PLH}	Low to high	Data output	Clock, preset	See Figures 1,2,3		100	160	
t_{PHL}	High to low							
t_{PLH}	Low to high	Data output	MR	See Figure 4		75	100	
t_{PHL}	High to low							
t_{PLH}	Low to high	Error output	Clock, MR, preset	See Figures 2,3,4		150	200	
t_{PHL}	High to low							
t_{REC}	Recovery time	Clock	MR, preset	See Figures 3,4		60	90	ns

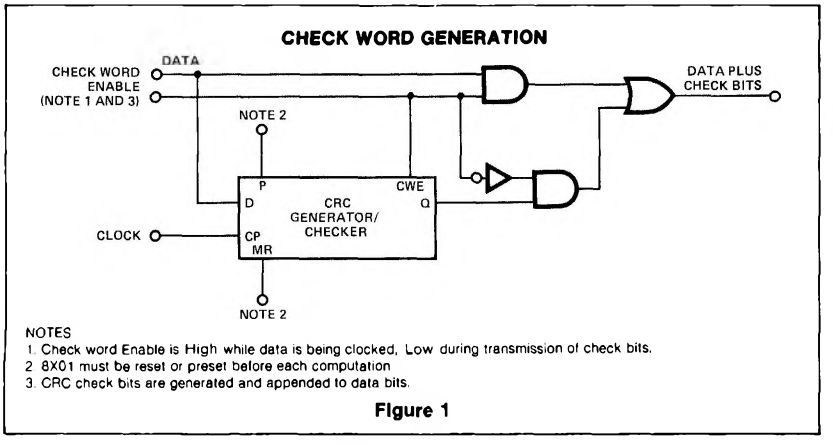


Figure 1

VOLTAGE WAVEFORMS

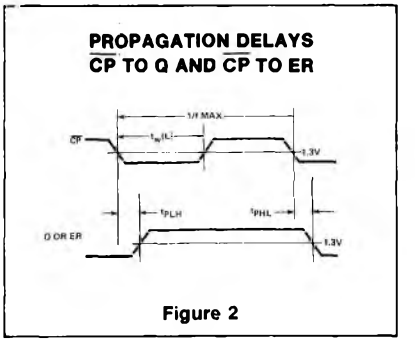


Figure 2

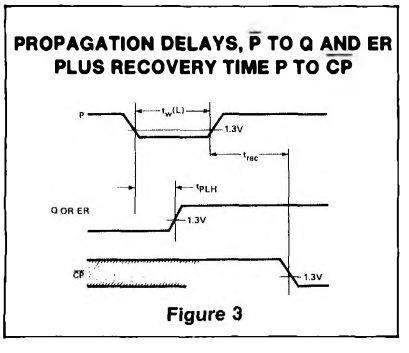


Figure 3

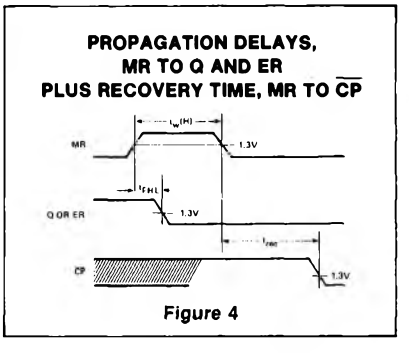


Figure 4

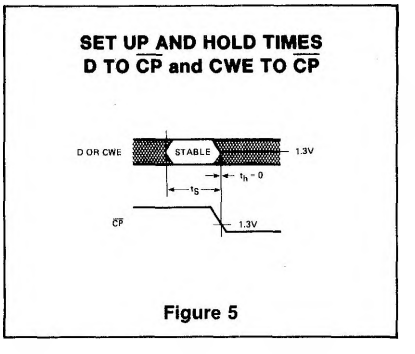


Figure 5