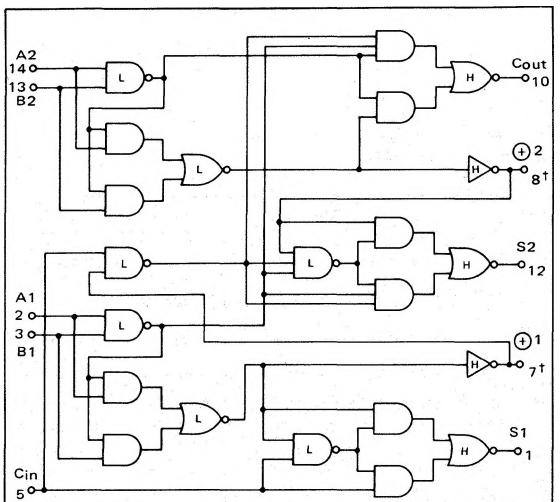
2-BIT FULL ADDER

MC15482L • MC17482L*
MC25482L • MC27482L*

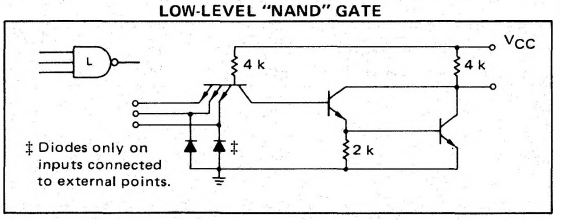


†Available only on MC25482/27482.

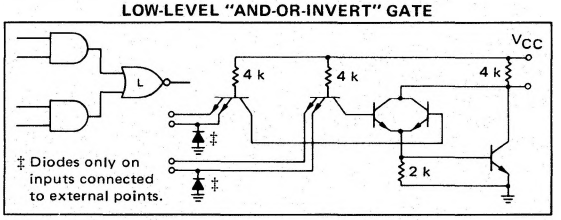
V_{CC} = PIN 4
GND = PIN 11

Input Loading Factor: A, B = 2; C_i = 3
Output Loading Factor = 10
Total Power Dissipation = 165 mW typ/pkg

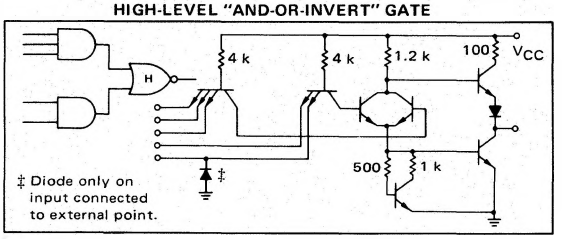
LOW-LEVEL "NAND" GATE



LOW-LEVEL "AND-OR-INVERT" GATE



HIGH-LEVEL "AND-OR-INVERT" GATE



*L suffix = TO-116 ceramic dual in-line package (Case 632).

ADVANCE INFORMATION/NEW PRODUCT

Each bit of this device performs the logical addition of two binary numbers. The sum outputs, the carry output for the second bit, and Exclusive OR outputs for each bit are available. A look-ahead carry is provided internally. The Exclusive OR outputs of the MC25482/MC27482 can be used for look-ahead carry when adding more than two bits.

This device is constructed from low and high-level NAND and AND-OR-INVERT gates as shown in the logic diagram to maximize output drive capability and minimize power dissipation.

TRUTH TABLE

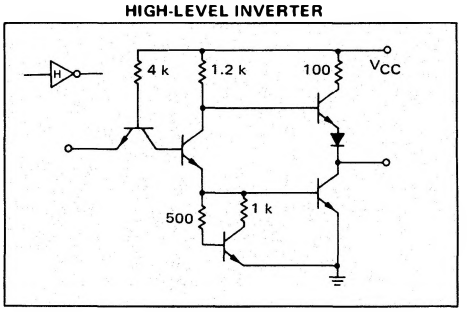
INPUT				OUTPUT							
				C_{in} = 0			C_{in} = 1				
A1	B1	A2	B2	S1	S2	C_o	S1	S2	C_o	⊕1†	⊕2†
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	1	1	0	0	0
0	0	1	0	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0	1	1	1
1	1	1	0	0	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	0	1	1	1
0	1	0	1	1	1	0	0	0	1	1	1
1	1	0	1	0	0	1	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	1	1	1	0
0	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	0	1	1	1	1	1	0	0

†Available only on MC25482/27482.

TYPICAL PROPAGATION DELAY TIMES
T_A = 25°C

	t_{pd-} (ns)				t_{pd+} (ns)			
	OUTPUT				OUTPUT			
INPUT	S1	S2	C_o	⊕	S1	S2	C_o	⊕
B2	–	18.5	–	9.5	–	27	–	14
C_i	5.5	13	9.5	–	9.0	18.5	14	–

HIGH-LEVEL INVERTER



DC ELECTRICAL CHARACTERISTICS

T_A = 0 to +70°C for MC17482 and MC27482
T_A = -55 to +125°C for MC15482 and MC25482

Characteristic	Symbol	Value	Conditions
Input			
Forward Current — A, B	I_F	-3.2 mAdc max	V_{in} = 0.4 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
C_i		-4.8 mAdc max	
Leakage Current — A, B	I_R	80 μAdc max	V_{in} = 2.4 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
C_i		120 μAdc max	
A, B, C_i		1.0 mAdc max	V_{in} = 5.5 Vdc, V_{CC} = 5.5 Vdc ① or 5.25 Vdc ②
Threshold Voltage	V_{th} "1"	2.0 Vdc	
	V_{th} "0"	0.8 Vdc	
Output			
Output Voltage	V_{OL}	0.4 Vdc max	I_{OL} = 16 mAdc, V_{CC} = 4.5 Vdc ① or 4.75 Vdc ② — Tested according to truth table. Logical "1" = V_{th} "0"; Logical "0" = V_{th} "1".
	V_{OH}	2.4 Vdc min	I_{OH} = -400 μAdc, V_{CC} = 4.5 Vdc ① or 4.75 Vdc ② — Tested according to truth table. Logical "1" = V_{th} "0"; Logical "0" = V_{th} "1".
Short-Circuit Current	I_{SC}	① -20 to -57 mAdc ② -18 to -57 mAdc	V_{CC} = 5.5 Vdc, output grounded. Tested according to truth table. Logical "1" = 4.5 Vdc; Logical "0" = Gnd.

① MC15482, MC25482
② MC17482, MC27482