ACS10MS

Radiation Hardened Triple Three-Input NAND Gate

April 1995

Features

- **1.25 Micron Radiation Hardened SOS CMOS**
- **Total Dose 300K RAD (Si)**
- **Single Event Upset (SEU) Immunity <1 x 10^{-10} Errors/Bit-Day (Typ)**
- **SEU LET Threshold >80 MEV-cm^2/mg**
- **Dose Rate Upset >10^{11} RAD (Si)/s, 20ns Pulse**
- **Latch-Up Free Under Any Conditions**
- **Military Temperature Range: -55°C to +125°C**
- **Significant Power Reduction Compared to ALSTTL Logic**
- **DC Operating Voltage Range: 4.5V to 5.5V**
- **Input Logic Levels**
  - **VIL = 30% of VCC Max**
  - **VIH = 70% of VCC Min**
- **Input Current ≤1μA at VOL, VOH**

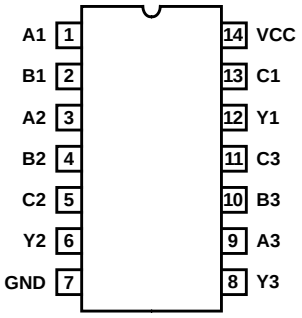
Description

The Intersil ACS10MS is a radiation hardened triple three-input NAND gate. A high on all inputs forces the output to a low state.

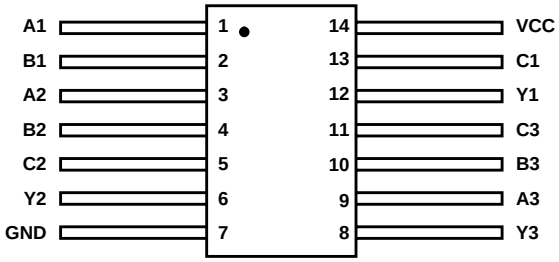
The ACS10MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

Pinouts

14 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



Ordering Information

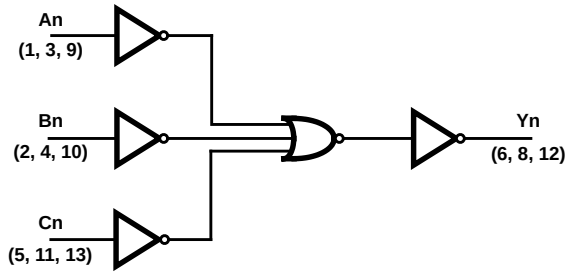
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
ACS10DMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead SBDIP
ACS10KMSR	-55°C to +125°C	Intersil Class S Equivalent	14 Lead Ceramic Flatpack
ACS10D/Sample	+25°C	Sample	14 Lead SBDIP
ACS10K/Sample	+25°C	Sample	14 Lead Ceramic Flatpack
ACS10HMSR	+25°C	Die	Die

Truth Table

INPUTS			OUTPUT
An	Bn	Cn	Yn
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTE: L = Logic Level Low, H = Logic Level High

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Spec Number **518814**
File Number **3630**

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (Soldering 10s) . . . . . $+265^oC$
Junction Temperature (TJ) . . . . . $+175^oC$
ESD Classification . . . . . Class 1
(All Voltages Reference to VSS)

Reliability Information

Thermal Impedance	θ_{JA}	θ_{JC}
DIP	$74^oC/W$	$24^oC/W$
Flatpack	$116^oC/W$	$30^oC/W$

Maximum Package Power Dissipation at $+125^oC$
DIP 0.7W
Flatpack 0.4W
Maximum Device Power Dissipation . . . . . (TBD)W
Gate Count . . . . . 42 Gates

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$
Input High Voltage (VIH) . . . . . VCC to 70% of VCC
Input Low Voltage (VIL) . . . . . 0V to 30% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	5	µA
			2, 3	$+125^oC$, -55^oC	-	100	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	$+25^oC$	-12	-	mA
			2, 3	$+125^oC$, -55^oC	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	$+25^oC$	12	-	mA
			2, 3	$+125^oC$, -55^oC	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50µA	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	$+25^oC$	-	±0.5	µA
			2, 3	$+125^oC$, -55^oC	-	±1.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 3)	7, 8A, 8B	$+25^oC$, $+125^oC$, -55^oC	-	-	V

NOTE:

1. All voltages referenced to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests, VO ≥4.0V is recognized as a logic "1", and VO ≤0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	13	ns
			10, 11	+125°C, -55°C	2	16	ns
	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	12	ns
			10, 11	+125°C, -55°C	2	15	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS			UNITS
					MIN	TYP	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	30	-	pF
				+125°C	-	32	-	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	-	10	pF
				+125°C	-	-	10	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMP	RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	100	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 2)	+25°C	-	-	V
Propagation Delay Input to Output	TPHL	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	16	ns
	TPLH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	15	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥4.0V is recognized as a logic “1”, and VO ≤0.5V is recognized as a logic “0”.

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	(NOTE 1) DELTA LIMIT	UNITS
Supply Current	ICC	±1.0	µA
Output Current	IOL/IOH	±15	%

NOTE:

1. All delta calculations are referenced to 0 hour readings or pre-life readings.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 1 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 2 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test 3 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate Group A testing may be exercised in accordance with MIL-STD-883, Method 5005.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUP	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < TA < 139°C)

OPEN	GROUND	1/2 VCC = 3V ±0.5V	VCC = 6V ±0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN 1 (Note 1)					
-	1, 2, 3, 4, 5, 7, 9, 10, 11, 13	6, 8, 12	14	-	-
STATIC BURN-IN 2 (Note 1)					
-	7	6, 8, 12	1, 2, 3, 4, 5, 9, 10, 11, 13, 14	-	-
DYNAMIC BURN-IN (Note 1)					
-	7	6, 8, 12	14	1, 2, 3, 4, 5, 9, 10, 11, 13	-

NOTE:

1. Each pin except VCC and GND will have a series resistor of 500Ω ±5% for static burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS (TA = +25°C, ±5°C)

FUNCTION	OPEN	GROUND	VCC = 5V ±0.5V
Irradiation Circuit (Note 1)	6, 8, 12	7	1, 2, 3, 4, 5, 9, 10, 11, 13, 14

NOTE:

1. Each pin except VCC and GND will have a series resistor of 47kΩ ±5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Intersil - Space Products MS Screening

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C (-65^{o} to $+150^{o}$C)

100% Constant Acceleration

100% PIND Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In 1 Method 1015, 24 Hours at $+125^{o}$C Min

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2 Method 1015, 24 Hours at $+125^{o}$C Min

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In Method 1015, 240 Hours at $+125^{o}$C or 180 Hours at $+135^{o}$C

100% Interim Electrical Test 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

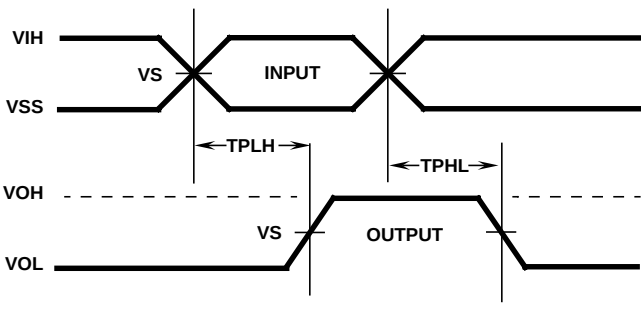
CSI and/or GSI (Optional) (Note 2)

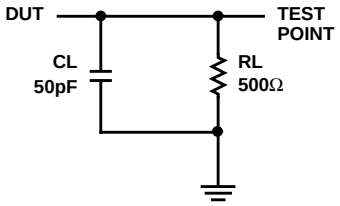
Data Package Generation (Note 3)

NOTES:

1. Failures from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Intersil Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include reproductions of SEM photos. NOTE: SEM photos to include percent of step coverage.
   X-Ray Report and Film, including penetrometer measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, RAD Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Intersil.

Propagation Delay Timing Diagram and Load Circuit





AC VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:

88 mils x 88 mils
2,240mm x 2,240mm

METALLIZATION:

Type: AlSiCu
Metal 1 Thickness: 6.75kÅ (Min), 8.25kÅ (Max)
Metal 2 Thickness: 9kÅ (Min), 11kÅ (Max)

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

DIE ATTACH:

Material: Silver Glass or JM 7000 after 7/1/95

WORST CASE CURRENT DENSITY:

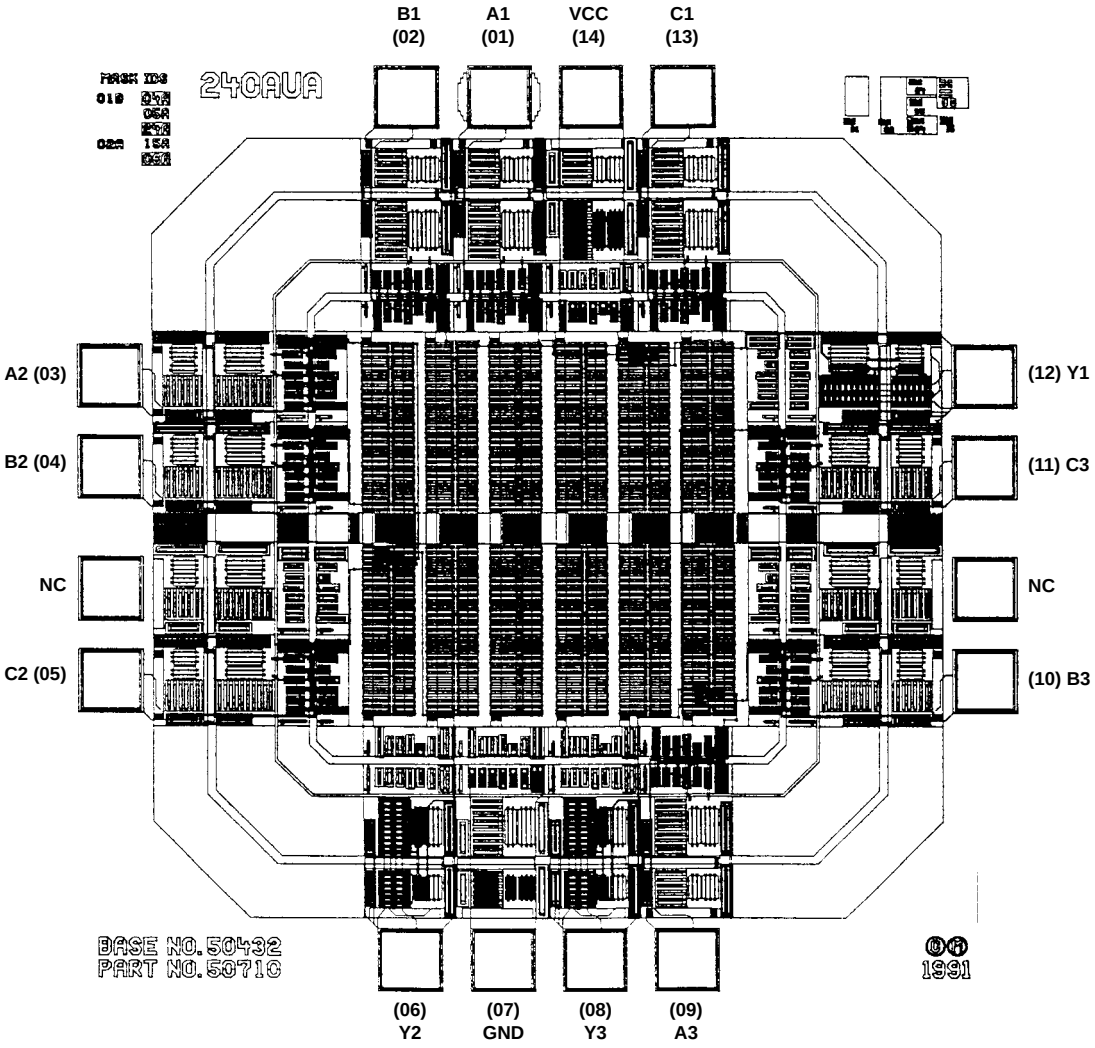
< 2.0 x 10^5A/cm^2

BOND PAD SIZE:

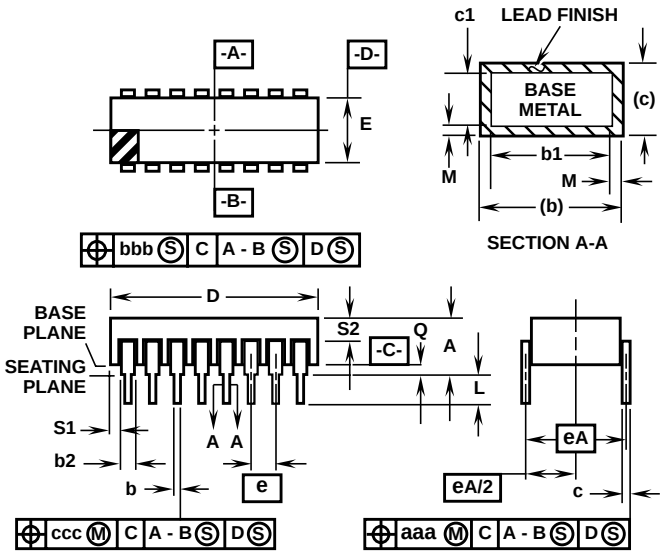
> 4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout

ACS10MS



Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D14.3 **MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)**
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

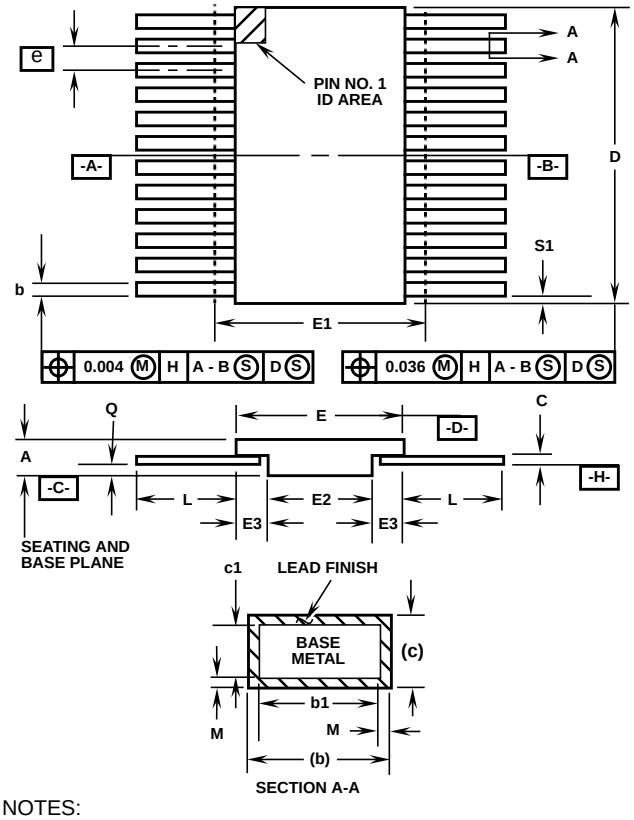
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A **MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)**
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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