192kHz STEREO ASYNCHRONOUS SAMPLE RATE CONVERTER

AD1896

PRELIMINARY TECHNICAL DATA

FEATURES

Patents Pending

Automatically Senses Sample Frequencies
No Programming Required
Attenuates Sample Clock Jitter
3-5V Input and 3.3V Core Supply Voltages
Accepts 16/18/20/24-Bit Data
1kHz to 192kHz Sample Rate Range
Input/Output Sample Ratios from 7.75:1 to 1:8
Bypass Mode
Multiple AD1896 TDM Daisy Chain Mode
Multiple AD1896 Matched Phase Mode
139 dB Signal-to-Noise and Dynamic Range (A-Weighted, 20-20kHz BW)
120 dB THD+N minimum for all sample rates and input frequencies
Linear Phase FIR Filter
Hardware Controllable Soft Mute
Supports 256xF_S, 512xF_S or 768xF_S Master Mode Clock
Flexible Three wire Serial Data Port with Left-Justified, I^2S, Right-Justified (16,18,20,24-Bits) and DSP Serial Port Modes
Master/Slave Input and Output Modes
28 Lead SSOP Plastic Package

APPLICATIONS

Home Theater Systems, Studio Digital Mixers, Automotive Audio Systems, DVD, Set-top Boxes, Digital Audio Effects Processors, Studio to Transmitter Links, Digital Audio Broadcast Equipment, Digital TapeVarispeed Applications

PRODUCT OVERVIEW

The AD1896 is a 24-bit, high-performance, single-chip, second-generation asynchronous sample rate converter. Based upon Analog Devices Inc. experience with its first asynchronous sample rate converter, the AD1890, the AD1896 offers improved performance and additional features. This improved performance includes a minimum THD+N of 120dB for all input frequencies and sample rates, 139 dB dynamic range, 192 kHz sampling frequencies for both input and output sample rates, improved jitter rejection and 1:8 up-sampling and 7.75:1 down-sampling ratios. Additional features include more serial formats, a bypass mode, better interfacing to digital signal processors and a phase matching mode.

The AD1896 has a 3 wire interface for the serial input and output ports that supports Left-Justified, I^2S and Right-Justified (16,18,20,24-Bit) modes. Additionally, the serial output port supports TDM mode for daisy chaining multiple AD1896's to a digital signal processor. The serial output data is dithered down to 20, 18 or 16 bits when 20,18 or 16 bit output data is selected. The AD1896 sample rate converts the data from the serial input port to the sample rate of the serial output port. The sample rate at the serial input port can be asynchronous with respect to the output sample rate of the output serial port. The master clock to the AD1896, MCLK, can be asynchronous to both the serial input and output ports.

MCLK can either be generated off chip or on chip by the AD1896 master clock oscillator. Since MCLK can be asynchronous to the input or output serial ports, a crystal can be used to generate MCLK internally to reduce noise and EMI emissions on the board. When MCLK is synchronous to either the output or input serial port, the AD1896 can be configured in a master mode where MCLK is divided down and used to generate the left/right and bit clocks for the serial port that is synchronous to MCLK. The AD1896 supports master modes of 256xFs, 512xFs and 768xFs for both input and output serial ports.

Conceptually, the AD1896 interpolates the serial input data by a rate of 2^{20} and samples the interpolated data stream by the output sample rate. In practice a 64 tap FIR filter with 2^{20} polyphases, a FIFO, a digital servo loop that measures the time difference between

input and output samples within 5 ps and a digital circuit to track the sample rate ratio are used to perform the interpolation and output sampling. Refer to the section titled “Theory of Operation”. The digital servo loop and sample rate ratio circuit automatically track the input and output sample rates.

The digital servo loop measures the time difference between input and output sample rates within 5 ps. This is necessary in order to select the correct polyphase filter coefficient The digital servo loop has excellent jitter rejection for both input and output sample rates as well as the master clock. The jitter rejection begins at less than one herz. This requires a long settling time whenever RESET is deasserted or when the input or output sample rate changes. To reduce the settling time, upon deassertion of RESET or a change in a sample rate the digital servo loop enters the fast settling mode. When the digital servo loop has adequately settled in the fast mode, it switches into the normal or slow settling mode and settles some more until the time difference measurement between input and output sample rates is within 5ps. During fast mode the MUTE_OUT signal is asserted high. Normally, the MUTE_OUT is connected to the MUTE_IN pin. The MUTE_IN signal is used to softly mute the AD1896 upon assertion and softly unmute the AD1896 when it is deasserted.

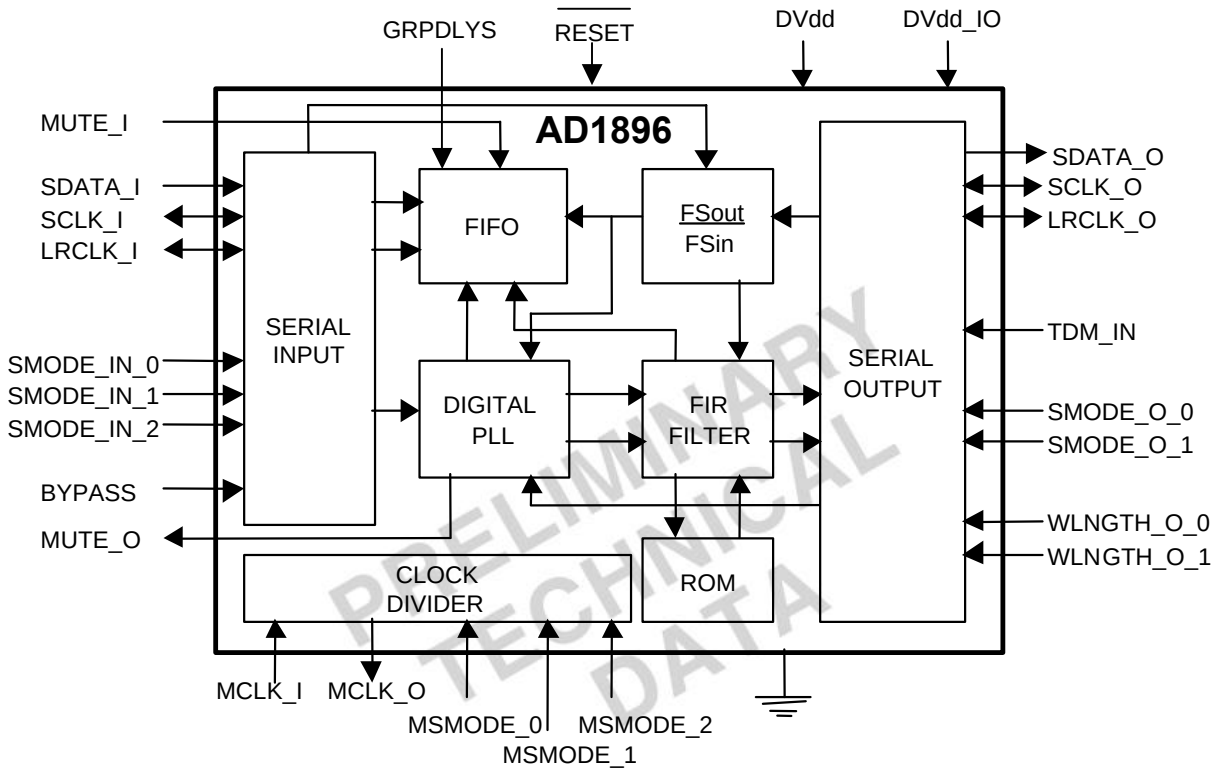
The sample rate ratio circuit is used to scale the filter length of the FIR filter for decimation. Hysteresis in measuring the sample rate ratio is used to avoid oscillations in the scaling of the filter length, which would cause distortion on the output. However, when multiple AD1896’s are used with the same serial input port clock and the same serial output port clock, the hyteresis causes different group delays between multiple AD1896’s. A phase matching mode feature was added to the AD1896 to address this problem. In phase matching mode one AD1896, the master, transmits its sample rate ratio to the other AD1896’s, the slaves, so that the group delay between the multiple AD1896’s remains the same.

The group delay of the AD1896 can be adjusted for short or long delay. An address offset is added to the write pointer of the FIFO in the sample rate converter. This offset is set to 16 for short delay and 64 for long delay. In long delay the group delay is effectively increased by 48 input sample clocks.

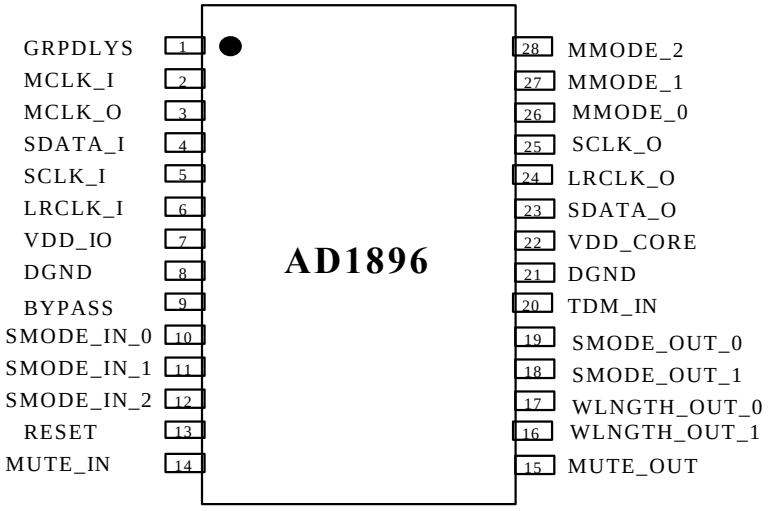
The sample rate converter of the AD1896 can be bypassed altogether using the bypass mode. In bypass mode the AD1896’s serial input data is passed directly to the serial output port without any dithering. This is useful for passing through non-audio data or when the input and output sample rates are synchronous to one another and the sample rate ratio is exactly 1 to 1.

The AD1896 is a +3.3 volt, +5V input tolerant part and is available in a 28-lead SSOP SMD package. The AD1896 is 5 volt input tolerant only when the VDD_IO supply pin is supplied with 5 volts.

AD1896 BLOCK DIAGRAM



AD1896 PIN OUT: PACKAGE, 28-LEAD SSOP (RS-28)



TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages (DV_{DD})	+3.3V
Vdd_IO	+3.3 or 5V
Ambient Temperature	$25^{O}C$
Input Clock	33MHz, (512xFs Mode)
Input Signal	1.000kHz, 0dBFS (Full Scale)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20kHz
Word Width	20 bits
Load Capacitance	50 pF
Input Voltage HI	2.4 V
Input Voltage LO	0.8 V

Values in **bold** typeface are tested, all others are guaranteed, not tested.

DIGITAL PERFORMANCE ($0°C<T_A<70°C$, DVdd = 3.3V±10%, 8MHz<MCLK<33MHz)

PARAMETER	Min	Typ	Max	Units
Resolution		24		Bits
Dynamic Range (20 Hz to 20 kHz, 1kHz, -60 dB Input) No Filter				
44.1kHz:48kHz		136		dB
48kHz:96kHz		136		dB
96kHz:48kHz		133		dB
48kHz:192kHz		135		dB
192kHz:32kHz		124		dB
Total Harmonic Distortion + Noise (20 Hz to 20 kHz, 1kHz, 0 dB Input) No Filter				
44.1kHz:48kHz		-124		dB
48kHz:96kHz		-132		dB
96kHz:48kHz		-132		dB
48kHz:192kHz		-132		dB
192kHz:32kHz		-127		dB
Interchannel Gain Mismatch		0.0		dB
Interchannel Phase Deviation		0.0		Degrees
Mute Attenuation (24 bit)		-144		dB

DIGITAL FILTERS (FSin/FSout=1, $0°C<T_A<70°C$, DVdd = 3.3V±10%, 8MHz<MCLK<30MHz)

FIR FILTER	MIN	TYPICAL	MAX	UNITS
Pass Band			0.4535Fs	Hz
Pass Band Ripple			±0.00xx	dB
Transition Band	0.4535Fs		0.5465Fs	Hz
Stop Band	0.5465Fs			Hz
Stop Band Attenuation	142			dB
Group Delay		nnn/Fs		μs

DIGITAL TIMING (0°C<T_A<70°C, DVdd = 3.3V±10%, 8MHz<MCLK<33MHz)

PARAMETER*		MIN	MAX	UNITS
t_{MCLKI}	MCLK_I Period	33.3	125	ns
f_{MCLKI}	MCLK_I Frequency	8.0	33.0	MHz
t_{MPWH}	MCLK_I Pulse Width High		TBD	ns
t_{MPWL}	MCLK_I Pulse Width Low		TBD	ns
t_{MCLKO}	MCLK_O Period		TBD	ns
f_{MCLKO}	MCLK_O Frequency		TBD	MHz
t_{LRIS}	LRCLK_I Setup to SCLK_I		TBD	ns
t_{LROS}	LRCLK_O Setup to SCLK_O (All Modes)		TBD	ns
t_{LROH}	LRCLK_O Hold from SCLK_O (TDM mode only)		TBD	ns
t_{DIS}	SDATA_I Setup to SCLK_I		TBD	ns
t_{DIH}	SDATA_I Hold from SCLK_I		TBD	ns
t_{DOPD}	SDATA_O Propagation delay from SCLK_O		TBD	ns
t_{DOH}	SDATA_O Valid from SCLK_O		TBD	ns
t_{SIH}	SCLK_I Pulse Width High		TBD	ns
t_{SIL}	SCLK_I Pulse Width Low		TBD	ns
t_{SOH}	SCLK_O Pulse Width High		TBD	ns
t_{SOL}	SCLK_O Pulse Width Low		TBD	ns
t_{LROH}	LRCLK_O Pulse Width High (TDM Mode Only)		TBD	ns
t_{LROL}	LRCLK_O Pulse Width Low (TDM Mode Only)		TBD	ns
f_{SCLKI}	SCLK_I Frequency With xMHz Clock		TBD	MHz
f_{SLCKO}	SCLK_O Frequency With xMHz Clock		TBD	MHz
f_{LRI}	LRCLK_I Frequency With xMHz Clock		TBD	MHz
f_{LRO}	LRCLK_O Frequency With xMHz Clock		TBD	MHz
t_{PDRP}	RESET Pulse Width HI		TBD	ns
t_{PDRS}	RESET Setup to MCLK_I		TBD	ns

* Refer to timing diagrams

DIGITAL I/O CHARACTERISTICS (0°C<T_A<70°C, DVdd = 3.3V±5%, MCLK=30MHz)

PARAMETER	MIN	TYP	MAX	UNITS
Input Voltage HI (V_{IH})	2.0			V
Input Voltage LO (V_{OH})			0.8	V
Input Leakage (I_{IH}@V_{IH}=3.5V)			100	µA
Input Leakage (I_{IL}@V_{IL}=0.8V)			100	µA
Input Capacitance		5	10	pF
Output Voltage HI (V_{OH}@I_{OH} = -200:A)	DV_{DD}-0.5	DV_{DD}-0.4		V
Output Voltage LO (V_{OL}@I_{OL}= 4mA)		0.2	0.5	V
Output Source Current HI (I_{OH})			??	mA
Output Sink Current LO(I_{OL})			??	mA

POWER SUPPLIES (0°C<T_A<70°C, DVdd = 3.3V±10%, MCLK=33MHz)

PARAMETER	MIN	TYP	MAX	UNITS
Supplies:				
Voltage (VDD_CORE)	3.0	3.3	3.5	V
Current (I_ CORE)				
48kHz:48kHz		20		mA
96kHz:96kHz		26		mA
192kHz:192kHz		43		mA

Current - Power-Down		TBD		mA
Power Dissipation: Operational				
48kHz:48kHz		65		mW
96kHz:96kHz		85		mW
192kHz:192kHz		132		mW
Power-Down		TBD		mW

TEMPERATURE RANGE

PARAMETER	MIN	TYP	MAX	UNITS
Specifications Guaranteed		25		°C
Functionality Guaranteed	-40		+105	°C
Storage	-55		125	°C
Thermal Resistance, 2_{JA}		TBD		°C/W

ABSOLUTE MAXIMUM RATINGS *

PARAMETER	MIN	MAX	UNITS
Power Supplies:			
Digital Core (DVdd)	-0.3	3.6	V
Digital IO (DV_{IO})	-0.3	6.0	V
Digital Inputs:			
Input Current		±20	mA
Input Voltage	DGND-0.3	DV_{IO}+0.3	V
Ambient Temperature (Operating)	-25	+70	°C
ESD Tolerance (Human Body Model, Method 3015.2, MIL-STD-883B)	1		kV

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
AD1896-ARS	-25°C to +85°C	28-Lead SSOP	Tube
AD1896-ARSRL	-25°C to +85°C	28-Lead SSOP	Reel

PIN FUNCTION DESCRIPTIONS

PIN	IN/OUT	PIN NAME	DESCRIPTION
1	IN	GRPDLYS	Group Delay HI=Short, LO=Long
2	IN	MCLK_IN	Master Clock or Crystal Input (33MHz)
3	OUT	MCLK_OUT	Master Clock output or Crystal Output
4	IN	SDATA_I	Input Serial Data (at Input Sample Rate)
5	IN/OUT	SCLK_I	Master/Slave Input Serial Bit Clock
6	IN/OUT	LRCLK_I	Master/Slave Input Left/Right Clock
7	IN	VDD_IO	3V/5V Input/Output Digital Supply Pin
8	IN	DGND	Digital Ground Pin
9	IN	BYPASS	ASRC Bypass Mode, Active High
10	IN	SMODE_IN_O	Input Port Serial Interface Mode Select Pin 0
11	IN	SMODE_IN_1	Input Port Serial Interface Mode Select Pin 1
12	IN	SMODE_IN_2	Input Port Serial Interface Mode Select Pin 2
13	IN	RESET	Reset Pin, Active Low
14	IN	MUTE_IN	Soft Mute Input Pin – Normally Connected to MUTE_OUT
15	OUT	MUTE_OUT	Output Mute Control – FIFO Pointer Overrun
16	IN	WLNGTH_OUT_1	Hardware Selectable Output Wordlength - Select Pin 1
17	IN	WLNGTH_OUT_0	Hardware Selectable Output Wordlength - Select Pin 0
18	IN	SMODE_OUT_1	Output Port Serial Interface Mode Select Pin 1
19	IN	SMODE_OUT_0	Output Port Serial Interface Mode Select Pin 0
20	IN	TDM_DATA_IN	Daisy Chain Mode, Serial Data Input. Ground when not used
21	IN	DGND	Digital Ground Pin
22	IN	VDD_CORE	3.3V Digital Supply Pin
23	OUT	SDATA_O	Output Serial Data (at Output Sample Rate)
24	IN/OUT	LRCLK_O	Master/Slave Output Left/Right Clock
25	IN/OUT	SCLK_O	Master/Slave Output Serial Bit Clock
26	IN	MMODE_0	Master/Slave Clock Ratio Mode Select Pin 0
27	IN	MMODE_1	Master/Slave Clock Ratio Mode Select Pin 1
28	IN	MMODE_2	Master/Slave Clock Ratio Mode Select Pin 2

ASRC FUNCTIONAL OVERVIEW

THEORY OF OPERATION

Asynchronous sample rate conversion is converting data from one clock source at some sample rate to another clock source at the same or different sample rate. The simplest approach to asynchronous sample rate conversion is the use of a zero-order hold between two samplers shown in figure 1. In an asynchronous system T2 is never equal to T1 nor is the ratio between T2 and T1 rational. As a result samples at FS_OUT will be repeated or dropped producing an error in the resampling process. The frequency domain shows the wide side lobes that result from this error when the sampling of FS_OUT is convolved with the attenuated images from the sin(x)/x nature of the zero-order hold. The images at FS_IN, DC signal images, of the zero-order hold are infinitely attenuated. Since the ratio of T2 to T1 is an irrational number, the error resulting from the resampling at FS_OUT can never be eliminated. However, the error can be significantly reduced through interpolation of the input data at FS_IN. The AD1896 is conceptually interpolated by a factor of 2^{20}.

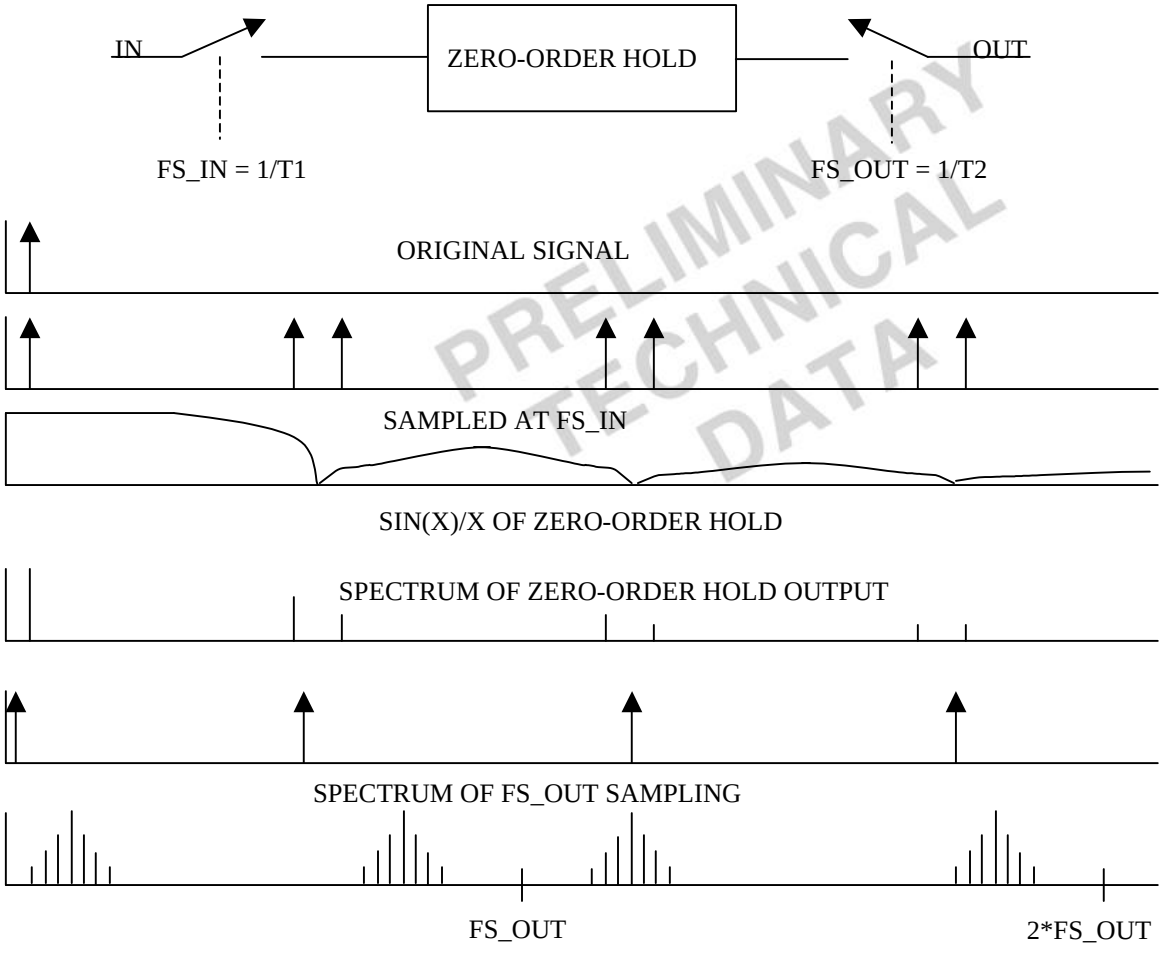


Figure 1. Zero-Order Hold being used by FS_OUT to resample data from FS_IN.

The Conceptual High Interpolation Model

Interpolation of the input data by a factor of 2^{20} involves placing (2^{20}-1) samples between each FS_IN sample. Figure 2 shows both the time domain and the frequency domain of interpolation by a factor of 2^{20}. Conceptually, interpolation by 2^{20} would involve the steps of zero-stuffing (2^{20} –1) number of samples between each FS_IN sample and convolving this interpolated signal with a digital lowpass filter to suppress the images. In the time domain it can be seen that FS_OUT selects the closest FS_IN*2^{20} sample from the zero-order hold as opposed to the nearest FS_IN sample in the case of no interpolation. This significantly reduces the resampling error.

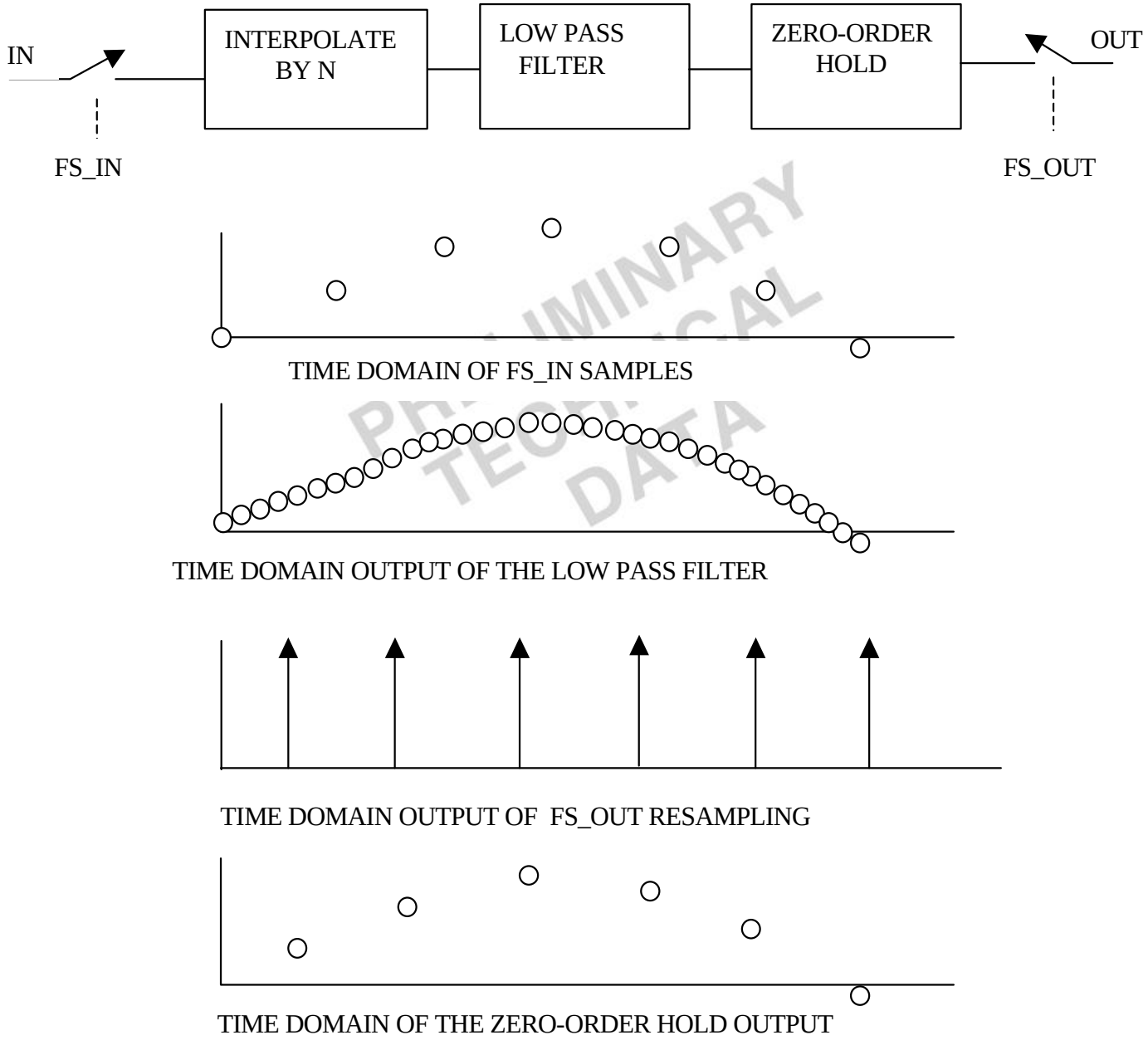


Figure 2. Time Domain of the Interpolation and Resampling.

In the frequency domain shown in figure 3 the interpolation expands the frequency axis of the zero-order hold. The images from the interpolation can be sufficiently attenuated by a good low pass filter. The images from the zero-order hold are now pushed by a factor of 2^{20} closer to the infinite attenuation point of the zero-order hold, which is FS_IN*2^{20}. The images at the zero-order hold are the determining factor for the fidelity of the output at FS_OUT. The worst case images can be computed from the zero-order hold frequency response, maximum image =

sin(π*F/FS_INTERP)/(π*F/FS_INTERP). F is the frequency of the worst case image which would be 2^{20}*FS_IN +/- FS_IN/2 , and FS_INTERP is FS_IN*2^{20}.

The following worst case images would appear for FS_IN=192kHz:

Image at FS_INTERP – 96kHz = -125.1 dB
Image at FS_INTERP + 96kHz = -125.1 dB

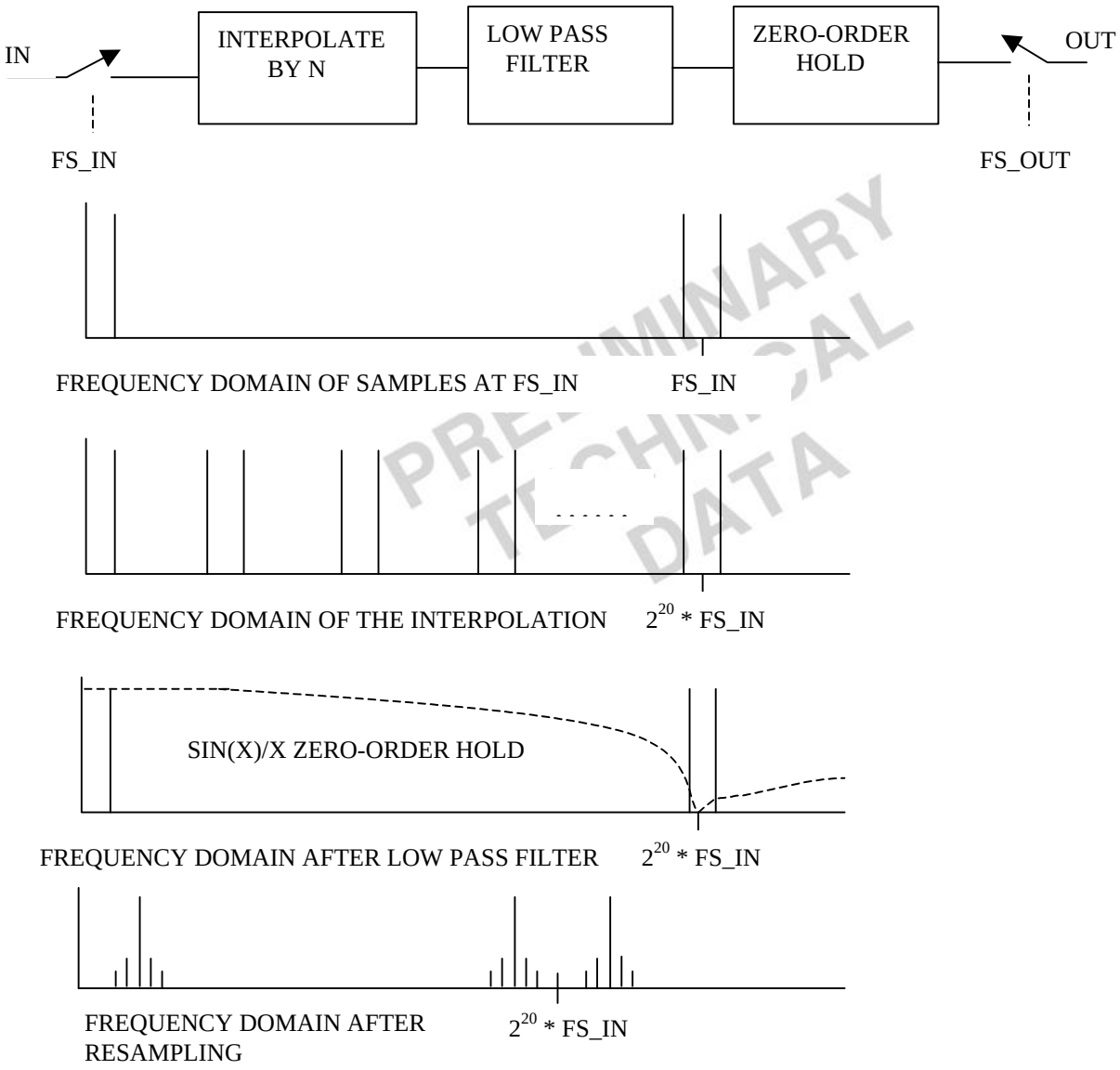


Figure 3. Frequency Domain of the Interpolation and Resampling.

Hardware Model

The output rate of the low pass filter of figure 2 would be the interpolation rate, 2^{20} * 192000 kHz = 201.3 GHz. Sampling at a rate of 201.3 GHz is clearly impractical not to mention the number of taps required to calculate each interpolated sample. However, since interpolation by 2^{20} involves zero-stuffing 2^{20}-1 samples between each FS_IN sample, most of the multiplies in the low pass FIR filter are by zero. A further reduction can be realized by the fact that

since only one interpolated sample is taken at the output at the FS_OUT rate, only one convolution needs to be performed per FS_OUT period instead of 2^{20} convolutions. A 64 tap FIR filter for each FS_OUT sample is sufficient to suppress the images caused by the interpolation.

The difficulty with the above approach is that the correct interpolated sample needs to be selected upon the arrival of FS_OUT. Since there are 2^{20} possible convolutions per FS_OUT period, the arrival of the FS_OUT clock must be measured with an accuracy of 1/201.3 GHz = 4.96 ps. Measuring the FS_OUT period with a clock of 201.3 GHz frequency is clearly impossible, instead, several coarse measurements of the FS_OUT clock period are made and averaged over time.

Another difficulty with the above approach is the number of coefficients required. Since there are 2^{20} possible convolutions with a 64 tap FIR filter, there needs to be 2^{20} polyphase coefficients for each tap, which requires a total of 2^{26} coefficients. To reduce the amount of coefficients in ROM, the AD1896 stores a small subset of coefficients and performs a high order interpolation between the stored coefficients.
So far the above approach works for the case of FS_OUT > FS_IN. However, in the case when the output sample rate, FS_OUT, is less than the input sample rate, FS_IN, the ROM starting address, input data and the length of the convolution must be scaled. As the input sample rate rises over the output sample rate, the anti-aliasing filter's cutoff frequency has to be lowered because the Nyquist frequency of the output samples is less than the Nyquist frequency of the input samples. To move the cutoff frequency of the anti-aliasing filter, the coefficients are dynamically altered and the length of the convolution is increased by a factor of (FS_IN/FS_OUT). This technique is supported by the Fourier transform property that if f(t) is F(ω), then f(k*t) is F(ω/k). Thus, the range of decimation is simply limited by the size of the RAM.

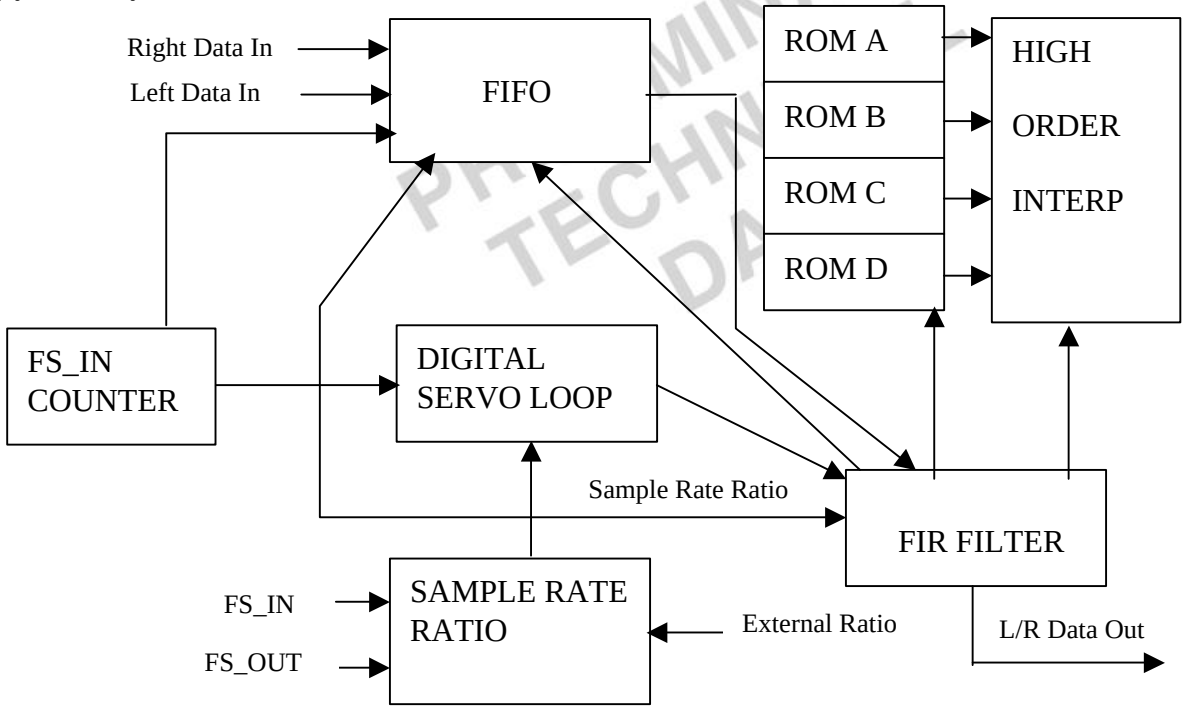


Figure 3. Architecture of the sample rate converter.

The Sample Rate Converter Architecture

The architecture of the sample rate converter is shown in figure 3. The sample rate converter's FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The FS_IN counter provides the write address to the FIFO block and the ramp input to the digital servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high order interpolation between the store coefficients. The sample rate ratio block measures the sample rate for dynamically altering the ROM coefficients and scaling of the FIR filter length as well as the input data. The digital servo loop automatically tracks the FS_IN and FS_OUT sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

The FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the sample rate converter and the scaling of the input data by the sample rate ratio before storing the samples in the RAM. The input data is scaled by the sample rate ratio because as the FIR filter length of the

convolution increases so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (FS_OUT/FS_IN) when FS_OUT < FS_IN. The FIFO also scales the input data for muting and unmuting of the AD1896.

The RAM in the FIFO is 512 words deep for both left and right channels. An offset to the write address provided by the FS_IN counter is added to prevent the RAM read pointer from ever overlapping the write address. The offset is selectable by the GRPDLYS, group delay select, signal. A small offset is added, 16, to the write address pointer when GRPDLYS is high, and a large offset is added, 64, to the write address pointer when GRPDLYS is low. Increasing the offset of the write address pointer is useful for applications when small changes in the sample rate ratio between FS_IN and FS_OUT are expected. The maximum decimation rate can be calculated from the RAM word depth and GRPDLYS as (512-16)/64 taps = 7.75 for short group delay and (512-64)/64 taps = 7 for long group delay.

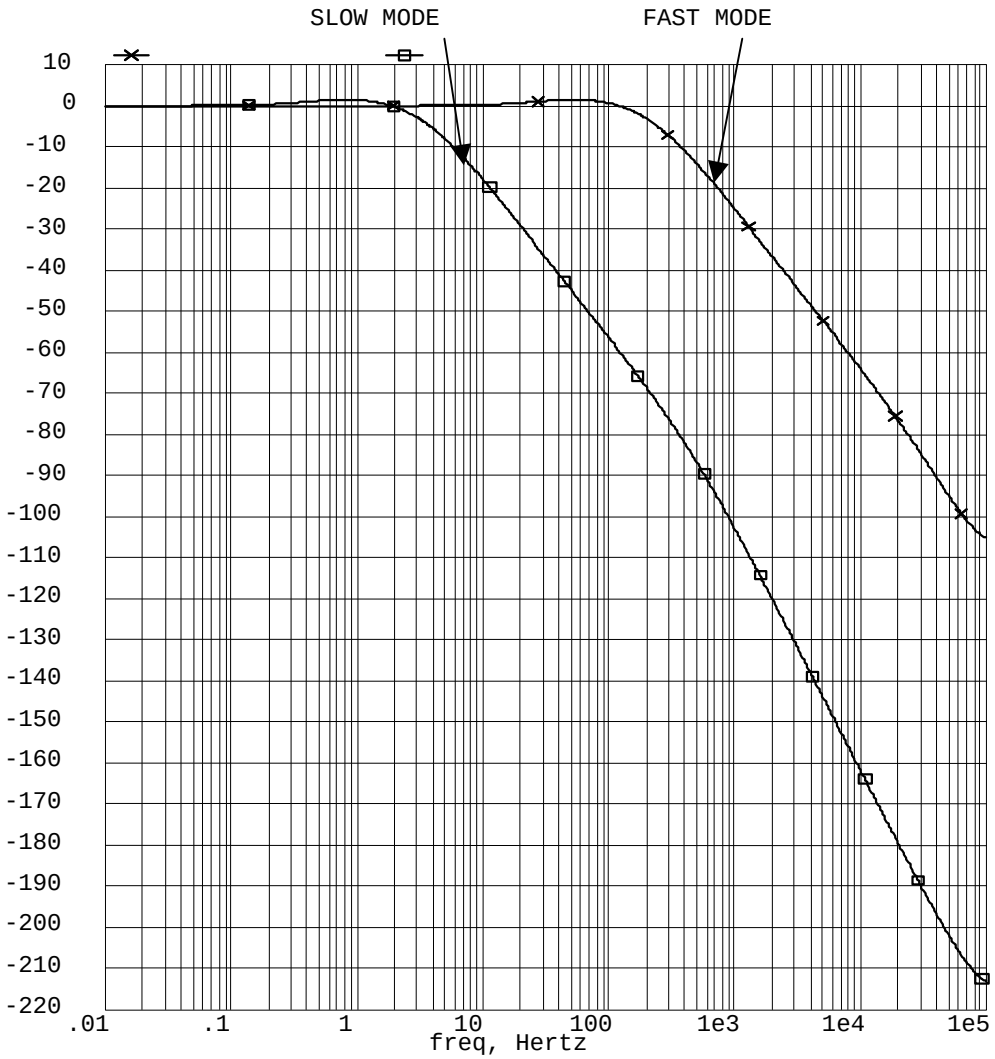


Figure 4. Frequency Response of the Digital Servo Loop. FS_IN is the x-axis, FS_OUT=192kHz, Master Clock Frequency is 30 MHz.

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter while the ROM is the fractional part. The digital servo loop must be able to provide excellent rejection of jitter on the FS_IN and FS_OUT clocks as well as measure the arrival of the FS_OUT clock within 4.97 ps. The digital servo loop will also divide the fractional part of the ramp output by the ratio of FS_IN/FS_OUT for

the case when FSIN > FSOUT to dynamically alter the ROM coefficients.

The digital servo loop is implemented with a multirate filter. To settle the digital servo loop filter quicker upon start up or a change in the sample rate, a “fast mode” was added to the filter. When the digital servo loop starts up or the sample rate is changed, the digital servo loop kicks into “fast mode” to adjust and settle on the new sample rate. Upon sensing the digital servo loop settling down to some reasonable value, the digital servo loop will kick into “normal” or “slow mode”. During “fast mode” the MUTE_OUT signal of the sample rate converter is asserted to let the user know that they should mute the sample rate converter to avoid any clicks or pops. The frequency response of the digital servo loop for “fast mode” and “slow mode” are show in figure 4.

The FIR filter is a 64 tap filter in the case of FS_OUT >= FS_IN and is (FS_IN/FS_OUT) * 64 taps for the case when FS_IN > FS_OUT. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital servo loop at the start of the FS_OUT period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the (FS_OUT/FS_IN)*2^{20} ratio for FS_IN > FS_OUT or 2^{20} for FS_OUT >= FS_IN. Once the ROM address rolls over, the convolution is completed. The convolution is performed for both the left and right channels and the multiply accumulate circuit used for the convolution is shared between the channels.

The FS_IN/FS_OUT sample rate ratio circuit is used to dynamically alter the coefficients in the ROM for the case when FS_IN > FS_OUT. The ratio is calculated by comparing the output of a FS_OUT counter to the output of a FS_IN counter. If FS_OUT > FS_IN, the ratio is held at one. If FS_IN > FS_OUT, the sample rate ratio is updated if it is different by more than two FS_OUT periods from the previous FS_OUT to FS_IN comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

However, the hysteresis of the FS_OUT/FS_IN ratio circuit can cause phase mismatching between two AD1896’s operating with the same input clock and the same output clock. Since the hysteresis requires a difference of more than two FS_OUT periods for the FS_OUT/FS_IN ratio to be updated, two AD1896’s may have differences in their ratios from 0 to 4 FS_OUT period counts. The FS_OUT/FS_IN ratio adjusts the filter length of AD1896, which corresponds directly with the group delay. Thus, the magnitude in the phase difference will depend upon the resolution of the FS_OUT and FS_IN counters. The greater the resolution of the counters, the smaller the phase difference error will be.

The AD1896’s FS_IN and FS_OUT counters have three bits of extra resolution over the AD1890, which reduces the phase mismatch error by a factor of 8. However, an additional feature was added to the AD1896 to eliminate the phase mismatching completely. One AD1896 can set the FS_OUT/FS_IN ratio of other AD1896’s by transmitting its FS_OUT/FS_IN ratio through the serial output port.

OPERATING FEATURES

Serial Input/Output Ports

Serial I/O Port Modes

Control Signals

Reset

Reset & Power Down

<Saving power in power down mode and initialising internal registers, timing, minimum reset delay after power up, minimum RESET risetime, reset requirement during power sag.>

Power Supply & Voltage Reference

The AD1896 is designed for three volt supplies with five volt input compliance. Separate power supply pins are used for the internal logic and the input and output interface logic. These pins should be bypassed with 100nF ceramic chip capacitors, as close to the pins as possible, to minimise noise pickup. A bulk aluminium electrolytic capacitor of 47:F should also be provided on the same PC board as the AD1896.

<Comments to be added: Supply tolerance, Current required, filtering, power down savings. Rate of power up, latchup, etc>

Digital Filter Group Delay

The group delay of the digital filter may be selected by the logic pin GRPDLYS. When this pin is high the filter group delay will be short and is given by the equation,

$$GDS = \frac{16}{FS_{in}} + \frac{32}{FS_{in}} \text{ seconds for } FS_{out} > FS_{in}$$

$$GDS = \frac{16}{FS_{in}} + \left(\frac{32}{FSin}\right) \times \left(\frac{FSin}{FSout}\right) \text{seconds for } FS_{out} < FS_{in}$$

$$GDL = \frac{64}{FS_{in}} + \frac{32}{FS_{in}} \text{ seconds for } FS_{out} > FS_{in}$$

$$GDL = \frac{64}{FS_{in}} + \left(\frac{32}{FSin}\right) \times \left(\frac{FSin}{FSout}\right) \text{seconds for } FS_{out} < FS_{in}$$

Note: For the long GDL mode, the Decimation Ratio is limited to less than 7:1

Mute Control

When active, the MUTE_IN control will linearly decrease the data to zero. When the MUTE_IN signal is removed, the attenuation will linearly decrease to zero. A 12-bit counter, clocked by LRCLK_I is used to control the mute attenuation hence the mute time will take 4096/LRCLK_I seconds.

When the internal FIFO read pointer overruns the write pointer the MUTE_OUT pin is activated. Normally this pin will be connected externally to the MUTE_IN pin to mute the audio output. The MUTE_OUT pin is also internally connected to the digital PLL fast/slow loop control.

Clock Signals

In master mode, the AD1896 requires a $256F_S$, $512F_S$ or $768F_S$ master clock (MCLK). The 'power-up' default is 256Fs. For a maximum master clock frequency of 33MHz, the maximum sample rate is limited to 96kHz. In slave mode, sample rates up to 192kHz can be handled.

<Master clock requirements, glitch sensitivity, jitter sensitivity, input and output synchronous serial bit clocks and frame clocks, BCLK and LRCLK requirements and jitter sensitivity.>

When either of the serial ports is operated in master mode, the master clock is divided down to derive the associated left/right subframe clock (LRCLK) and serial bit clock (SCLK). The master clock frequency can be selected for 256, 512 or 768 times the output sample rate. A 33MHz crystal or external clock can be used. The LRCLK and BCLK clock signals will be synchronous with their respective input and output sample rates.

MMODE_0/1/2			INTERFACE FORMAT
2	1	0	
0	0	0	Both Serial Ports are in Slave Mode
0	0	1	Output Serial Port is Master with 768xFs
0	1	0	Output Serial Port is Master with 512xFs
0	1	1	Output Serial Port is Master with 256xFs
1	0	0	Matched Phase Mode
1	0	1	Input Serial Port is Master with 768xFs
1	1	0	Input Serial Port is Master with 512xFs
1	1	1	Input Serial Port is Master with 256xFs

Reset Control

<Timing, functionality, power down savings, default states.>

Serial Data Ports – Data Format

The serial data input port mode is set by the logic levels on the SMODE_IN_0/1/2 pins. The serial mode can be changed to I2S, Right Justified (RJ), 16, 20 or 24-Bits, or TDM as defined in the following table.

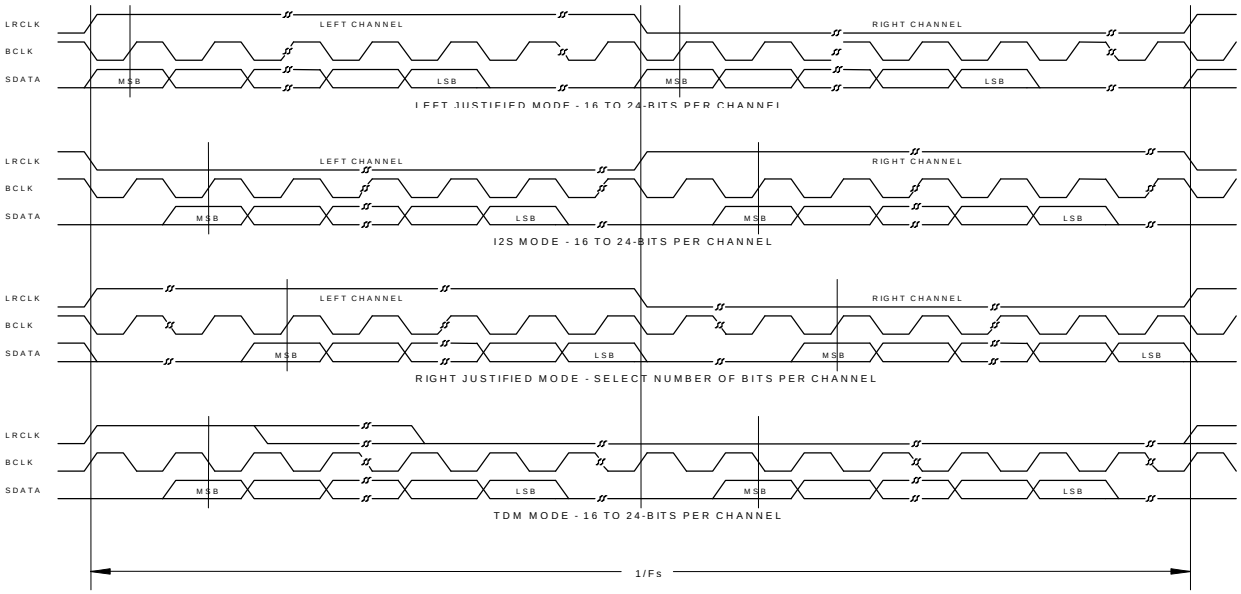
SMODE_IN_0..2			INTERFACE FORMAT
2	1	0	
0	0	0	Left Justified
0	0	1	I2S
0	1	0	Undefined
0	1	1	Undefined
1	0	0	Right Justified, 16-Bits
1	0	1	Right Justified, 18-Bits
1	1	0	Right Justified, 20-Bits
1	1	1	Right Justified, 24-Bits

The serial data output port mode is set by the logic levels on the SMODE_OUT_0/1 and WLNGTH_O_0/1 pins. The serial mode can be changed to I2S, Right Justified (RJ), 16, 20 or 24-Bits, or TDM as defined in the following table. The Right Justified serial Data Out Mode assumes 64 SCLK_O cycles per frame, divided evenly for left and right.

SMODE_OUT_0..1		INTERFACE FORMAT
1	0	
0	0	Left Justified (LJ)
0	1	I2S
1	0	TDM Mode
1	1	Right Justified (RJ)

WLNGTH_OUT_0/1		WORD WIDTH
1	0	
0	0	24-Bits
0	1	20-Bits
1	0	18-Bits
1	1	16-Bits

The following timing diagrams, show the serial mode formats.

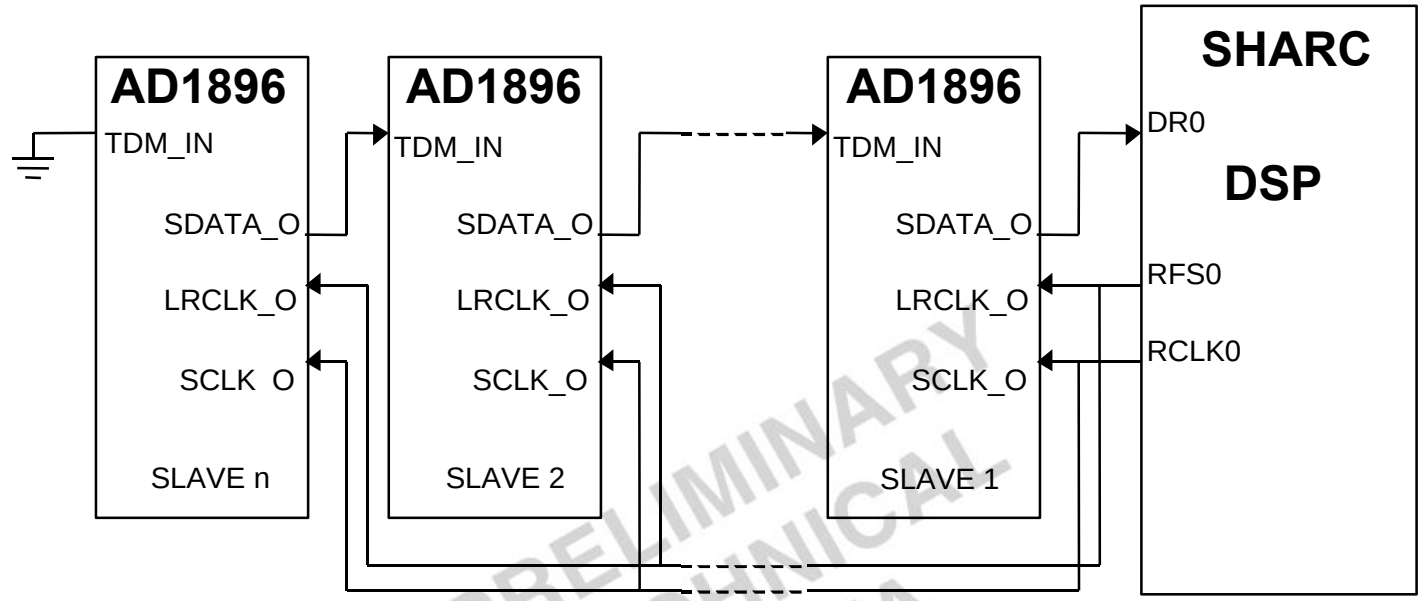


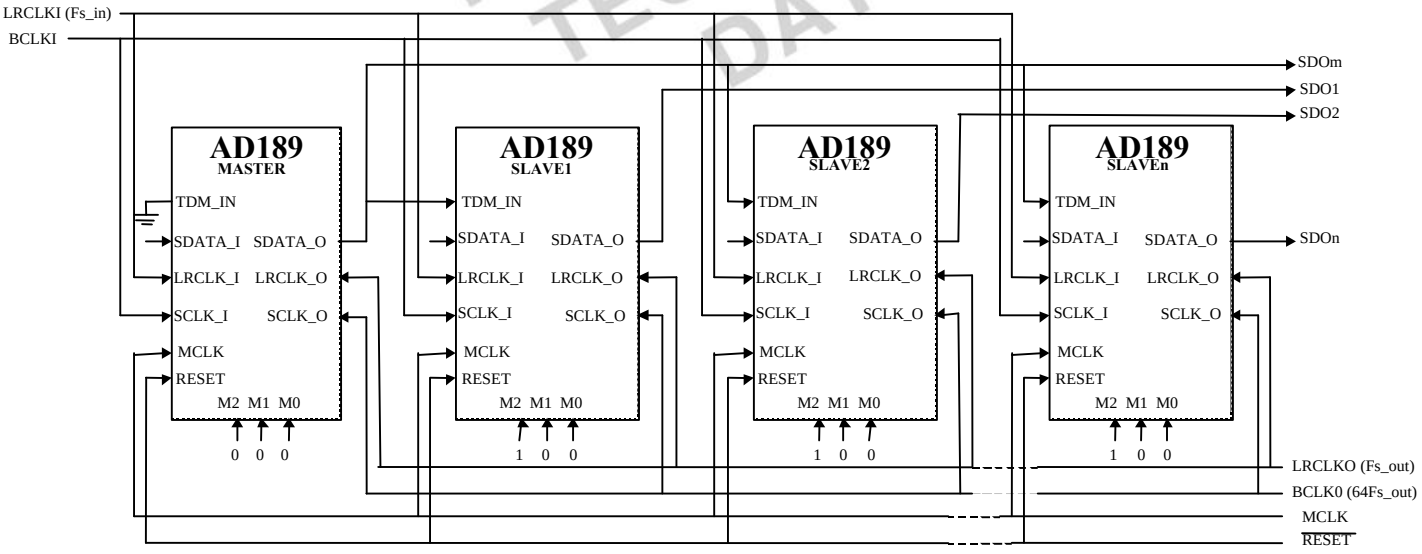
NOTES: 1. TDM MODE DOESN'T IDENTIFY CHANNEL
2. LRCLK NORMALLY OPERATES AT Fs EXCEPT FOR TDM MODE WHICH IS NxFs. WHERE N = NUMBER OF STEREO CHANNELS IN TDM CHAIN
3. BCLK FREQUENCY IS NORMALLY 64xLRCLK

In TDM mode, several AD1896's can be daisy chained together and connected to the serial input port of a SHARC DSP. The AD1896 contains a 64-bit parallel load shift register. When the FSYNC pulse arrives, each AD1896 parallel loads its Left and Right data into the 64-bit shift register. The input to the shift register is connected to TDM_IN while the output is connected to SDATA_O. By connecting the SDATA_O to the TDM_IN of the next AD1896, a large shift register is created which is clocked by SCLK.

APPLICATION INFORMATION

AD1896 DAISY CHAIN APPLICATION





AD1896 - MATCHED PHASE MODE(NON-TDM MODE)

The matched phase mode is the mode discussed in the Theory of Operation section that eliminates the phase mismatch between multiple AD1896's. The master AD1896 device transmits its FS_OUT/FS_IN ratio through the SDATA_O pin to the slave AD1896s' TDM_IN pins. The slave AD1896s receive the transmitted FS_OUT/FS_IN ratio and use the transmitted FS_OUT/FS_IN ratio instead of its own internally derived FS_OUT/FS_IN ratio. The master device can have both its serial ports in slave mode as depicted or either one in master mode. The slave AD1896s have to have their MMODE_2, MMODE_1 and MMODE_0 pins set to 100 respectively. SCLK_I and SCLK_O may be asynchronous with respect to each other in this mode.

TIMING DIAGRAMS

<Timing diagrams for SCLK and LRCLK, SDATA setup and hold times for both slave and master modes
MUTE_IN,OUT timing
RESET timing diagram
MCLK timing diagram>

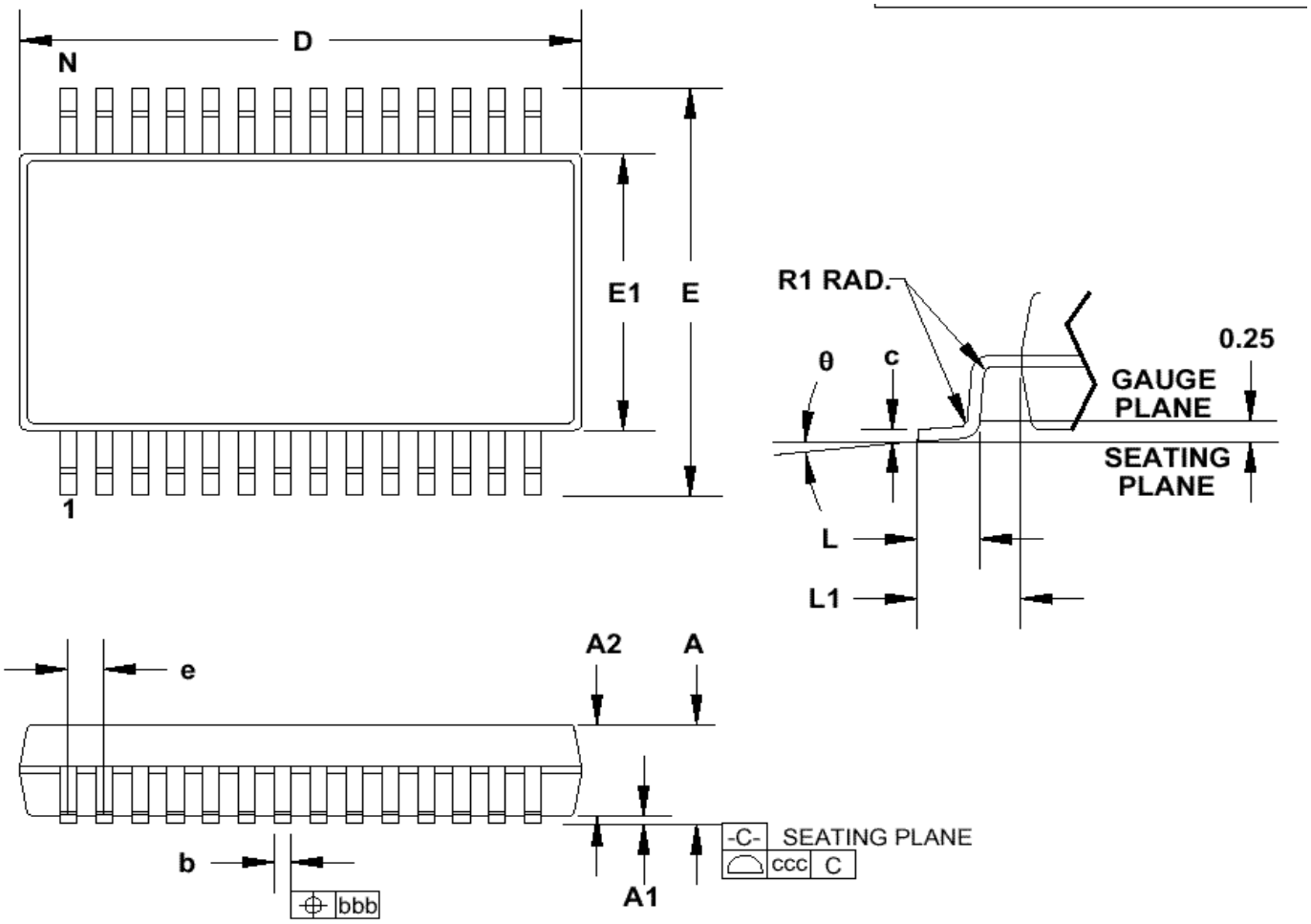
PERFORMANCE PLOTS

<Insert plots here>

Examples:

FFT: 1kHz, 5kHz, 10kHz, 20kHz, 40kHz @ 0dBFS @ 48/96/192kHz
FFT : 1kHz, 5kHz, 10kHz, 20kHz, 40kHz @ -60dBFS @ 48/96/192kHz
THD+N vs Freq
THD+N vs Level
DNR vs Freq
DNR vs Level
Linearity: 0dBFS to –140dBFS
Noise floor
Passband Filter Frequency Response at 48/96/192kHz
Stopband Filter Frequency Response at 48/96/192kHz
Two tone IMD
PSRR

PACKAGE INFORMATION



# of LDS	D		
	Min	Nom	Max
8	2.70	3.00	3.30
14	5.90	6.20	6.50
16	5.90	6.20	6.60
18	6.90	7.20	7.50
20	6.90	7.20	7.50
22	7.90	8.20	8.50
24	7.90	8.20	8.50
28	9.90	10.20	10.50
30	9.90	10.20	10.50
38	12.3	12.60	12.90

Dim	Min.	Nom.	Max
A			2.0
A1	0.05		
A2	1.65	1.75	1.85
b	0.22		0.38
c	0.09		0.25
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e		0.65 BSC	
L	0.55	0.75	0.95
L1		1.25 REF	
R1	0.09		
Θ1	0°	4°	8°
bbb		0.15	
ccc		0.10	

Title: SSOP 5.3mm
Package Outline,CUSTOMER

NOTES:

1. Controlling Dimensions are in mm.
2. All Dimensions per JEDEC Standards MO-150