ANALOG DEVICES

64-Position OTP I²C Compatible Digital Potentiometer

Preliminary Technical Data

AD5171

FEATURES

- Set & Forget One Time Programmable Wiper Set
- 64-Position
- End-to-End Resistance 5k. 10k. 50k. 100kΩ
- Compact SOT23-8 (2.9 x 3mm) Package
- I²C interface
- Full Read/write of wiper register
- Extra Package address decode pin A0
- Power ON Reset to Midscale
- I_{DD} ~ 0.01 μA
- Single Supply +2.7V to +5.5V
- Low Temperature Coefficient 35ppm/°C
- Wide Operating Temperature –40°C to +125°C

Applications

- Permanent Factory PCB Setting
- Resistor Adjustment & Final Set
- Replacement of Trimmers[®] in new designs
- Pressure, Temperature, Position, Chemical and Optical Sensor Calibration
- RF Amplifier biasing
- Automotive Electronics Adjustment
- Gain Control and Offset Adjustment

GENERAL DESCRIPTION

The AD5171 provides a compact 2.9x3mm packaged solution for 64-position OTP adjustment applications. This device performs the same electronic adjustment function as a mechanical trimmer[®] or a variable resistor. Available in four different end-to-end resistance values (5k, 10k, 50k, 100k Ω) these low temperature coefficient devices are ideal for high accuracy and stability variable resistance adjustments.

These devices will provide variable resistance under 2-wire I²C compatible program control in servo adjustment factory applications. Once the final value is determined. The user programs a permanent write command freezing the wiper position at the desired setting (analogous to placing epoxy on a mechanical

Notes:

1. The terms digital potentiometers, VR, and RDAC are used interchangeably.

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trimmer). This one time program sets a validation bit, which can be read through the I²C interface. Once this acknowledge bit is set the wiper position can not be changed due to power supply sequencing, temperature, RF fields, ESD exposure, when maintained within its absolute maximum ratings. For applications that require continuous infrequent adjustment of wiper resistance settings, see the AD523x/AD525x families of nonvolatile memory digital potentiometers.

Operating from a 2.7 to 5.5 volt power supply consuming less than 1uA allows for usage in portable battery operated applications.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

1	W	А	8
2	V_{DD}	В	7
3	GND	A0	6
4	SCL	SDA	5

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64 Position Digital Potentiometer

AD5171

AD5171 ELECTRICAL CHARACTERISTICS 5K, 10K, 50K, 100K Ω **VERSION** (V_{DD} = +5V ± 10%, or +3V ± 10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +125°C unless otherwise noted.)

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	+3V ± 10%, V _A = +V _{DD} , V _B = 0V, -40° Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
Resistor Integral Nonlinearity2R-INL $R_{WB}^{-}V_{A} = No Connect$ -2±0.5+2LSBNominal Resistor Tolerance3 AR_{AB} $Ta = 25^{\circ}$ $V_{AB} = V_{DD}$, Wiper PN Connect3035 $ppm^{m}C$ Wiper Resistance Temperature Coefficient R_{W}^{-} $V_{DD} = +5V$ 50100 Ω DC CHARACTERISTICS POTENTIOMETER DIVIDER MODESpecifications apply to all VRs8BitsResolutionN -1 $\pm 1/4$ $+1$ LSBIntegral Nonlinearity4DNL -2 $\pm 1/2$ $+2$ LSBVoltage Divider Temperature Coefficient AV_{W}/XT Code = 80 ₁ -2 $\pm 1/4$ $+1$ LSBVoltage Divider Temperature Coefficient AV_{W}/XT Code = 80 ₁ -1 $\pm 1/4$ $+1$ LSBZero Scale Error $V_{W/SE}$ Code = 60_{11} -1 $\pm 1/4$ $+1$ LSBZero Scale Error $V_{W/SE}$ Code = 60_{11} -1 $\pm 1/4$ $+1$ LSBValtage Range ⁶ $V_{A,B,W}$ $C_{A,B}$ $f = 1$ MHz, measured to GND, Code = 80_{11} 45 pF Capacitance4 A, B $C_{A,B}$ $f = 1$ MHz, measured to GND, Code = 80_{11} 45 pF Capacitance4 $V_{A,B,W}$ $V_{A,B,W}$ 2.4 V V_{DD} Common-Mode Leakage $I_{M,W}$ $V_{M,B}$ 2.4 V V Input Logic Low $V_{H,B}$ $V_{M,B}$ $V_{M,B}$ $V_{M,B}$ $V_{M,B}$ $V_{M,B}$ Logic Supply Current	DC CHARACTERISTICS RHEOSTAT MOD	E					
Resistor Integral Nonlinearity2R-INL ABue $R_{WD} V_A = No Connect$ T a 25°C-2 -2 	Resistor Differential Nonlinearity ²	R-DNL	R_{WB} , V_A = No Connect	-1	±0.25	+1	LSB
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Resistor Integral Nonlinearity ²	R-INL		-2	±0.5	+2	LSB
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Nominal Resistor Tolerance ³	ΔR_{AB}		-30		30	%
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Resistance Temperature Coefficient	$R_{AB}/\Delta T$	$V_{AB} = V_{DD}$, Wiper = No Connect		35		ppm/°C
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Wiper Resistance	R _W	$V_{DD} = +5V$		50	100	Ω
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	DC CHARACTERISTICS POTENTIOMETER	R DIVIDER MOD	E Specifications apply to all VRs				
$\begin{array}{ c c c c c c } \mbox{Integral Nonlinearity}^{4} & NL \\ \mbox{Volge Divider Temperature Coefficient} \\ \mbox{Volge Range}^{5} \\ \mbox{Volge Temperature Coefficient} \\ \mbox{Volge Range}^{5} \\ \mbox{Volge Range}^{5} \\ \mbox{Volge Range}^{5} \\ \mbox{Volge Range}^{5} \\ \mbox{Volge Temperature Coefficient} \\ \mbox{Volge Range}^{5} \\ Volge R$	Resolution	Ν		8			Bits
	Differential Nonlinearity ⁴	DNL		-1	±1/4	+1	LSB
	Integral Nonlinearity ⁴			-2	±1/2	+2	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Voltage Divider Temperature Coefficient	$\Delta V_W / \Delta T$	Code = 80 _H		5		ppm/°C
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Full-Scale Error	V _{WFSE}	Code = FF _H	–1.5	-0.5	+0	LSB
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Zero-Scale Error	V _{WZSE}	Code = 00 _H	0	+0.5	+1.5	LSB
$ \begin{array}{cccc} Capacitance^{i} A, B & C_{A,B} & f = 1 \mbox{ MHz, measured to GND, Code = 80_H} & 45 & PF \\ Capacitance^{i} W & C_W & f = 1 \mbox{ MHz, measured to GND, Code = 80_H} & 60 & PF \\ Shutdown Supply Current? & I_{DO, SD} & V_{DD} = 5.5V & 0.01 & 5 & \muA \\ Common-Mode Leakage & I_{CM} & V_{A} = V_B = V_{DO}/2 & 1 & nA \\ \hline DIGITAL INPUTS & OUTPUTS & I_{LM} & V_{A} = V_B = V_{DO}/2 & 1 & 0.8 & V \\ Input Logic Ligh & V_{IL} & 0.8 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.8 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +5V & 0.5 & PF \\ \hline POWER SUPPLIES & V_{DD} RANGE & V_{SS} = 0V & 0.8 & 5 & PF \\ Capacitance^6 & C_{IL} & V_{SS} = 0V & 0.3 & 5.5 & V \\ Supply Current & I_{DD} & V_{DD} RANGE & V_{SS} = 0V & 0.3 & 5.5 & V \\ Supply Current & I_{DD} & V_{H} = +5V \ or V_{IL} = 0V, V_{DD} = +5V & 0.2 & mW \\ Power Dissipation^6 & P_{DISS} & V_{H} = +5V \ or V_{IL} = 0V, V_{DD} = +5V & 0.2 & mW \\ Power Supply Sensitivity & PSS & \Delta V_{DD} = +5V \pm 10\%, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_10K & R_{NB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{NB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{NB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{NB} = 0V, F1KHz, R_{AB} = 10K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} = V, V_{S} = 0V, V_{S} = V, V_{S} = 10K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} = V, V_{S} = V, V_{S} = V, V_{S} = V, V_{S} = 10K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} = V, V_{S} = V, F1KHz, R_{AB} = 10K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} = V, V_{S} = V, F1KHz, R_{AB} = 10K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} = V, V_{S} = V, F1KHz, R_{S} = 0K\Omega & 0.003 & \% \\ V_{NS} Stitling Time (10K\Omega/50K\Omega) & V_{S} & V_{A} = 5V, V_{S} = 0V, F1$	RESISTOR TERMINALS						
$\begin{array}{cccc} Capacitance^{6} A, B & C_{A,B} & f = 1 \mbox{ MHz, measured to GND, Code = 80_H} & 45 & pF \\ Capacitance^{6} W & C_W & f = 1 \mbox{ MHz, measured to GND, Code = 80_H} & 60 & pF \\ Shutdown Supply Current? & loo_so & V_{DD} = 5.5V & 0.01 & 5 & \muA \\ Common-Mode Leakage & lc_M & V_A = V_B = V_{DD}/2 & 1 & nA \\ \hline DIGITAL INPUTS & OUTPUTS & & 2.4 & V \\ Input Logic Ligh & V_{IL} & V_{DD} = +3V & 2.1 & 0.8 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Clow & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 2.1 & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +3V & 0.6 & V \\ Input Logic Low & V_{IL} & V_{DD} = +5V & 0.5 & PF \\ \hline POWER SUPPLIES & & 2.7 & 5.5 & V \\ Supply Current & I_{DD} & V_{DD \ RANGE} & V_{SS} = 0V & 0.3 & 5.5 & V \\ Supply Current & I_{DD} & V_{DD \ RANGE} & V_{SS} = 0V & 0.3 & 5.5 & V \\ Supply Current & I_{DD} & V_{DD \ RANGE} & V_{DD \ RANGE} & V_{SS} = 0V & 0.0 & 0.001 & +0.01 & \%/\% \\ Power Dissipation^{6} & P_{DISS} & V_{H} = +5V \ or V_{IL} = 0V, V_{DD} = +5V & 0.2 & mW \\ Power Supply Sensitivity & PSS & \Delta V_{DD} = +5V \pm 10\%, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_10K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K\Omega, Code = 80_H & 600 & KHz \\ Bandwidth -3dB & BW_50K & R_{AB} = 10K$	Voltage Range ⁵	V _{A.B.W}		Vss		V _{DD}	v
$\begin{array}{cccc} Capacitance^{\delta} W & C_W & f = 1 \mbox{ MHz, measured to GND, Code = 80_H} & 60 & pF \\ Shutdown Supply Current? & lop_SD & V_{DD} = 5.5V & 0.01 & 5 & \muA \\ Common-Mode Leakage & low & V_A = V_B = V_{DD}/2 & 1 & nA \\ \hline DIGITAL INPUTS & OUTPUTS & & & & & & & & & & & & & & & & & & &$			f = 1 MHz, measured to GND, Code = 80_{H}		45	55	pF
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Capacitance ⁶ W	1	f = 1 MHz, measured to GND, Code = 80_{H}		60		pF
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Shutdown Supply Current ⁷	IDD SD	$V_{DD} = 5.5V$		0.01	5	μA
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Common-Mode Leakage	Ісм	$V_A = V_B = V_{DD} / 2$		1		nA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	DIGITAL INPUTS & OUTPUTS						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Logic High	VIH		2.4			v
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$						0.8	v
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			$V_{DD} = +3V$	2.1			V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Logic Low		$V_{DD} = +3V$			0.6	V
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Input Current		$V_{IN} = 0V \text{ or } +5V$			±1	μA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Input Capacitance ⁶				5		pF
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	POWER SUPPLIES						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		VLOGIC		2.7		5.5	v
Supply CurrentIDD $V_{IH} = +5V \text{ or } V_{IL} = 0V$ 5 μA Power Dissipation ⁸ P_{DISS} $V_{IH} = +5V \text{ or } V_{IL} = 0V, V_{DD} = +5V$ 0.2mWPower Supply SensitivityPSS $\Delta V_{DD} = +5V \pm 10\%, \text{ Code} = \text{Midscale}$ -0.010.001 ± 0.01 $\%/\%$ DYNAMIC CHARACTERISTICS ^{6,9} BW_10KR_{AB} = 10K\Omega, Code = 80_H600KHzBandwidth -3dBBW_50KR_{AB} = 50K\Omega, Code = 80_H100KHzTotal Harmonic DistortionTHD _W V _A = 1Vrms, V _B = 0V, f=1KHz, R_{AB} = 10K\Omega0.003%V _W Settling Time (10K\Omega/50K\Omega)t _S V _A = 5V, V _B =0V, ±1 LSB error band2/9 μ s	0 11 5		V _{SS} = 0V				v
Power Dissipation ⁸ Power Supply Sensitivity P_{DISS} PSS V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V ΔV_{DD} = +5V ΔV_{DD} = +5V ± 10%, Code = Midscale-0.010.01 0.2 mW mWDYNAMIC CHARACTERISTICS ^{6, 9} BW_10K Bandwidth -3dBBW_10K BW_50KR_{AB} = 10K Ω , Code = 80 _H 600KHzBandwidth -3dB Total Harmonic Distortion V _W Settling Time (10K Ω /50K Ω)BW_50K t_SR_{AB} = 50K Ω , Code = 80 _H 100KHzV _W Settling Time (10K Ω /50K Ω)t _S V _A = 5V, V _B =0V, f=1KHz, R_{AB} = 10K Ω 0.003%	Supply Current		$V_{IH} = +5V \text{ or } V_{II} = 0V$		5		μA
Power Supply SensitivityPSS $\Delta V_{DD} = +5V \pm 10\%$, Code = Midscale-0.010.001+0.01%/%DYNAMIC CHARACTERISTICS ^{6, 9} BW_10KRAB = 10K\Omega, Code = 80H600KHzBandwidth -3dBBW_50KRAB = 50K\Omega, Code = 80H100KHzTotal Harmonic DistortionTHD _W V _A = 1Vrms, V _B = 0V, f=1KHz, RAB = 10K\Omega0.003%V _W Settling Time (10KΩ/50KΩ)t _S V _A = 5V, V _B =0V, ±1 LSB error band2/9μs						0.2	mW
Bandwidth -3dBBW_10K $R_{AB} = 10K\Omega$, Code = 80_H 600KHzBandwidth -3dBBW_50K $R_{AB} = 50K\Omega$, Code = 80_H 100KHzTotal Harmonic DistortionTHD _W $V_A = 1Vrms$, $V_B = 0V$, f=1KHz, $R_{AB} = 10K\Omega$ 0.003% V_W Settling Time ($10K\Omega/50K\Omega$) t_S $V_A = 5V$, $V_B = 0V$, ±1 LSB error band2/9 μ_S	•			-0.01	0.001	+0.01	%/%
Bandwidth -3dBBW_50K $R_{AB} = 50K\Omega$, Code = 80_H 100KHzTotal Harmonic DistortionTHD _W $V_A = 1Vrms$, $V_B = 0V$, f=1KHz, $R_{AB} = 10K\Omega$ 0.003% V_W Settling Time (10KΩ/50KΩ) t_S $V_A = 5V$, $V_B = 0V$, ±1 LSB error band2/9µs	DYNAMIC CHARACTERISTICS ^{6, 9}						
Bandwidth -3dBBW_50K $R_{AB} = 50K\Omega$, Code = 80_H 100KHzTotal Harmonic DistortionTHD _W $V_A = 1Vrms$, $V_B = 0V$, f=1KHz, $R_{AB} = 10K\Omega$ 0.003% V_W Settling Time (10KΩ/50KΩ) t_S $V_A = 5V$, $V_B = 0V$, ±1 LSB error band2/9µs		BW 10K	$B_{AB} = 10 KO$ Code = 80μ		600		KH7
Total Harmonic Distortion THD_W $V_A = 1Vrms$, $V_B = 0V$, $f=1KHz$, $R_{AB} = 10K\Omega$ 0.003% V_W Settling Time ($10K\Omega/50K\Omega$) t_S $V_A = 5V$, $V_B = 0V$, ± 1 LSB error band2/9 μ s		-					
V_W Settling Time (10KΩ/50KΩ) t_S V_A = 5V, V_B =0V, ±1 LSB error band 2/9 µs							
			<i>N</i>				
	Resistor Noise Voltage Density	e _{N WB}	$R_{WB} = 5K\Omega$, RS = 0				nV√Hz

PRELIMINARY TECHNICAL DATA

64 Position Digital Potentiometer

AD5171

AD5171 ELECTRICAL CHARACTERISTICS 5K, 10K, 50K, 100K Ω VERSION (V_{DD} = +5V \pm 10%, or

+3V \pm 10%, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
INTERFACE TIMING CHARACTERISTIC	S applies to	all parts(Notes 6,12)				
SCL Clock Frequency	f _{SCL}				400	KHz
$t_{\sf BUF}$ Bus free time between STOP & START	t1		1.3			μs
t _{HD;STA} Hold Time (repeated START)	t2	After this period the first clock pulse is generated	0.6			μs
tLOW Low Period of SCL Clock	t3		1.3			μs
t _{HIGH} High Period of SCL Clock	t4		0.6		50	μs
t _{SU;STA} Setup Time For START Condition	t5		0.6			μs
t _{HD;DAT} Data Hold Time	t6				0.9	μs
t _{SU;DAT} Data Setup Time	t7		100			ns
t_F Fall Time of both SDA & SCL signals	t8				300	ns
$t_{\rm R}$ Rise Time of both SDA & SCL signals	t9				300	ns
$t_{\mbox{SU;STO}}$ Setup time for STOP Condition	t10		0.6			μs

NOTES:

1. Typicals represent average readings at +25°C and V_{DD} = +5V.

2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

3. V_{AB} = V_{DD}, Wiper (V_W) = No connect

4. INL and DNL are measured at Vw with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_DD and VB = 0V.

DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions.

5. Resistor terminals A,B,W have no limitations on polarity with respect to each other.

6. Guaranteed by design and not subject to production test.

- 7. Measured at the A terminal. A terminal is open circuited in shutdown mode.
- 8. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation

9. All dynamic characteristics use V_{DD} = +5V.

See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=2ns(10% to 90% of +3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using V_{LOGIC} = +5V.

11. The AD5171 contains xxxx transistors. Die Size: 30.7mil x 76.8 mil, 2358sq. mil.

12. See timing diagram for location of measured values.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5171 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5171

64 Position Digital Potentiometer ABSOLUTE MAXIMUM RATINGS¹ (T_A = +25°C, unless

otherwise noted)
V _{DD} to GND0.3, +7V
$V_{\text{A}},V_{\text{B}},V_{\text{W}}$ to GND
I _{MAX}
Digital Inputs & Output Voltage to GND0V, +7V
Operating Temperature Range40°C to +125°C
Maximum Junction Temperature (T _{J MAX})+150°C
Storage Temperature65°C to +150°C
Lead Temperature (Soldering, 10 sec)+300°C
Thermal Resistance ³ $\theta_{JA,}$
SOT23-8 230°C/W

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. 2. Maximum terminal current is bounded by the maximum current handling of the switches,

maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance

3. Package Power Dissipation (TJMAX-TA)/ 0JA

ORDERING GUIDE

Model#	R (Ω)	Package Description	Package Option	Brand
AD5171BRJ5	5K	SOT23-8	RJ-8	D12
AD5171BRJ10	10K	SOT23-8	RJ-8	D13
AD5171BRJ50	50K	SOT23-8	RJ-8	D14
AD5171BRJ100	100K	SOT23-8	RJ-8	D15

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64 Position Digital Potentiometer

AD5171

Write Mode:

s	0	1	0	1	1	0	A 0	w	Α	x	R S	S D	x	x	х	x	x	Α	D X	D X	D 5	D 4	D 3	D 2	D 1	D 0	Α	Ρ
		65	Slave	e Ado	dress	s Byt	е				Instruction Byte							Data	Byte	e								

Read Mode:

s	0	1	0	1	1	0	A 0	R	Α	D X	D X	D 5	D 4	D 3	D 2	D 1	D 0	Α	Ρ
	Slave Address Byte										Data	Byte	9						

S = Start Condition

- P = Stop Condition
- **A** = Acknowledge
- X = Don't Care
- W = Write
- R = Read

RS = Reset wiper to Midscale 20_H SD = Shutdown connects wiper to B terminal and open circuits A terminal. It does not change contents of wiper register.

D5,D4,D3,D2,D1,D0 = Data Bits













Figure 3. Reading Data from a Previously Selected RDAC Register in Write Mode

64 Position Digital Potentiometer TABLE 1: AD5171 PIN Descriptions

Pin	Name	Description
1	W	W Terminal
2	V_{DD}	Positive Power Supply
3	GND	Ground
4	SCL	Serial Clock Input, positive edge
		triggered
5	SDA	Serial Data Input/Output
6	A0	Programmable address bit 0 for
		multiple package decoding
7	В	B Terminal
8	А	A Terminal

AD5171

PIN CONFIGURATION

1	W	А	8
2	V_{DD}	В	7
3	GND	A0	6
4	SCL	SDA	5

64 Position Digital Potentiometer

AD5171

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178BA