40-Channel, 14-Bit, Parallel and Serial Input, Voltage-Output DAC

Preliminary Technical Data — AD5379

FEATURES

- 40-Channel DAC in 13 x 13 mm² 108-lead CSPBGA
- System Calibration Function allowing User Programmable Offset and Gain
- Buffered Voltage Outputs
- Output Voltage Span of 3.5V_{REF}(+)
- Maximum Output Voltage Span of 17.5V
- Clear Function to User-defined REFGND ($\overline{CLR}$ Pin)
- Simultaneous Update of DAC Outputs ($\overline{LDAC}$ Pin)
- DAC Increment/Decrement Mode
- Parallel Interface
- DSP-/Microcontroller-compatible 3-wire Serial Interface
- SDO Daisy-Chaining Option
- Power-On-Reset
- Digital Reset ($\overline{RESET}$ pin and Soft-Reset function)

APPLICATIONS

- Automatic Test Equipment
- Optical Networks
- Industrial Control Systems

GENERAL DESCRIPTION

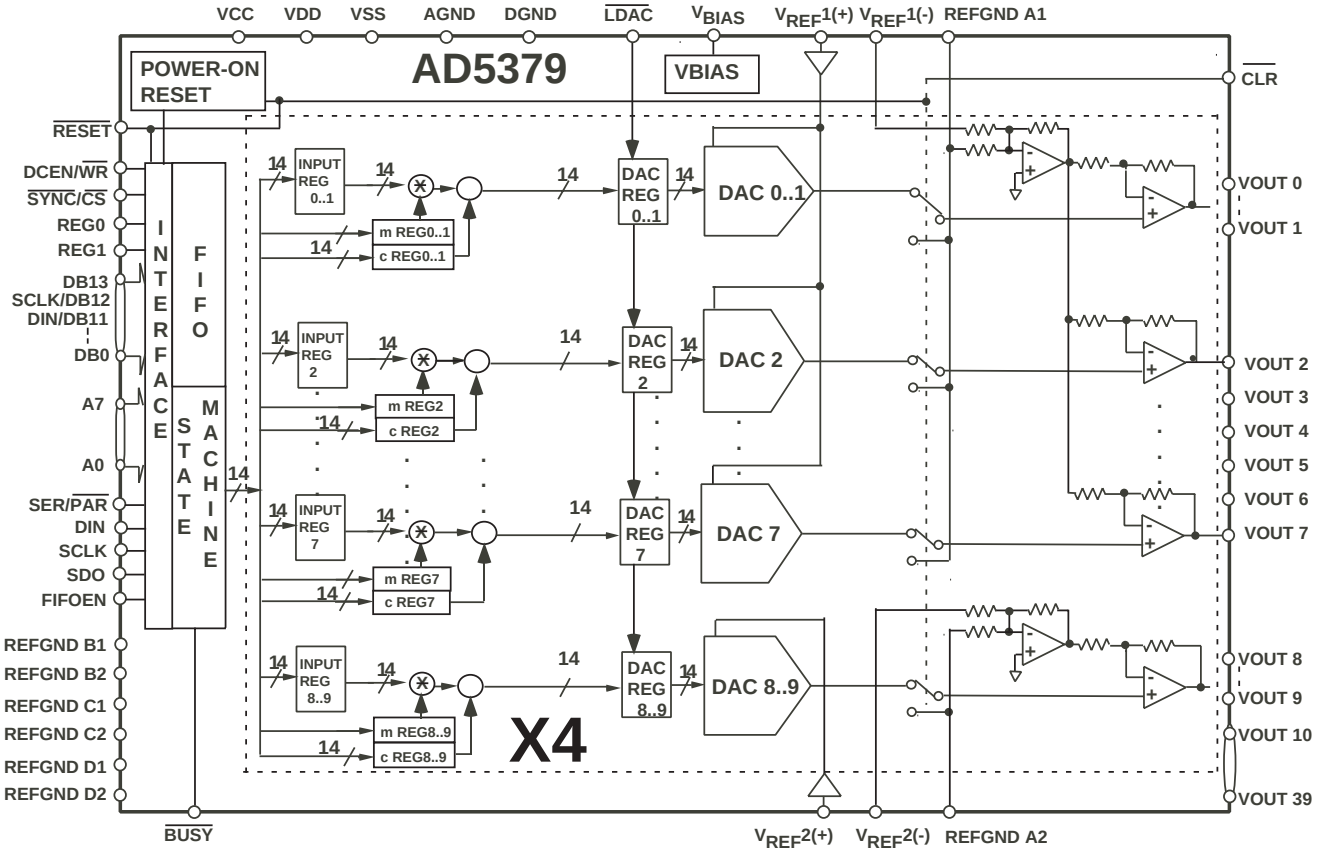
The AD5379 contains forty 14-bit DACs in one package. It has a maximum output voltage span of 17.5V which corresponds to an output range of -8.75 V to +8.75 V derived from reference voltages of -3.5 V and +5 V.

The AD5379 has a parallel interface in which 14 data-bits are loaded into one of the input registers under the control of the $\overline{WR}$, $\overline{CS}$ and DAC channel address pins, A0–A7. It also has a 3-wire serial interface which is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs can be updated simultaneously by taking the $\overline{LDAC}$ input low. Each channel has a programmable gain and offset adjust register.

Each DAC output is gained and buffered on-chip with respect to an external REFGND input. The DAC outputs can also be switched to REFGND via the $\overline{CLR}$ pin.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent Nos. 5,969,657; other patents pending.

SPI and **QSPI** are Trademarks of Motorola, Inc.

MICROWIRE is a Trademark of National Semiconductor Corporation.

REV. PrR

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AD5379–SPECIFICATIONS

(V_{CC} = 2.7 V to 5.5 V; V_{DD} = 12 V ± 5%; V_{SS} = -12 V ± 5% ; V_{REF}(+) = 5 V; V_{REF}(-) = -3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V; C_L = 200 pF to GND; R_L = 11 kΩ to 3 V; Gain = 1; Offset = 0 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy	±4	LSB max	
Differential Nonlinearity	-1/+2	LSB max	Guaranteed Monotonic Over Temperature.
Zero-Scale Error	±10	mV max	
Full-Scale Error	±10	mV max	
Gain Error	TBD	mV max	Typically ±5 mV
Gain Temperature Coefficient[2]	20	ppm FSR/°C typ	
DC Crosstalk[2]	0.5	mV max	Typically 100 µV
REFERENCE INPUTS[2]			
V_{REF}(+) DC Input Impedance	1	MΩ min	Typically 100 MΩ
V_{REF}(-) DC Input Impedance	8	kΩ min	Typically 12 kΩ
V_{REF}(+) Input Current	±10	µA max	Per Input. Typically ±30 nA
V_{REF}(+) Range	1.5/5	V min/max	
V_{REF}(-) Range	-3.5/0	V min/max	
REFGND INPUTS[2]			
DC Input Impedance	80	kΩ min	Typically 120 kΩ
Input Range	±0.5	V min/max	
OUTPUT CHARACTERISTICS[2]			
Output Voltage Range	V_{SS} + 2.5	V min	I_{LOAD} = ±1.5 mA
	V_{DD} - 2.5	V max	I_{LOAD} = ±1.5 mA
Short Circuit Current	15	mA max	
Load Current	±1.5	mA max	
Capacitive Load	200	pF max	
DC Output Impedance	1	Ω max	
DIGITAL INPUTS[2]			
Input High Voltage	2.0	V min	V_{CC} = 2.7 V to 5.5 V
Input Low Voltage	0.8	V max	
Input Current	±30	µA max	Total for All Pins. Input Current per pin < 5µA max.
Input Capacitance	10	pF max	
DIGITAL OUTPUTS ($\overline{BUSY}$, SDO)[2]			
Output Low Voltage	0.5	V max	Sinking 200 µA
Output High Voltage (SDO)	V_{CC} - 0.5	V min	Sourcing 200 µA
Output High Voltage ($\overline{BUSY}$)	V_{CC} + 0.3	V max	Open-drain output. $\overline{BUSY}$ has an internal clamp diode to Vcc
High Impedance Leakage Current	±10	µA max	SDO Only
High Impedance Output Capacitance	10	pF typ	
POWER REQUIREMENTS			
V_{CC}	2.7/5.5	V min/max	
V_{DD}	8.5/16.5	V min/max	
V_{SS}	-3/-16.5	V min/max	
Power Supply Sensitivity[2]			
ΔFull Scale/ΔV_{DD}	-75	dB typ	
ΔFull Scale/ΔV_{SS}	-75	dB typ	
ΔFull Scale/ΔV_{CC}	-90	dB typ	
I_{CC}	5	mA max	V_{CC} = 5.5V. V_{IH} = V_{CC}, V_{IL} = GND.
I_{DD}	40	mA max	V_{DD} = 12.6V. Outputs Unloaded. Typically 14.5 mA
I_{SS}	40	mA max	V_{SS} = -12.6V. Outputs Unloaded. Typically 10.5 mA
Power Dissipation(outputs unloaded)[3]	1.03	W max	$P = (V_{DD} \times I_{DD}) + (V_{SS} \times I_{SS}) + (V_{CC} \times I_{CC})$
Power Dissipation(outputs loaded)[3,4,5]	TBD	W max	$P_{TOTAL} = P + \Sigma[(V_{DD} - V_O) \times I_{SOURCE}] + \Sigma[(V_O - V_{SS}) \times I_{SINK}]$

NOTES

[1]Temperature range for A Version: -40°C to +85°C

[2]Guaranteed by characterization. Not production tested.

[3]V_{DD} = 12.6 V, V_{SS} = -12.6 V, V_{CC} = 5.5 V.

[4]This includes the power dissipation due to the additional current in the 40 output buffers when driving external loads. It does not include the power dissipated in the external loads.

[5]Ensure you do not exceed $T_{J\,(max)}$

Specifications subject to change without notice.

AC CHARACTERISTICS[1]

(V_{CC} = 2.7 V to 5.5 V; V_{DD} = 12 V ± 5%; V_{SS} = -12 V ± 5 %; V_{REF}(+) = 5 V; V_{REF}(-) = -3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V; C_L = 50 pF; R_L = 11 kΩ to 3 V; Gain = 1; Offset = 0 V;)

Parameter	A	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	20	µs typ	Full-Scale Change to ±1/2 LSB.
	TBD	µs max	DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	1	V/µs typ	
Digital-to-Analog Glitch Energy	20	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV max	
Channel-to-Channel Isolation	100	dB typ	V_{REF}+ = 2V pk=pk, (1V Bias) 1kHz, V_{REF}- = -1V
DAC-to-DAC Crosstalk	40	nV-s typ	See Terminology. Between DACs inside a Group
DAC-to-DAC Crosstalk	10	nV-s typ	Between DACs from different groups
Digital Crosstalk	2	nV-s typ	
Digital Feedthrough	1	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density @ 1 kHz	350	nV/(Hz)$^{1/2}$ typ	V_{REF}(+) = V_{REF}(–) = 0 V

[1]Guaranteed by design and characterization, not production tested.
Specifications subject to change without notice.

TIMING CHARACTERISTICS

SERIAL INTERFACE

(V_{CC} = 2.7 V to 5.5 V; V_{DD} = 12 V ± 5%; V_{SS} = -12 V ± 5 %; V_{REF}(+) = 5 V; V_{REF}(-) = -3.5 V; AGND = DGND = REFGND = 0 V; V_{BIAS} = 5 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1,2,3]	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_5[4]	13	ns min	24th SCLK Falling Edge to $\overline{SYNC}$ Falling Edge
t_6[4]	33	ns min	Minimum $\overline{SYNC}$ Low Time
t_7	10	ns min	Minimum $\overline{SYNC}$ High Time
t_8	5	ns min	Data Setup Time
t_9	4.5	ns min	Data Hold Time
t_{10}[4,5]	30	ns max	24th SCLK Falling Edge to $\overline{BUSY}$ Falling Edge
t_{11}	900	ns typ	$\overline{BUSY}$ Pulse Width Low (Single Channel Update)
t_{12}[4]	20	ns min	24th SCLK Falling Edge to $\overline{LDAC}$ Falling Edge
t_{13}	20	ns min	$\overline{LDAC}$ Pulse Width Low
t_{14}	100	ns max	$\overline{BUSY}$ Rising Edge to DAC Output Response Time
t_{15}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{LDAC}$ Falling Edge
t_{16}	100	ns min	$\overline{LDAC}$ Falling Edge to DAC Output Response Time
t_{17}	30	µs typ	DAC Output Settling Time
t_{18}	20	ns min	$\overline{CLR}$ Pulse Width Low
t_{19}	300	ns max	$\overline{CLR}$ Pulse Activation Time
t_{20}[6,7]	20	ns max	SCLK Rising Edge to SDO Valid
t_{21}[7]	5	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_{22}[7]	8	ns min	$\overline{SYNC}$ Rising Edge to SCLK Rising Edge
t_{23}[7]	20	ns min	$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3]See Figures 3 and 4
[4]Stand-Alone Mode only.
[5]This is measured with the load circuit of Figure 1a.
[6]This is measured with the load circuit of Figure 1b.
[7]Daisy-Chain Mode only.
Specifications subject to change without notice.

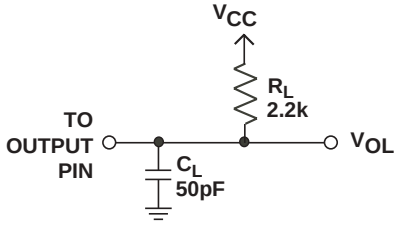


Figure 1a Load Circuit for $\overline{BUSY}$ Timing Diagram

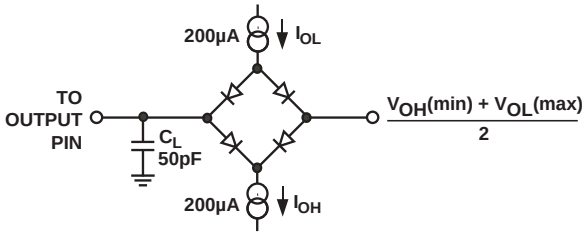


Figure 1b Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain mode)

TIMING CHARACTERISTICS
PARALLEL INTERFACE

(V_{CC} = 2.7 V to 5.5 V; V_{DD} = 12 V ± 5 %; V_{SS} = -12 V ± 5%; AGND = DGND = DUTGND = 0 V; V_{REF}(+) = 5 V; V_{REF}(-) = -3.5 V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1,2,3]	Limit at T_{MIN}, T_{MAX}	Units	Description
t_0	4.5	ns min	REG0, REG1, Address to $\overline{WR}$ Rising Edge Setup Time
t_1	4.5	ns min	REG0, REG1, Address to $\overline{WR}$ Rising Edge Hold Time
t_2	20	ns min	$\overline{CS}$ Pulse Width Low
t_3	20	ns min	$\overline{WR}$ Pulse Width Low
t_4	0	ns min	$\overline{CS}$ to $\overline{WR}$ Falling Edge Setup Time
t_5	0	ns min	$\overline{WR}$ to $\overline{CS}$ Rising Edge Hold Time
t_6	4.5	ns min	Data to $\overline{WR}$ Rising Edge Setup Time
t_7	4.5	ns min	Data to $\overline{WR}$ Rising Edge Hold Time
t_8	20	ns min	$\overline{WR}$ Pulse Width High
t_9[4]	430	ns min	Minimum $\overline{WR}$ Cycle Time (Single Channel Write)
t_{10}[4]	30	ns max	$\overline{WR}$ Rising Edge to $\overline{BUSY}$ Falling Edge
t_{11}[4,5]	400	ns max	$\overline{BUSY}$ Pulse Width Low (Single Channel Update)
t_{12}[4]	30	ns min	$\overline{WR}$ Rising Edge to $\overline{LDAC}$ Falling Edge
t_{13}	20	ns min	$\overline{LDAC}$ Pulse Width Low
t_{14}[4]	100	ns max	$\overline{BUSY}$ Rising Edge to DAC Output Response Time
t_{15}	20	ns min	$\overline{LDAC}$ Rising Edge to $\overline{WR}$ Rising Edge
t_{16}	0	ns min	$\overline{BUSY}$ Rising Edge to $\overline{LDAC}$ Falling Edge
t_{17}[4]	100	ns min	$\overline{LDAC}$ Falling Edge to DAC Output Response Time
t_{18}	30	µs typ	DAC Output Settling Time
t_{19}	20	ns min	$\overline{CLR}$ Pulse Width Low
t_{20}	300	ns max	$\overline{CLR}$ Pulse Activation Time

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3]See Timing Diagram in Figure 2.
[4]See Table III.
[5]This is measured with the load circuit of Figure 1a.
Specifications subject to change without notice.

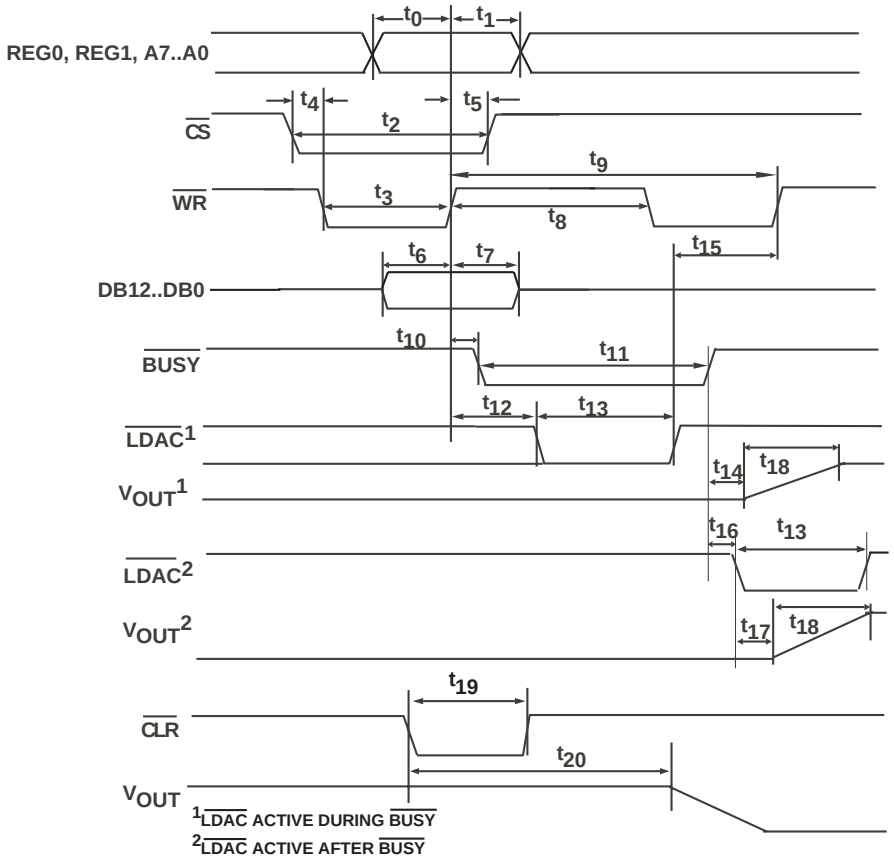


Figure 2. Parallel Interface Timing Diagram

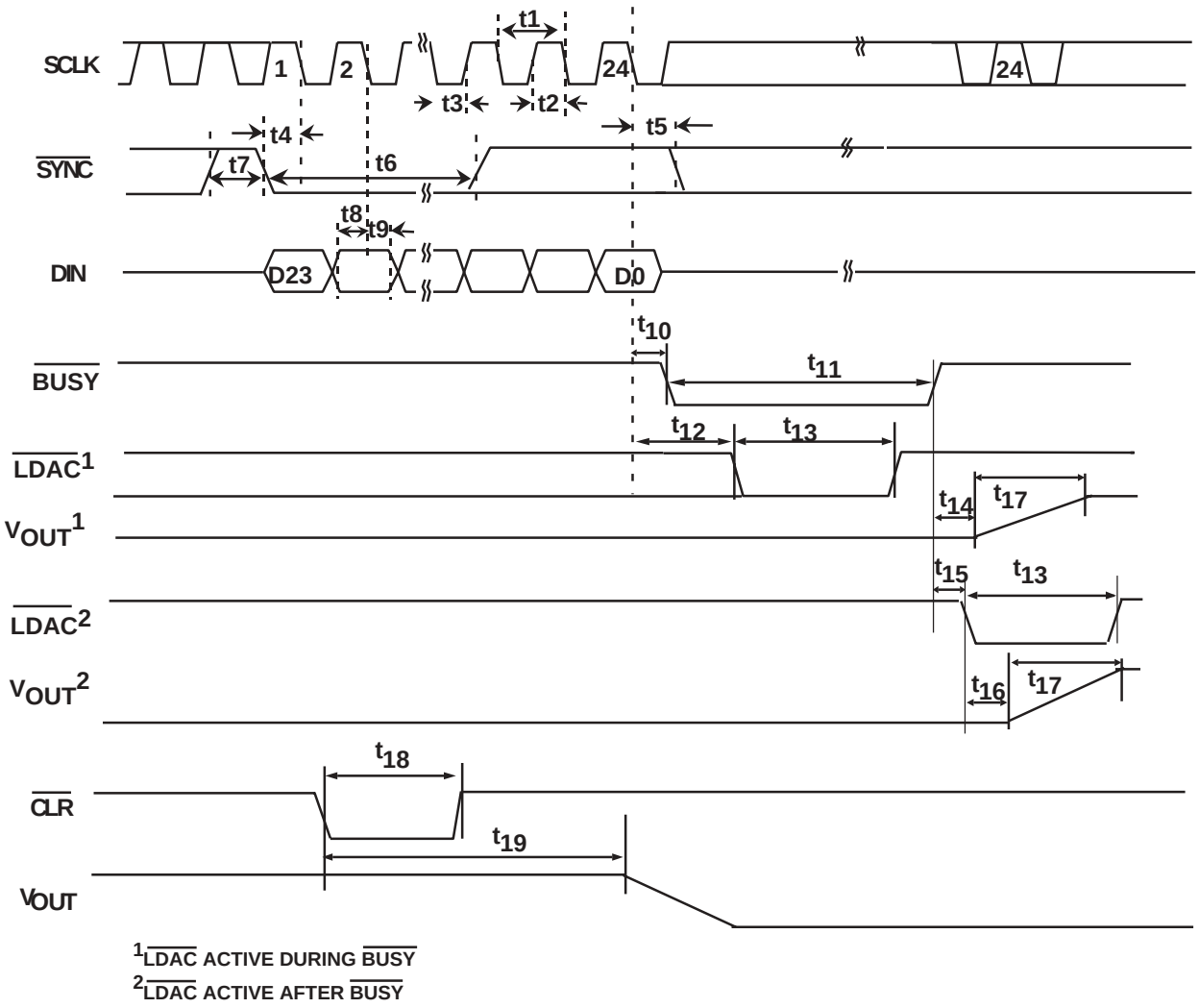


Figure 3. Serial Interface Timing Diagram (Stand-Alone mode)

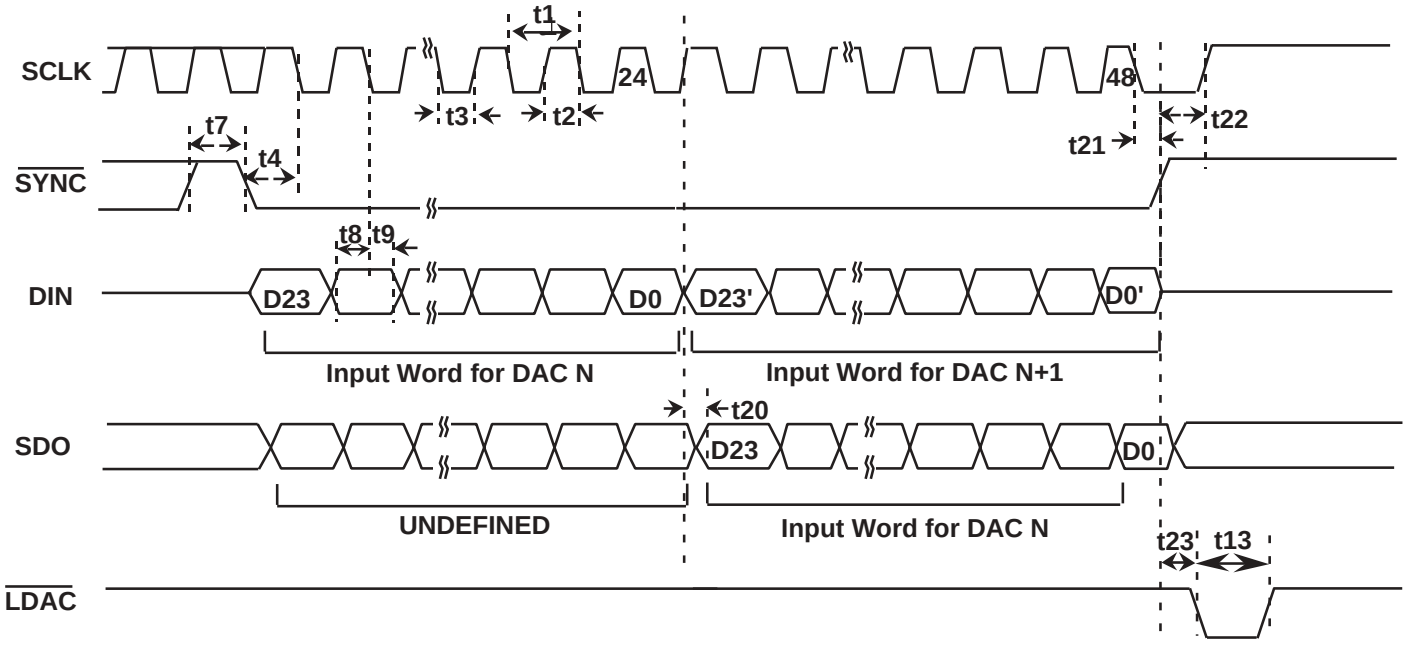


Figure 4. Serial Interface Timing Diagram (Daisy-Chain mode)

ABSOLUTE MAXIMUM RATINGS[1,2]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND.....-0.3 V to +17 V
V_{SS} to AGND.....+0.3 V to -17 V
V_{CC} to DGND.....-0.3 V to +7 V
Digital Inputs to DGND.....-0.3 V to V_{CC} + 0.3 V
Digital Outputs to DGND.....-0.3 V to V_{CC} + 0.3 V
$V_{REF}1(+)$, $V_{REF}2(+)$ to AGND.....-0.3 V to +7 V
$V_{REF}1(-)$, $V_{REF}2(-)$ to AGND.....V_{SS} - 0.3 V to V_{DD} + 0.3 V
V_{BIAS} to AGND.....-0.3 V to +5.5 V
VOUT0-39 to AGND.....V_{SS} - 0.3 V to V_{DD} + 0.3 V
REFGND to AGND.....V_{SS} - 0.3 V to V_{DD} + 0.3 V
AGND to DGND..... -0.3 V to +0.3 V

Operating Temperature Range (T_A)
Industrial(A Version).....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max).....+150°C
108-lead CSPBGA Package,
θ_{JA} Thermal Impedance.....47°C/W
θ_{JC} Thermal Impedance.....7°C/W
Max Power Dissipation[3].....(150°C - T_A)/θ_{JA} mW
Reflow Soldering
Peak Temperature.....230°C
Time at Peak Temperature..... 10 sec to 40 sec

NOTES:
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up
3This limit includes additional power due to external loads

ORDERING GUIDE

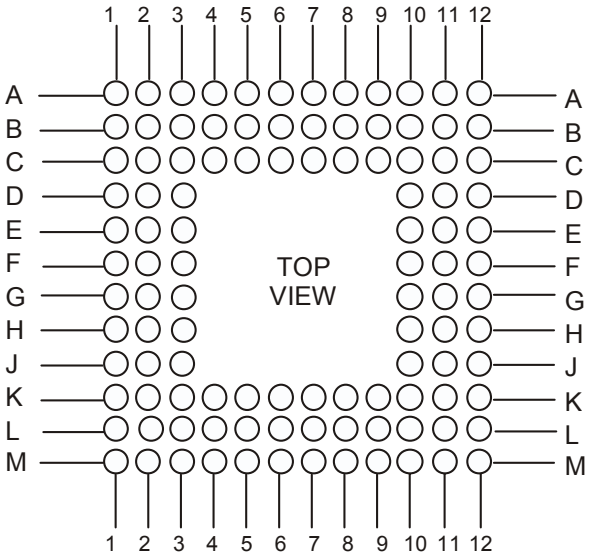
Model	Temperature Range	Linearity Error (LSBs)	Package Description*	Package Option
AD5379ABC	-40°C to +85°C	±4	108-lead CSPBGA	BC-108

* 144 Lead CSPBGA depopulated as shown in Pin Configuration.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5379 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



108-Lead CSPBGA Ball Configuration

CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name
A1	REG0	D1	DB7	K1	A4
A2	VCC3	D2	DB8	K2	A5
A3	DB10	D3	DGND1	K3	A3
A4	AGND4	D10	$V_{REF}1(-)$	K4	DGND2
A5	VBIAS	D11	VOUT35	K5	REFGNDA2
A6	VOUT5	D12	VOUT36	K6	$V_{REF}2(-)$
A7	AGND3	E1	DB5	K7	VOUT12
A8	REFGNDA1	E2	DB6	K8	VOUT13
A9	VDD5	E3	VCC1	K9	VOUT16
A10	VSS5	E10	REFGNDB2	K10	VOUT18
A11	VSS4	E11	VOUT37	K11	VOUT22
A12	VDD4	E12	VOUT38	K12	VOUT23
B1	REG1	F1	DB4	L1	A7
B2	DGND4	F2	DB3[2]	L2	A6
B3	DB9	F3	DB2[2]	L3	N/C[1, 3]
B4	$\overline{CLR}$	F10	VDD3	L4	$\overline{RESET}$[4]
B5	VOUT7	F11	REFGNDD2	L5	VOUT17
B6	VOUT6	F12	VOUT39	L6	AGND2
B7	VOUT0	G1	DB1[2]	L7	VOUT14
B8	VOUT1	G2	DB0[2]	L8	VOUT10
B9	VOUT2	G3	$\overline{BUSY}$	L9	VDD1
B10	VOUT31	G10	VSS3	L10	$V_{REF}2(+)$
B11	REFGNDD1	G11	VOUT29	L11	VOUT20
B12	VOUT30	G12	REFGNDC2	L12	VOUT21
C1	DB13	H1	$\overline{WR}$/DCEN[2]	M1	DGND3
C2	DB12/SCLK	H2	SDO	M2	VCC2
C3	DB11/DIN	H3	$\overline{CS}$/SYNC	M3	FIFOEN[2]
C4	SER/$\overline{PAR}$	H10	VOUT28	M4	AGND1
C5	$\overline{LDAC}$	H11	VOUT26	M5	VOUT15
C6	VOUT8	H12	VOUT27	M6	VOUT11
C7	VOUT3	J1	A0	M7	REFGNDB1
C8	VOUT4	J2	A1	M8	$V_{REF}1(+)$
C9	VOUT9	J3	A2	M9	VSS1
C10	VOUT34	J10	VOUT19	M10	VSS2
C11	VOUT32	J11	VOUT24	M11	VDD2
C12	VOUT33	J12	VOUT25	M12	REFGNDC1

[1]N/C should be left unconnected

[2]Internal 1MΩ pull-down device on these logic inputs. Therefore they can be left floating and will default to a logic low condition.

[3]Internal active pull-up device on these logic inputs. Therefore they can be left floating and will default to a logic high condition.

[4]Internal 1MΩ pull-up device on these logic inputs. Therefore they can be left floating and will default to a logic high condition.

PIN FUNCTION DESCRIPTION

Pin	Function
V_{CC}(1-3)	Logic Power Supply; 2.7 V to 5.5 V.
V_{SS}(1-5)	Negative Analog Power Supply; -12 V ± 5%.
V_{DD}(1-5)	Positive Analog Power Supply; +12 V ± 5%.
AGND(1-4)	Ground for all analog circuitry.
DGND(1-4)	Ground for all digital circuitry.
V_{REF}1(+), V_{REF}1(-)	Reference Inputs for DACs 0 to 7, 10 to 17, 20 to 27 and 30 to 37. These voltages are referred to AGND.
V_{REF}2(+), V_{REF}2(-)	Reference Inputs for DACs 8, 9, 18, 19, 28, 29, 38 and 39. These reference voltages are referred to AGND.
V_{BIAS}	DAC Bias Voltage Input/Output. This pin provides an acess to the on chip voltage generator voltage and is provided for bypassing and overdriving purposes only. If V_{REF}(+) > 4.25 V, V_{BIAS} must be pulled high externally to an equal or higher potential (e.g. 5 V). If V_{REF}(+) < 4.25 V, the on-chip bias generator can be used. In this case the V_{BIAS} pin should be decoupled with a 10 nF capacitor to AGND.
VOUT0 ...VOUT39	DAC Outputs.
SER/$\overline{PAR}$	Interface Select Input. This pin allows the user to select whether the serial or parallel interface will be used. If it is tied high the serial interface will be used.
$\overline{SYNC}$[1]	Active Low Input. This is the Frame Synchronisation signal for the serial interface.
SCLK[1]	Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
DIN[1]	Serial Data Input. Data must be valid on the falling edge of SCLK.
SDO[1]	Serial Data Output. CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
DCEN[1]	Daisy-Chain Select Input (level sensitive, active high). When high this signal is used in conjunction with SER/$\overline{PAR}$ high to enable serial interface daisy-chain mode.
$\overline{CS}$	Parallel Interface Chip Select Input (level sensitive, active low). If it is low the device is selected.
$\overline{WR}$	Parallel Interface Write Input (edge sensitive). The rising edge of $\overline{WR}$ is used in conjunction with $\overline{CS}$ low and the address bus inputs to write to the selected AD5379 registers.
DB13...DB0	Parallel Data Inputs. The AD5379 can accept a straight 14-bit parallel word on DB0 to DB13 where DB13 is the MSB and DB0 is the LSB.
A0...A7	Parallel Address Inputs. A7 to A4 are decoded to select one group or multiple groups of registers for a data transfer. A3 to A0 are decoded to select one of ten input registers, gain registers (m) or offset registers (c). See Page 13 for details of the address decoding.
REG0	Parallel Interface Register Select Input. This pin is used together with REG1 to select data registers, gain registers, offset registers, Increment/Decrement mode or Soft-Reset. See Table II.
REG1	Parallel Interface Register Select Input. This pin is used together with REG0 to select data registers, gain registers, offset registers, Increment/Decrement mode or Soft-Reset. See Table II.
$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). When $\overline{CLR}$ is low, the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant REFGND pin. While $\overline{CLR}$ is low all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is taken high again, the DAC outputs remain cleared until $\overline{LDAC}$ is taken low. The contents of input registers and DAC registers 0 to 39 are not affected by taking $\overline{CLR}$ low.
$\overline{BUSY}$	Digital Input/Open-Drain Output. $\overline{BUSY}$ goes low during internal calculations of x2. During this time the user can continue writing new data to further x1, c and m registers (these are stored in a FIFO) but no further updates to the DAC registers and DAC outputs can take place. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is low this event is stored. Since $\overline{BUSY}$ is bidirectional, it can be pulled low externally in order to delay $\overline{LDAC}$ action. $\overline{BUSY}$ also goes low during power-on-reset or when the $\overline{RESET}$ pin is low. During this time the parallel interface is disabled and any events on $\overline{LDAC}$ are ignored.
$\overline{LDAC}$	Load DAC Logic Input (active low). If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is inactive (high) the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is active and internal calculations are taking place, the $\overline{LDAC}$ event is stored and the DAC registers are updated when $\overline{BUSY}$ goes inactive. However any events on $\overline{LDAC}$ during power-on-reset or $\overline{RESET}$ are ignored.
RESET	Asynchronous Digital Reset Input (falling edge senstive). If unused, RESET may be left unconnected, an internal pullup resistor (1MW) will ensure the RESET input is held high. The function of this pin is equivalent to that of the Power-On-Reset generator. When this pin is taken low, the AD5379 state-machine initiates a reset sequence to digitally reset x1, m, c, and x2 registers to their default power-on values. This sequence takes 100 ms (typ). Furthermore the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant REFGND pin. During RESET, BUSY goes low and the

[1]These serial interface signals do not require separate pins but share parallel interface pins.

PIN FUNCTION DESCRIPTION (CONTINUED)

Pin	Function
	parallel interface is disabled.All LDAC pulses are ignored until BUSY goes high. When RESET is taken high again, the DAC outputs remain at REFGND until LDAC is taken low.
V_{CC}(1-3)	Logic Power Supply; 2.7 V to 3.6 V.
REFGNDA1	Device Sense Ground for DACs 0 to 7. VOUT0 to VOUT7 are referenced to this voltage.
REFGNDA2	Device Sense Ground for DACs 8 and 9. VOUT8 and VOUT9 are referenced to this voltage.
REFGNDB1	Device Sense Ground for DACs 10 to 17. VOUT10 to VOUT17 are referenced to this voltage.
REFGNDB2	Device Sense Ground for DACs 18 and 19. VOUT18 and V_{OUT}19 are referenced to this voltage.
REFGNDC1	Device Sense Ground for DACs 20 to 27. VOUT20 to VOUT27 are referenced to this voltage.
REFGNDC2	Device Sense Ground for DACs 28 and 29. VOUT28 and VOUT29 are referenced to this voltage.
REFGNDD1	Device Sense Ground for DACs 30 to 37. VOUT30 to VOUT37 are referenced to this voltage.
REFGNDD2	Device Sense Ground for DACs 38 and 39. VOUT38 and VOUT39 are referenced to this voltage.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in Least Significant Bits.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register.
Ideally, with all 0s loaded to the DAC and m = all 1s,
c = 10 0000 0000 0000:

$$VOUT_{(Zero\text{-}Scale)} = 2.5 \times (V_{REF}(-) - AGND) + REFGND$$

Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It is mainly due to offsets in the output amplifier.

Full-Scale Error

Full-scale error is the error in DAC output voltage when all 1s are loaded into the DAC register.
Ideally, with all 1s loaded to the DAC and m = all 1s,
c = 10 0000 0000 0000:

$$VOUT_{(Full\text{-}Scale)} = 3.5 \times (V_{REF}(+) - AGND) + 2.5 \times (V_{REF}(-) - AGND) + REFGND$$

Full-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It does not include zero-scale error.

Gain Error

Gain Error is defined as the difference between Full-Scale Error and Zero-Scale Error. It is expressed in mV.

Gain Error = Full-Scale Error – Zero-Scale Error

DC Output Impedance

This is the effective output source resistance. It is dominated by package lead resistance.

DC Crosstalk

Although the common input reference voltage signals are internally buffered, small IR drops in the individual DAC reference inputs across the die can mean that an update to one channel can produce a dc output change in one or other of the channel outputs.

The forty DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or other channel outputs. This effect is more significant at high load currents and reduces as the load currents are reduced. With high impedance loads the effect is virtually unmeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize DC crosstalk.

Output Voltage Settling Time

This is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy

This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 1FFFHex and 2000Hex.

Channel-to-Channel Isolation

Channel-to-channel isolation refers to the proportion of input signal from one DACs reference input that appears at the output of another DAC operating from another reference. It is expressed in dBs.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is defined as the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog O/P change at another converter. It is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(Hz)^{1/2}$.

FUNCTIONAL DESCRIPTION

DAC Architecture — General

The AD5379 contains 40 DAC channels and 40 output amplifiers in a single package. The architecture of a single DAC channel consists of a 14-bit resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, each of value R, from $V_{REF}(+)$ to AGND. This type of architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier translates the output of the DAC to a wider range. The DAC output is gained up by a factor of 3.5 and offset by the voltage on the $V_{REF}(-)$ pin. See the section on Transfer Function.

Channel Groups

The 40 DAC channels on the AD5379 are arranged in 4 groups (A, B, C, D) of 10 channels. In each group there are 8 channels connected to $V_{REF}1(+)$ and $V_{REF}1(-)$ and the remaining 2 channels are connected to $V_{REF}2(+)$ and $V_{REF}2(-)$. Each group has 2 individual REFGND pins e.g. in Group A there are 8 channels connected to REFGNDA1 and the remaining 2 channels are connected to REFGNDA2.

In addition to an input register (x1) and a DAC register (x2), each channel has a gain register (m) and an offset register (c). See Tables IX, X and XI.

Table I shows the reference inputs and REFGND inputs, m and c registers for Group A. Groups B, C and D are similar.

Table I. Group A

Channel	Reference	REFGND	m, c Registers
0..7	$V_{REF}1(+)$, $V_{REF}1(-)$	REFGNDA1	m REG0..7 c REG0..7
8..9	$V_{REF}2(+)$, $V_{REF}2(-)$	REFGNDA2	m REG8..9 c REG8..9

Transfer Function

The digital input transfer function for each DAC can be represented as:

$$x2 = [(m + 1)/2^{13} \times x1] + c$$

x2 is the Dataword loaded to the resistor string DAC (default is 10 0000 0000 0000)
x1 is the 14-bit Dataword written to the DAC input register (default is 10 0000 0000 0000)
m is the 13-bit Gain Coefficient (default is 1 1111 1111 1111)
c is the 14-bit Offset Coefficient (default is 10 0000 0000 0000)

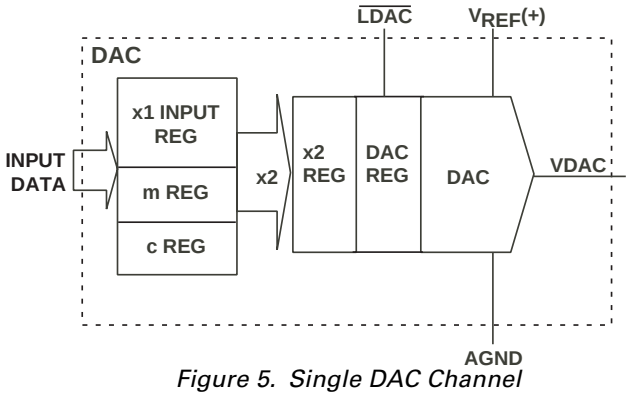


Figure 5. Single DAC Channel

Figure 5 shows a single DAC channel and its associated registers. The power-on values for the m and c registers are full-scale and 2000H respectively. The user can individually adjust the voltage range on each DAC channel by over-writing the power-on values of m and c. The AD5379 has digital overflow and underflow detection circuitry to clamp the DAC output at full-scale or zero-scale when the values chosen for x1, m and c result in x2 being out of range.

The complete transfer function for the AD5379 can be represented as:

$$VOUT = 3.5 \times ((V_{REF}(+) - AGND) \times x2/2^{14}) + 2.5 \times (V_{REF}(-) - AGND) + REFGND$$

x2 is the Dataword loaded to the resistor string DAC
$V_{REF}(+)$ is the voltage at the positive reference pin
$V_{REF}(-)$ is the voltage at the negative reference pin

Figure 6 shows the output amplifier stage of a single channel. VDAC is the voltage output from the resistor-string DAC. The nominal range of VDAC is 1 LSB to full-scale.

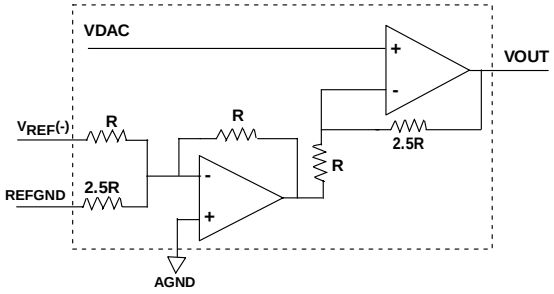


Figure 6. Output Amplifier Stage

V_{BIAS} Function

The AD5379 has an on-chip voltage-generator which provides a bias voltage of 4.25 V (min). The V_{BIAS} pin provides access to this voltage:

For $V_{REF}(+) < 4.25$ V the on-chip bias generator should be used and the V_{BIAS} pin must be decoupled externally with a 10 nF capacitor.

For $V_{REF}(+) > 4.25$ V, V_{BIAS} must be over-driven externally by an equal or higher voltage. The external voltage source should be capable of driving a 50 uA (typ) current sink load.

Reference Selection

The voltages applied to $V_{REF}(+)$ and $V_{REF}(-)$ determine the output voltage range and span on VOUT0-VOUT39. If the offset and gain features are not used (m and c are left at their power-on values), the reference levels required can be calculated as follows:

$$V_{REF}(+)_{min} = (VOUT_{max} - VOUT_{min}) / 3.5$$
$$V_{REF}(-)_{max} = (AGND + VOUT_{min}) / 2.5$$

If the offset and gain features of the AD5379 are used, then the output range required is slightly different. The reference levels required can be calculated as follows:

- Identify the nominal output range on VOUT.
- Identify the maximum offset span and the maximum gain required on the full output signal range.
- Calculate the new maximum output range on VOUT.
- Choose the new "$VOUT_{max}$" and "$VOUT_{min}$" required, keeping the new VOUT limits centred on the nominal values and assuming REFGND is zero (or equal to AGND). Note that V_{DD} and Vss must provide sufficient headroom.

- Calculate the values of $V_{REF}(+)$ and $V_{REF}(-)$ as follows:
  $V_{REF}(+)_{min} = (VOUT_{max} - VOUT_{min}) / 3.5$
  $V_{REF}(-)_{max} = (AGND + VOUT_{min}) / 2.5$

Reference Selection Example

Nominal output range = 10 V; (-2 V to 8 V)
Offset Error = ± 100 mV;
Gain Error = ± 3%;
REFGND = AGND = 0 V;

1) Gain Error = ± 3%;
=> Maximum Positive Gain Error = + 3%
=> Output Range incl. gain error = 10 + 0.03 (10) = 10.3 V

2) Offset Error = ± 100 mV;
=> Maximum Offset Error Span = 2(100) mV = 0.2 V
=> Output Range incl. gain error and offset error
= 10.3 + 0.2 = 10.5 V

3) $V_{REF}(+)$ and $V_{REF}(-)$ Calculation:
Actual Output range = 10.5 V i.e. -2.25 V to 8.25 V (centred);
=> $V_{REF}(+) = (8.25 + 2.25) / 3.5 = 3$ V
$V_{REF}(-) = -2.25 / 2.5 = -0.9$ V

If the solution yields inconvenient reference levels, the user can adopt one of three approaches:
(1) Use a resistor divider to divide down a convenient, higher reference level to the required level.
(2) Select convenient reference levels above $V_{REF}(+)_{min}$ or below $V_{REF}(-)_{max}$. Modify the gain and offset registers to down-size the references digitally. In this way, the user can use almost any convenient reference level, but may reduce performance by over-compaction of the transfer function.
(3) Use a combination of these two approaches.

AD5379 Calibration

The user can perform a system-calibration by overwriting the default values in the m and c registers for any individual DAC channel as follows:
- Calculate the nominal offset and gain coefficients for the new output range (see previous example)
- Calculate the new m and c values for each channel based on the specified offset and gain errors.

Calibration Example

Nominal Offset Coefficient = 0
Nominal Gain Coefficient = 10/10.5 × 8191 = 0.95238 × 8191 = 7801

Example 1: Channel 0, Gain Error = +3%, Offset Error = +100 mV
1) Gain Error (+3%) Calibration:
7801 × 1.03 = 8035
=> Load Code "1 1111 0110 0011" to m Register 0

2) Offset Error (+100 mV) Calibration:
LSB size = 10.5 / 16384 = 641 µV;
Offset Coefficient for +100 mV offset = 100 / 0.64 = 156 LSBs
=> Load "10 0000 1001 1100" to c Register 0

Example 2: Channel 1, Gain Error = -3%, Offset Error = -100 mV
1) Gain Error (-3%) Calibration:
7801 × 0.97 = 7567
=> Load Code "1 1110 1000 1111" to m Register 1

2) Offset Error (-100 mV) Calibration:
LSB size = 10.5 / 16384 = 641 µV;
Offset Coefficient for -100 mV offset = -100 / 0.64 = -156 LSBs
=> Load "01 1111 0110 0100" to c Register 1

INTERFACES

The AD5379 contains both a parallel and a serial interface. The active interface is selected via the SER/$\overline{PAR}$ pin.

The AD5379 uses an internal FIFO memory to allow high speed successive writes. The user can continue writing new data to the AD5379 while write instructions are being executed. The $\overline{BUSY}$ signal goes low while instructions in the FIFO are being executed. Up to 120 successive intructions can be written to the FIFO at maximum speed in parallel mode. When the FIFO is full any further writes to the AD5379 are ignored.

To minimize both the power consumption of the device and on-chip digital noise, the active interface only powers up fully when the device is being written to, i.e. on the falling edge of $\overline{WR}$ or on the falling edge of $\overline{SYNC}$.

Parallel Interface

The SER/$\overline{PAR}$ pin must be tied low to enable the parallel interface and disable the serial interface. Figure 2 shows the timing diagram for a parallel write to the AD5379. The parallel interface is controlled by the following pins:

$\overline{CS}$ Pin

Active low device select pin.

$\overline{WR}$ Pin

On the rising edge of $\overline{WR}$, with $\overline{CS}$ low, the address values at pins A7-A0 are latched and data values at pins DB13-DB0 are loaded into the selected AD5379 input registers.

REG1, REG0 Pins

The REG1 and REG0 pins determine the destination register of the data being written to the AD5379. See Table II.

Table II. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Register

DB13-DB0 Pins

The AD5379 accepts a straight 14-bit parallel word on DB0-DB13 where DB13 is the MSB and DB0 is the LSB. See Tables IV, V, VI, VII and VIII.

A7-A0 Pins

Each of the 40 DAC channels can be addressed individually. There are also several channel groupings which enable the user to simultaneously write the same data to multiple DAC channels. Address bits A7-A4 are decoded to select one group or multiple groups of registers. Address bits A3-A0 select one of ten input data registers (x1), offset registers (c) or gain registers (m). See Tables IX, X and XI.

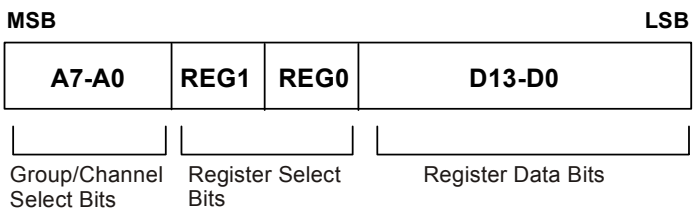


Figure 7. Serial Data Format

Serial Interface

The SER/$\overline{PAR}$ pin must be tied high to enable the serial interface and disable the parallel interface. The serial interface is controlled by five pins as follows:

$\overline{SYNC}$, DIN, SCLK - Standard 3-wire interface pins.

DCEN - Selects Stand-Alone Mode or Daisy-Chain Mode.

SDO - Data Out pin for Daisy-Chain Mode.

Figures 3 and 4 show the timing diagram for a serial write to the AD5379 in both Stand-Alone and Daisy-Chain Mode.

The 24-bit data word format for the serial interface in shown in Figure 7.

Stand-Alone Mode

By connecting DCEN (Daisy-Chain Enable) pin low, Stand-Alone Mode is enabled. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{SYNC}$ starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{SYNC}$ are ignored until 24 bits are shifted in. Once 24 bits have been shifted in, the SCLK is ignored. In order for another serial transfer to take place the counter must be reset by the falling edge of $\overline{SYNC}$.

Daisy-Chain Mode

For systems which contain several DACs the SDO pin may be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and reducing the number of serial interface lines.

By connecting DCEN (Daisy-Chain Enable) pin high, the Daisy-Chain Mode is enabled. The first falling edge of $\overline{SYNC}$ starts the write cycle. The SCLK is continuously applied to the input shift register when $\overline{SYNC}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next device in the chain, a multi-device interface is constructed. 24 clock pulses are required for each AD5379 in the system. Therefore, the total number of clock cycles must equal 24N where N is the total number of AD5379 devices in the chain.

When the serial transfer to all devices is complete, $\overline{SYNC}$ should be taken high. This latches the input data in each device in the daisy-chain and prevents any further data being clocked into the input shift register.

A continuous SCLK source may be used if it can be arranged that $\overline{SYNC}$ is held low for the correct number of clock cycles. Alternatively, a burst clock containing the exact number of clock cycles may be used and $\overline{SYNC}$ taken high some time later.

When the transfer to all input registers is complete, a common $\overline{LDAC}$ signal updates all DAC registers and all analog outputs are updated simultaneously.

ADDITIONAL FUNCTIONS

Clear Function

The clear function on the AD5379 can be implemented by using analog or digital control.

1) Bringing the $\overline{CLR}$ line low switches the outputs, VOUT0-VOUT39 to the externally set potential on the REFGND pin. This is achieved by switching in REFGND and re-configuring the output amplifier stages. The contents of the input registers and DAC registers are not affected by taking $\overline{CLR}$ low. When $\overline{CLR}$ is brought high, the DAC outputs remain cleared until $\overline{LDAC}$ is taken low. While $\overline{CLR}$ is low the value of $\overline{LDAC}$ is ignored.

2) Loading a clear code to the x1 registers also enables the user to set VOUT0 to VOUT39 to the REFGND level. The Default Clear Code corresponds to m at full-scale and c at mid-scale (i.e. x2 = x1).

Default Clear Code

$= 2^{14} \times (-Output\ Offset) / (Output\ range)$

$= 2^{14} \times 2.5 \times (AGND - V_{REF}(-)) / (3.5 \times (V_{REF}(+) - AGND))$

The more general expression for the Clear Code is as follows:

$Clear\ code = (2^{14})/(m+1) \times (Default\ Clear\ Code - c\ )$

$\overline{BUSY}$ and $\overline{LDAC}$ Functions

The value of x2 is calculated each time the user writes new data to the corresponding x1, c or m registers. During the calculation of x2 the $\overline{BUSY}$ output goes low. While $\overline{BUSY}$ is low the user can continue writing new data to the x1, m or c registers but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{LDAC}$ input low. If $\overline{LDAC}$ goes low while $\overline{BUSY}$ is active, the $\overline{LDAC}$ event is stored and the DAC outputs update immediately after $\overline{BUSY}$ goes high. A user may also hold the $\overline{LDAC}$ input permanently low. In this case the DAC outputs update immediately after $\overline{BUSY}$ goes high.

The value of x2 for a single channel or group of channels is re-calculated each time there is a write to any x1 register(s), c register(s) or m register(s). During the calculation of x2 $\overline{BUSY}$ goes low. The duration of this $\overline{BUSY}$ pulse depends on the no. of channels being updated e.g. if x1, c or m data is written to one DAC channel, $\overline{BUSY}$ goes low for 900 ns (max). However if data is written to two DAC channels, $\overline{BUSY}$ goes low for 1250 ns (max). Note there is 500 ns overhead due to FIFO access. See Table III.

The AD5379 contains an extra feature whereby a DAC register is not updated unless it's x2 register has been written to since the last time $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However the AD5379 will only update the DAC register if the x2 data has changed, thereby removing unnecessary digital crosstalk.

Table III. $\overline{BUSY}$ Pulsewidth

Action	$\overline{BUSY}$ Pulsewidth	
Loading x1 or c or m to 1 Channel	900	ns (max)
Loading x1 or c or m to 2 Channels	1250	ns (max)
Loading x1 or c or m to 3 Channels	1600	ns (max)
Loading x1 or c or m to 4 Channels	1950	ns (max)
Loading x1 or c or m to all 40 Channels	14550	ns (max)

$\overline{\text{BUSY}}$ Input Function

Since the $\overline{\text{BUSY}}$ pin is bi-directional and open-drain, a second AD5379 or any other device (e.g. system controller), can pull $\overline{\text{BUSY}}$ low and therefore delay DAC update(s), if required. This is a means of holding off any $\overline{\text{LDAC}}$ action. This feature allows synchronous updates of multiple AD5379 devices in a system at maximum speed. As soon as the last device connected to the $\overline{\text{BUSY}}$ pin is ready, all DACs will update automatically. Tying the $\overline{\text{BUSY}}$ pin of multiple devices together enables synchronous updating of all DACs without the addition of extra hardware.

Power-On-Reset

The AD5379 contains a power-on-reset generator and state-machine. During power-on $\overline{\text{CLR}}$ becomes active (internally), the power-on state-machine resets all internal registers to their default values and $\overline{\text{BUSY}}$ goes low. This sequence takes 10 ms (typ). The outputs, VOUT0-VOUT39 are switched to the externally set potential on the REFGND pin. During power-on the parallel interface is disabled so it is not possible to write to the part. Any transitions on $\overline{\text{LDAC}}$ during the power-on period will be ignored in order to reject initial $\overline{\text{LDAC}}$ pin glitching. A rising edge on $\overline{\text{BUSY}}$ indicates that power-on is complete and that the parallel interface is enabled. All DACs remain in their power-on state until $\overline{\text{LDAC}}$ is used to update the DAC outputs as described above.

$\overline{\text{RESET}}$ Input Function

The AD5379 can be placed in its power-on-reset state at any time by activating the $\overline{\text{RESET}}$ pin. The AD5379 state-machine initiates a reset sequence to digitally reset x1, m, c and x2 registers to their default power-on values. This sequence takes 100 µs (typ) and during this sequence $\overline{\text{BUSY}}$ goes low. While $\overline{\text{RESET}}$ is low any transitions on $\overline{\text{LDAC}}$ will be ignored. As with the $\overline{\text{CLR}}$ input, while $\overline{\text{RESET}}$ is low the DAC outputs are switched to REFGND.

This reset function can also be implemented via the parallel interface by setting REG0 and REG1 pins low and writing all 1s to DB13-DB0 (see Table VIII for Soft-Reset).

Increment/Decrement Function

The AD5379 has a Special Function Register which enables the user to increment or decrement the internal 13-Bit Input Register data (x1) in steps of 0 to 127 LSBs. The increment/decrement mode is selected by setting both REG1 and REG0 pins (or bits) low. The address pins (or bits) A7-A0 are used to select a DAC channel or a group of channels.

The amount by which the x1 is incremented/decremented is determined by bits/pins DB6-DB0 e.g. for a 1 LSB increment/decrement DB6..DB0 = 0000001 while for a 7 LSB increment/decrement, DB6...DB0 = 0000111. DB8 determines whether the Input Register data is incremented (DB8 = 1) or decremented (DB8 = 0). The maximum amount by which the user is allowed to increment or decrement the data is 127 LSBs i.e DB6...DB0 = 1111111. The 0 LSB step is included to facilitate software loops in the user's application. See Table VII.

The AD5379 has digital overflow and underflow detection circuitry to clamp at full-scale or zero-scale when the values chosen for increment or decrement mode are out of range.

DATA DECODING

The AD5379 contains a 14-bit data bus, DB13-DB0. Depending on the value of REG1 and REG0, this data is loaded into the addressed DAC input register(s), Offset (c) register(s), Gain (m) register(s) or the Special Function register.

Table IV. DAC Data format (REG1 = 1, REG0 = 1)

DB13 to DB0	DAC Output
11 1111 1111 1111	$(16383/16384)V_{REF}(+)$ V
11 1111 1111 1110	$(16382/16384)V_{REF}(+)$ V
10 0000 0000 0001	$(8193/16384)V_{REF}(+)$ V
10 0000 0000 0000	$(8192/16384)V_{REF}(+)$ V
01 1111 1111 1111	$(8191/16384)V_{REF}(+)$ V
00 0000 0000 0001	$(1/16384)V_{REF}(+)$ V
00 0000 0000 0000	0 V

Table V. Offset Data format (REG1 = 1, REG0 = 0)

DB13 to DB0	Offset
11 1111 1111 1111	+8191 LSB
11 1111 1111 1110	+8190 LSB
10 0000 0000 0001	+1 LSB
10 0000 0000 0000	+0 LSB
01 1111 1111 1111	-1 LSB
00 0000 0000 0001	-8191 LSB
00 0000 0000 0000	-8192 LSB

Table VI. Gain Data format (REG1 = 0, REG0 = 1)

DB13 to DB1	Gain
1 1111 1111 1111	8192/8192
1 1111 1111 1110	8191/8192
1 0000 0000 0001	4098/8192
1 0000 0000 0000	4097/8192
0 1111 1111 1111	4096/8192
0 0000 0000 0001	2/8192
0 0000 0000 0000	1/8192

Table VII. Special Function Data format (REG1 = 0, REG0 = 0)

DB13 to DB0	Increment/Dccrement step
00000 10 1111111	+127 LSB
00000 10 0000111	+7 LSB
00000 10 0000001	+1 LSB
00000 X0 0000000	0 LSB
00000 00 0000001	-1 LSB
00000 00 0000111	-7 LSB
00000 00 1111111	-128 LSB

Table VIII. Soft-Reset (REG1 = 0, REG0 = 0)

DB12 to DB0	DAC Output
11 1111 1111 1111	REFGND

ADDRESS DECODING

The AD5379 contains an 8-bit address bus, A7-A0. This address bus allows each DAC input register (x1), each Offset (c) register and each Gain (m) register to be individually updated. Note when all 40 DAC channels are selected address bits A[3:0] are ignored.

Table IX. DAC Input Register (x1) Selection (REG1 = REG0 = 1)

A7	A6	A5	A4	Group
0	0	0	0	All 40 DACs
0	0	0	1	Group 1
0	0	1	0	Group 2
0	0	1	1	Group 1, 2
0	1	0	0	Group 3
0	1	0	1	Group 1, 3
0	1	1	0	Group 2, 3
0	1	1	1	Group 1, 2, 3
1	0	0	0	Group 4
1	0	0	1	Group 1, 4
1	0	1	0	Group 2, 4
1	0	1	1	Group 1, 2, 4
1	1	0	0	Group 3, 4
1	1	0	1	Group 1, 3, 4
1	1	1	0	Group 2, 3, 4
1	1	1	1	Group 1, 2, 3, 4

A3	A2	A1	A0	DATA REGISTER
0	0	0	0	Input Register 0 (with m, c, Registers 0)
0	0	0	1	Input Register 1 (with m, c, Registers 1)
0	0	1	0	Input Register 2 (with m, c, Registers 2)
0	0	1	1	Input Register 3 (with m, c, Registers 3)
0	1	0	0	Input Register 4 (with m, c, Registers 4)
0	1	0	1	Input Register 5 (with m, c, Registers 5)
0	1	1	0	Input Register 6 (with m, c, Registers 6)
0	1	1	1	Input Register 7 (with m, c, Registers 7)
1	0	0	0	Input Register 8 (with m, c, Registers 8)
1	0	0	1	Input Register 9 (with m, c, Registers 9)

Table X. DAC Offset Register (c) Selection (REG1 = 1, REG0 = 0)

A7	A6	A5	A4	Group
0	0	0	0	All 40 DACs
0	0	0	1	Group 1
0	0	1	0	Group 2
0	0	1	1	Group 1, 2
0	1	0	0	Group 3
0	1	0	1	Group 1, 3
0	1	1	0	Group 2, 3
0	1	1	1	Group 1, 2, 3
1	0	0	0	Group 4
1	0	0	1	Group 1, 4
1	0	1	0	Group 2, 4
1	0	1	1	Group 1, 2, 4
1	1	0	0	Group 3, 4
1	1	0	1	Group 1, 3, 4
1	1	1	0	Group 2, 3, 4
1	1	1	1	Group 1, 2, 3, 4

A3	A2	A1	A0	OFFSET REGISTER
0	0	0	0	Offset Register 0
0	0	0	1	Offset Register 1
0	0	1	0	Offset Register 2
0	0	1	1	Offset Register 3
0	1	0	0	Offset Register 4
0	1	0	1	Offset Register 5
0	1	1	0	Offset Register 6
0	1	1	1	Offset Register 7
1	0	0	0	Offset Register 8
1	0	0	1	Offset Register 9

Table XI. DAC Gain Register (m) Selection (REG1 = 0, REG0 = 1)

A7	A6	A5	A4	Group
0	0	0	0	All 40 DACs
0	0	0	1	Group 1
0	0	1	0	Group 2
0	0	1	1	Group 1, 2
0	1	0	0	Group 3
0	1	0	1	Group 1, 3
0	1	1	0	Group 2, 3
0	1	1	1	Group 1, 2, 3
1	0	0	0	Group 4
1	0	0	1	Group 1, 4
1	0	1	0	Group 2, 4
1	0	1	1	Group 1, 2, 4
1	1	0	0	Group 3, 4
1	1	0	1	Group 1, 3, 4
1	1	1	0	Group 2, 3, 4
1	1	1	1	Group 1, 2, 3, 4

A3	A2	A1	A0	GAIN REGISTER
0	0	0	0	Gain Register 0
0	0	0	1	Gain Register 1
0	0	1	0	Gain Register 2
0	0	1	1	Gain Register 3
0	1	0	0	Gain Register 4
0	1	0	1	Gain Register 5
0	1	1	0	Gain Register 6
0	1	1	1	Gain Register 7
1	0	0	0	Gain Register 8
1	0	0	1	Gain Register 9

Table XII. DAC Special Function Register Selection (REG1 = REG0 = 0)

A7	A6	A5	A4	Group
0	0	0	0	All 40 DACs
0	0	0	1	Group 1
0	0	1	0	Group 2
0	0	1	1	Group 1, 2
0	1	0	0	Group 3
0	1	0	1	Group 1, 3
0	1	1	0	Group 2, 3
0	1	1	1	Group 1, 2, 3
1	0	0	0	Group 4
1	0	0	1	Group 1, 4
1	0	1	0	Group 2, 4
1	0	1	1	Group 1, 2, 4
1	1	0	0	Group 3, 4
1	1	0	1	Group 1, 3, 4
1	1	1	0	Group 2, 3, 4
1	1	1	1	Group 1, 2, 3, 4

A3	A2	A1	A0	Inc/Dec REGISTER
0	0	0	0	Register 0
0	0	0	1	Register 1
0	0	1	0	Register 2
0	0	1	1	Register 3
0	1	0	0	Register 4
0	1	0	1	Register 5
0	1	1	0	Register 6
0	1	1	1	Register 7
1	0	0	0	Register 8
1	0	0	1	Register 9

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5379 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5379 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, V_{CC}) it is recommended to tie these pins together and to decouple each supply once.

The AD5379 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

Digital lines running under the device should be avoided as these will couple noise onto the device. The analog ground plane should be allowed to run under the AD5379 to avoid noise coupling. The power supply lines of the AD5379 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching digital signals should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. It is essential to minimize noise on all $V_{REF}(+)$ and $V_{REF}(-)$ lines. The V_{BIAS} pin should be decoupled with a 10 nF capacitor to AGND.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the CSPBGA package and to avoid a point load on the surface of this package during the assembly process.

Power On

An on chip power supply monitor makes the AD5379 robust to power sequencing. The supply monitor powers up the analog section after (V_{DD} - V_{SS}) is greater than 7V. The output buffers power up in $\overline{CLR}$ mode forced to the DUTGND potential even if V_{CC} remains at 0V. After V_{SS} is applied the analog circuitry powers up and the buffered DAC output level settles linearly within the supply range.

OUTLINE DIMENSIONS

Dimensions shown in mm and (inches).

108-Lead CSPBGA
(BC-108)