ANALOG DEVICES

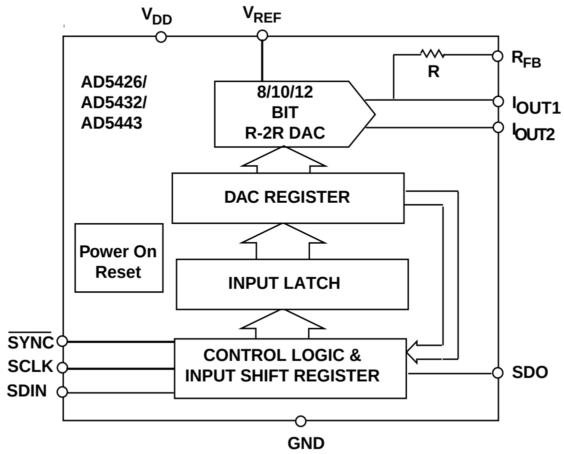
High Bandwidth CMOS 8/10/12-Bit Serial Interface Multiplying DACs

Preliminary Technical Data — AD5426/AD5432/AD5443*

FEATURES
- +2.5 V to +5.5 V Supply Operation
- 50MHz Serial Interface
- 10MHz Multiplying Bandwidth
- ±10V Reference Input
- Extended Temperature Range -40 °C to +125 °C
- 10-Lead MSOP Package
- Pin Compatible 8, 10 and 12 Bit Current Output DACs
- Guaranteed Monotonic
- Four Quadrant Multiplication
- Power On Reset with Brown out Detec
- Daisy Chain Mode
- Readback Function
- 0.4µA typical Power Consumption

APPLICATIONS
- Portable Battery Powered Applications
- Waveform Generators
- Analog Processing
- Instrumentation Applications
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Calibration
- Programmable Filters and Oscillators
- Composite Video
- Ultrasound
- Gain, offset and Voltage Trimming

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5426/AD5432/AD5443 are CMOS 8, 10 and 12-bit Current Output digital-to-analog converters respectively.

These devices operate from a +2.5 V to 5.5 V power supply, making them suited to battery powered applications and many other applications.

These DACs utilize double buffered 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE™ and most DSP interface standards. In addition, a serial data out pin (SDO) allows for daisy chaining when multiple packages are used. Data readback allows the user to read the contents of the DAC register via the SDO pin. On power-up, the internal shift register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS sub micron process, they offer excellent four quadrant multiplication characteristics, with large signal multiplying bandwidths of 10MHz.

The applied external reference input voltage (V_{REF}) determines the full scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full scale voltage output when combined with an external Current to Voltage precision amplifier.

The AD5426/AD5432/AD5443 DACs are available in small 10-lead MSOP packages.

PRODUCT HIGHLIGHTS

1. 10MHz Multiplying Bandwidth
2. 3mm x 5mm 10-lead MSOP package
3. Low Voltage, Low Power Current Output DACs.

*US Patent Number 5,689,257
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corporation.

Rev. PrK May 2003

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AD5426/AD5432/AD5443–SPECIFICATIONS[1]

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = +10 V, $I_{OUT}X$ = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted. DC performance measured with OP1177, AC performance with AD9631 unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Conditions
STATIC PERFORMANCE					
AD5426					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5432					
Resolution			10	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5443					
Resolution			12	Bits	
Relative Accuracy			±2	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
Gain Error			±2	mV	
Gain Error Temp Coefficient[2]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0000_H, T_A = 25°C, I_{OUT1}
			±50	nA	Data = 0000_H, I_{OUT1}
Output Voltage Compliance Range		TBD		V	
REFERENCE INPUT[2]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = -50ppm/°C
DIGITAL INPUTS/OUTPUT[2]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			1	μA	
Input Capacitance			10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} - 1			V	I_{SOURCE} = 200 μA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} - 0.5			V	I_{SOURCE} = 200 μA
DYNAMIC PERFORMANCE[2]					
Reference Multiplying BW	10			MHz	V_{REF} = 100 mV rms, DAC loaded all 1s
	TBD			MHz	V_{REF} = 6 V rms, DAC loaded all 1s
Output Voltage Settling Time					
AD5426		30	TBD	ns	Measured to ½ LSB. R_{LOAD} = 100Ω, C_{LOAD} = 15pF.
AD5432		35	TBD	ns	DAC latch alternately loaded with 0s and 1s.
AD5443		40	TBD	ns	
Slew Rate		100		V/μs	
Digital to Analog Glitch Impulse		3		nV-s	1 LSB change around Major Carry
Multiplying Feedthrough Error			-75	dB	DAC latch loaded with all 0s. Reference = 10kHz.
Output Capacitance			2	pF	DAC Latches Loaded with all 0s
			4	pF	DAC Latches Loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with $\overline{SYNC}$ high and Alternate Loading of all 0s and all 1s.
Total Harmonic Distortion		-85		dB	V_{REF} = 6 V rms, All 1s loaded, f = 1kHz
		-85		dB	V_{REF} = 5 V, Sinewave generated from digital code.
Output Noise Spectral Density		25		nV/√Hz	@ 1kHz
SFDR performance		72		dB	
Intermodulation Distortion		TBD		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}		0.4	10	μA	Logic Inputs = 0 V or V_{DD}
Power Supply Sensitivity[2]			0.001	%/%	ΔV_{DD} = ±5%

NOTES
[1]Temperature range is as follows: Y Version: –40°C to +125°C.
[2]Guaranteed by design and characterisation, not subject to production test.
Specifications subject to change without notice.

Single Supply Operation (Biased Mode)

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = + 2V, $I_{OUT}2$ = +1 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted. DC performance measured with OP1177, AC performance with AD9631 unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Conditions
STATIC PERFORMANCE					
AD5426					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5432					
Resolution			10	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5443					
Resolution			12	Bits	
Relative Accuracy			±2	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
Gain Error			±2	mV	
Gain Error Temp Coefficient[2]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0000_H, T_A = 25°C, I_{OUT1}
			±50	nA	Data = 0000_H, I_{OUT1}
Output Voltage Compliance Range		TBD		V	
REFERENCE INPUT[2]					
Reference Input Range		tbd		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = -50ppm/°C
DIGITAL INPUTS/OUTPUT[2]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance			10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 1			V	I_{SOURCE} = 200 µA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 0.5			V	I_{SOURCE} = 200 µA
DYNAMIC PERFORMANCE[2]					
Reference Multiplying BW	10			MHz	V_{REF} = 100 mV rms, DAC loaded all 1s
	TBD			MHz	V_{REF} = 1 V, DAC loaded all 1s
Output Voltage Settling Time					
AD5426		30	TBD	ns	Measured to ½ LSB. R_{LOAD} = 100Ω, C_{LOAD} = 15pF.
AD5432		35	TBD	ns	V_{REF} = 0V,DAC latch alternately loaded with 0s & 1s.
AD5443		40	TBD	ns	
Slew Rate		100		V/µs	
Digital to Analog Glitch Impulse		3		nV-s	1 LSB change around Major Carry
Multiplying Feedthrough Error			-75	dB	DAC latch loaded with all 0s. Reference = 10kHz.
Output Capacitance			2	pF	DAC Latches Loaded with all 0s
			4	pF	DAC Latches Loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with $\overline{SYNC}$ high and Alternate Loading of all 0s and all 1s.
Total Harmonic Distortion		-85		dB	V_{REF} = 2 Vp-p, 1V Bias, All 1s loaded, f = 1kHz
		-85		dB	V_{REF} = 2 V, Sinewave generated from digital code.
Output Noise Spectral Density		25		nV/√Hz	@ 1kHz
SFDR performance		72		dB	
Intermodulation Distortion		TBD		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}		0.4	10	µA	Logic Inputs = 0 V or V_{DD}
Power Supply Sensitivity[2]			0.001	%/%	ΔV_{DD} = ±5%

NOTES
[1]Temperature range is as follows: Y Version: –40°C to +125°C.
[2]Guaranteed by design and characterisation, not subject to production test.
Specifications subject to change without notice.

AD5426/AD5432/AD5443–SPECIFICATIONS[1]

TIMING CHARACTERISTICS[1] (V_{DD} = 2.5 V to 5.5 V, V_{REF} = +5 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
f_{SCLK}	50	MHz max	Max Clock frequency
t_1	20	ns min	SCLK Cycle time
t_2	8	ns min	SCLK High Time
t_3	8	ns min	SCLK Low Time
t_4[2]	13	ns min	$\overline{SYNC}$ falling edge to SCLK active edge setup time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	5	ns min	$\overline{SYNC}$ rising edge to SCLK active edge
t_8	30	ns min	Minimum $\overline{SYNC}$ high time
t_9[3]	25	ns min	SCLK Active edge to SDO valid

NOTES

[1]See Figures 1 & 2. Temperature range is as follows: Y Version: –40°C to +125°C. Guaranteed by design and characterisation, not subject to production test. All input signals are specified with tr =tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

[2]Falling or Rising edge as determined by control bits of Serial word.

[3]Daisychain and Readback modes cannot operate at max clock frequency. SDO timing specifications measured with load circuit as shown in Figure 3.

Specifications subject to change without notice.

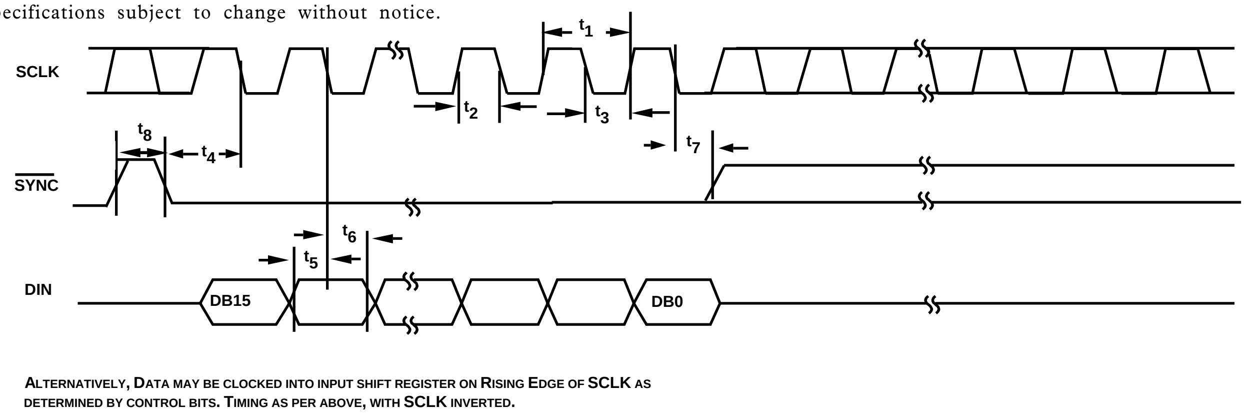


Figure 1. Stand Alone Mode Timing Diagram.

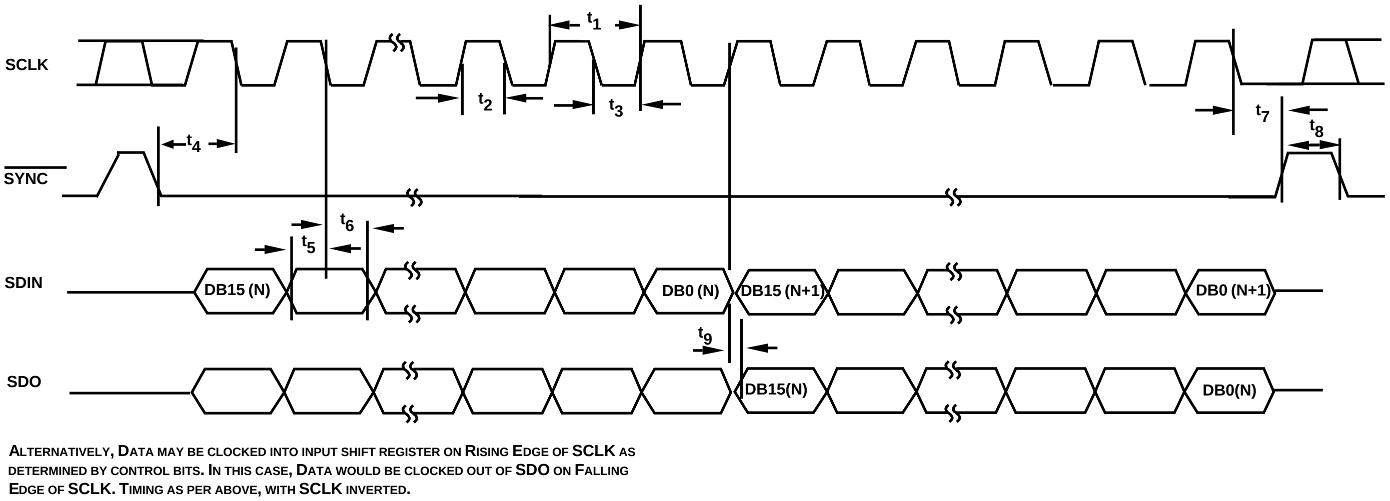


Figure 2. Daisy Chain and Readback Modes Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to +7 V
V_{REF}, R_{FB} to GND	–12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	–0.3 V to +7 V
Input Current to any pin except supplies	±10 mA
Logic Inputs & Output[3]	-0.3V to V_{DD} +0.3 V
Operating Temperature Range	
Extended Industrial (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
10 lead MSOP θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature (<20 seconds)	+235°C

NOTES

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

2 Transient currents of up to 100mA will not cause SCR latchup.

3 Overvoltages at SCLK, $\overline{SYNC}$, DIN, will be clamped by internal diodes. Current should be limited to the maximum ratings given.

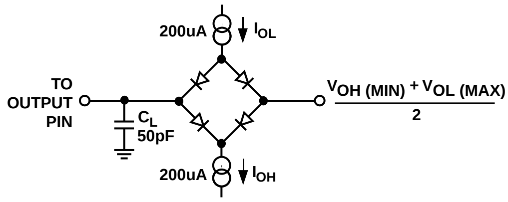


Figure 3. Load Circuit for SDO Timing Specifications

ORDERING GUIDE

Model	Resolution	INL (LSBs)	Temperature Range	Package Description	Branding	Package Option
AD5426YRM	8	±0.5	-40 °C to +125 °C	MSOP	D01	RM-10
AD5432YRM	10	±1	-40 °C to +125 °C	MSOP	D02	RM-10
AD5443YRM	12	±2	-40 °C to +125 °C	MSOP	D03	RM-10

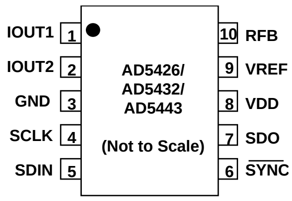
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5426/AD5432/AD5443 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	$I_{OUT}1$	DAC Current Output.
2	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	GND	Ground Pin.
4	SCLK	Serial Clock Input. By default, data is clocked into the input shift register on the falling edge of the serial clock input. Alternatively, by means of the serial control bits, the device may be configured such that data is clocked into the shift register on the rising edge of SCLK.
5	SDIN	Serial Data Input. Data is clocked into the 16-bit input register on the active edge of the serial clock input. By default, on power up, data is clocked into the shift register on the falling edge of SCLK. The control bits allow the user to change the active edge to rising edge.
6	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is loaded to the shift register on the active edge of the following clocks. In stand alone mode, the serial interface counts clocks and data is latched to the shift register on the 16th active clock edge.
7	SDO	Serial Data Output. This allows a number of parts to be daisychained. By default, data is clocked into the shift register on the falling edge and out via SDO on the rising edge of SCLK. Data will always be clocked out on the alternate edge to loading data to the shift register. Writing the Readback control word to the shift register makes the DAC register contents available for readback on the SDO pin, clocked out on the opposite edges to the active clock edge.
8	V_{DD}	Positive power supply input. These parts can be operated from a supply of +2.5 V to +5.5 V.
9	V_{REF}	DAC reference voltage input pin.
10	R_{FB}	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATION
MSOP



Typical Performance Characteristics

TPC 1. INL vs. Code (8-Bit DAC)

TPC 2. INL vs. Code (10-Bit DAC)

TPC 3. INL vs. Code (12-Bit DAC)

TPC 4. DNL vs. Code (8-Bit DAC)

TPC 5. DNL vs. Code (10-Bit DAC)

TPC 6. DNL vs. Code (12-Bit DAC)

TPC 7. INL vs Reference Voltage

TPC 8. DNL vs. Reference Voltage

TPC 9. Linearity Errors vs. V_{DD}

TPC10. INL vs Code - Biased Mode

TPC11. DNL vs Code - Biased Mode

TPC12. INL Error vs. Reference - Biased Mode

TPC 13. DNL Error vs. Reference - Biased Mode

TPC 14. TUE vs Code

TPC 15. Logic Threshold vs Supply Voltage

TPC 16. Supply Current vs Logic Input Voltage

TPC 17. Supply Current vs. Clock Freq

TPC 18. Reference Multiplying Bandwidth - small signal

TPC 19. Reference Multiplying Bandwidth - large signal

TPC 20. Reference Multiplying Bandwidth - small signal

TPC 21. Reference Multiplying Bandwidth - large signal

TPC 22. Settling Time

TPC 23. Midscale Transition and Digital Feedthrough

TPC 24. Power Supply Rejection vs Frequency

TPC 25. Noise Spectral Density vs Frequency

TPC 26. Glitch Impulse

TPC 27. TBD

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} – 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current

Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s

Output Capacitance

Capacitance from I_{OUT1} or I_{OUT2} to AGND.

Output Current Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full scale input change. For these devices, it is specifed with a 100 Ω resistor to ground.

Digital to Analog Glitch lmpulse

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device digital inputs is capacitivelly coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error

This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT1} terminal, when all 0s are loaded to the DAC.

Harmonic Distortion

The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonices are included, such as second to fifth.

$$THD = 20\log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}$$

Intermodulation Distortion

The DAC is driven by two combinded sine waves references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa±nfb where m, n = 0, 1, 2, 3... Intermodulation terms are those for which m or n is not equal to zero. The second order terms include (fa +fb) and (fa - fb) and the third order terms are (2fa + fb), (2fa -fb), (f+2fa + 2fb) and (fa - 2fb). IMD is defined as

$$IMD = 20\log \frac{\text{(rms sum of the sum and diff distortion products)}}{\text{rms amplitude of the fundamental}}$$

Compliance Voltage Range

The maximum range of (output) terminal voltage for which the device will provide the specified characteristics.

GENERAL DESCRIPTION

DAC SECTION

The AD5426, AD5432 and AD5443 are 8, 10 and 12 bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-Bit AD54246 is shown in Figure 4. The feedback resistor R_{FB} has a value of R. The value of R is typically 10kΩ (minimum 8kΩ and maximum 12kΩ). If I_{OUT1} and I_{OUT2} are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of value R. The DAC output (I_{OUT}) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

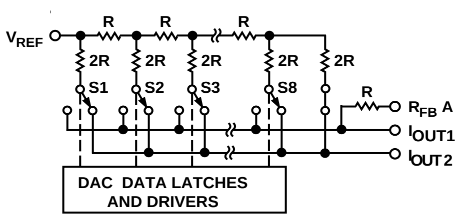


Figure 4. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, I_{OUT1} and I_{OUT2} terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, four quadrant multiplication in bipolar mode or in single supply modes of operation. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

SERIAL INTERFACE

The AD5426/AD5432/AD5443 have an easy to use 3-wire interface which is compatible with SPI/QSPI/MicroWire and DSP interface standards. Data is written to the device in 16 bit words. This 16-bit word consists of 4 control bits and either 8, 10 or 12 data bits as shown in Figure 5.The AD5443 uses all 12 bits of DAC data. The AD5432 uses ten bits and ignores the two LSBs, while the AD5426 uses eight bits and ignores the last four bits. As good programming practice, these ignored LSB's should be set to '0'.

Low Power Serial Interface

To minimize the power consumption of the device, the interface only powers up fully when the device is being written to, i.e., on the falling edge of $\overline{SYNC}$. The SCLK and DIN input buffers are powered down on the rising edge of $\overline{SYNC}$.

DAC Control Bits C3 - C0

Control bits C3 to C0 allow control of various functions of the DAC as can be seen in Table I. Default settings of the DAC on power on are as follows :
Data clocked into shift register on falling clock edges; Daisy chain mode is enabled. Device powers on with zeroscale load to the DAC register and I_{OUT} lines.
The DAC control bits allow the user to adjust certain features on power on, for example, Daisy chaining may be disabled if not in use, active clock edge may be changed to rising edge and DAC output may be cleared to either zero or midscale. The user may also initiate a readback of the DAC register contents for verification purposes.

DB15 (MSB) … DB0 (LSB)

C3	C2	C1	C0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0
CONTROL BITS				DATA BITS											

Figure 5a. AD5426 8 bit Input Shift Register Contents

DB15 (MSB) … DB0 (LSB)

C3	C2	C1	C0	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0
CONTROL BITS				DATA BITS											

Figure 5b. AD5432 10 bit Input Shift Register Contents

DB15 (MSB) … DB0 (LSB)

C3	C2	C1	C0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CONTROL BITS				DATA BITS											

Figure 5c. AD5443 12 bit Input Shift Register Contents

TABLE I. DAC CONTROL BITS

C3	C2	C1	C0	Funtion Implemented
0	0	0	0	No Operation (Power On Default)
0	0	0	1	Load and Update
0	0	1	0	Initiate Readback
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Daisy Chain Disable
1	0	1	0	Clock Data to shift register On Rising Edge
1	0	1	1	Clear DAC output to Zero
1	1	0	0	Clear DAC output to Midscale
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

$\overline{\text{SYNC}}$ Function

$\overline{\text{SYNC}}$ is an edge-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{\text{SYNC}}$ is low. To start the serial data transfer, $\overline{\text{SYNC}}$ should be taken low observing the minimum $\overline{\text{SYNC}}$ falling to SCLK falling edge setup time, t_4.

Daisy Chain Mode

Daisy Chain is the default power on mode. To disable the daisy chain function, write "1001" to control word. In Daisy-Chain Mode the internal gating on SCLK is disabled. The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 16 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK (this is the default, use the control word to change the active edge) and is valid for the next device on the falling edge (default). By connecting this line to the DIN input on the next device in the chain, a multidevice interface is constructed. 16 clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 16N where N is the total number of devices in the chain. See the timing diagram in Figure 3.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ should be taken high. This prevents any further data being clocked into the input shift register. A burst clock containing the exact number of clock cycles may be used and $\overline{\text{SYNC}}$ taken high some time later. After the rising edge of $\overline{\text{SYNC}}$, data is automatically transferred from each device's input shift register to the addressed DAC. When control bits = "0000", the device is in No Operation mode. This may be useful in daisy-chain applications where the user does not wish to change the settings of a particular DAC in the chain. Simply write "0000" to the Control bits for that DAC and the following data bits will be ignored.

Stand alone Mode

After power on, write "1001" to control word to disable Daisy Chain Mode. The first falling edge of $\overline{\text{SYNC}}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits are shifted in and out of the serial shift registers. A rising edge on $\overline{\text{SYNC}}$ during a write causes the write cycle to be aborted.
After the falling edge of the 16th SCLK pulse, data will automatically be transferred from the input shift register to the DAC. In order for another serial transfer to take place the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2 quadrant multiplying operation or a unipolar output voltage swing as shown in Figure 6.

When an output amplifier is connected in unipolar mode, the output voltage is given by:

$$V_{OUT} = -D/2^n \times V_{REF}$$

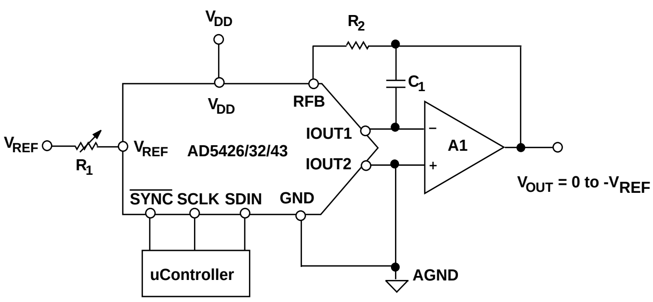
Where D is the fractional representation of the digital word loaded to the DAC, and n is the number of bits.

D = 0 to 255 (8-Bit AD5426)
= 0 to 1023 (10-Bit AD5432)
= 0 to 4095 (12-Bit AD5443)

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal digital logic to drive the DAC switches' ON and OFF states.

These DACs are also designed to accommodate ac reference input signals in the range of -10V to +10V.



NOTES:
[1]R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
[2]C1 PHASE COMPENSATION (1pF - 5pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 6. Unipolar Operation

With a fixed 10 V reference, the circuit shown above will give an unipolar 0V to -10V output voltage swing. When V_{IN} is an ac signal, the circuit performs two-quadrant multiplication.

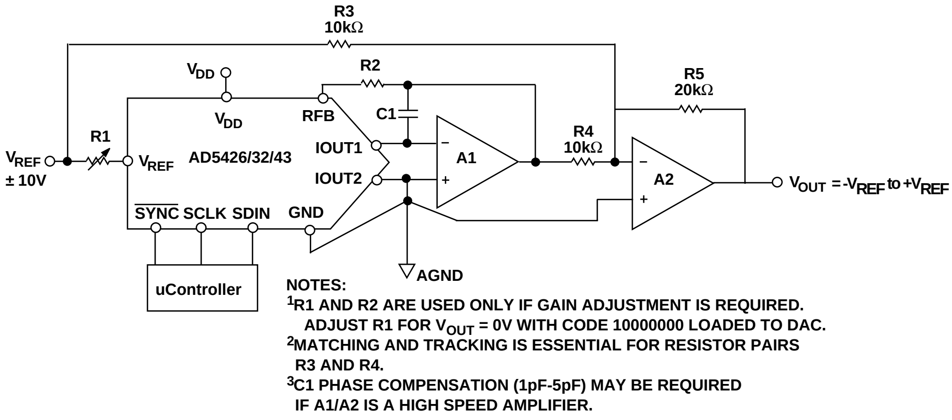


Figure 7. Bipolar Operation (4 Quadrant Multiplication)

The following table shows the relationship between digital code and expected output voltage for unipolar operation. (AD5426, 8-Bit device).

Table II. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Bipolar Operation

In some applications, it may be necessary to generate full 4-Quadrant multplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors as shown in Figure 7. In this circuit, the second amplifier A2 provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = - V_{REF}) to midscale (V_{OUT} - 0V) to full scale (V_{OUT} = + V_{REF}).

$$V_{OUT} = (V_{REF} \times D / 2^{n-1}) - V_{REF}$$

Where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

D = 0 to 255 (8-Bit AD5424)
= 0 to 1023 (10-Bit AD5433)
= 0 to 4095 (12-Bit AD5445)

When V_{IN} is an ac signal, the circuit performs four-quadrant multiplication.

Table III. shows the relationship between digital code and the expected output voltage for bipolar operation (AD5426, 8-Bit device).

Table III. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open loop response which can cause ringing or instability in the closed loop applications circuit.

An optional compensation capacitor, C1 can be added in parallel with R_{FB} for stability as shown in figures 6 and 7. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically but 1-2pF is generally adequate for the compensation.

SINGLE SUPPLY APPLICATIONS

Current Mode Operation

These DACs are specified and tested to guarantee operation in single supply applications. Figure 8 shows a typical circuit for operation with a single 2.5V to 5V supply. In the current mode circuit of Figure 8, I_{OUT2} and hence I_{OUT1} is biased positive by an amount V_{BIAS}.
In this configuration, the output voltage is given by

$$Vout = \{D \times (R_{FB}/R_{DAC}) \times (V_{BIAS} - V_{IN})\} + V_{BIAS}$$

As D varies from 0 to 255 (AD5426), 1023 (AD5432) or 4095 (AD5443), the output voltage varies from

$$V_{OUT} = V_{BIAS} \text{ to } V_{OUT} = 2\ V_{BIAS} - VIN.$$

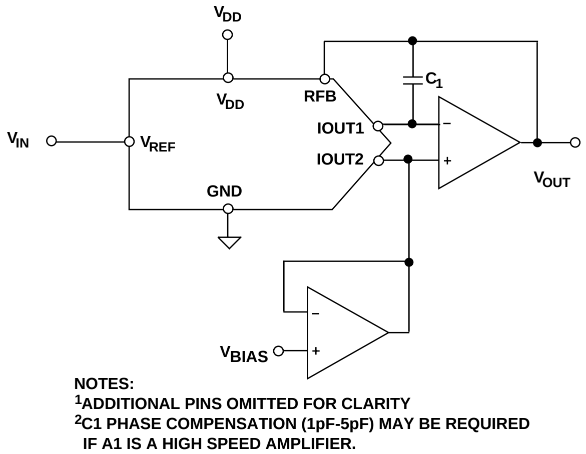


Figure 8. Single Supply Current Mode Operation.

V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the I_{OUT2} terminal without any problems.

Voltage Switching Mode of Operation

Figure 9 shows these DACs operating in the voltage-switching mode. The reference voltage, V_{IN} is applied to the I_{OUT1} pin, I_{OUT2} is connected to AGND and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage making single supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance). Thus an op-amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. So, the voltage input should be driven from a low impedance source.

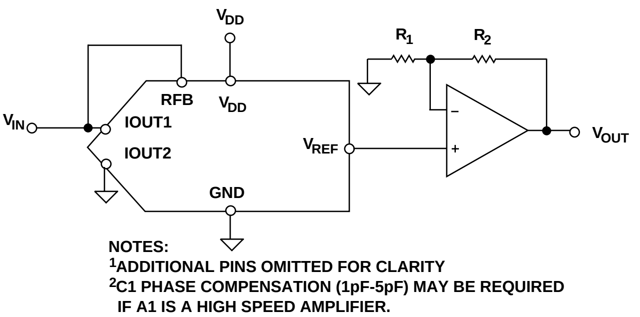


Figure 9. Single Supply Voltage Switching Mode Operation.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result their on resistance differs and this degrades the integral linearity of the DAC. Also, V_{IN} must not go negative by more than 0.3V or an internal diode will turn on, exceeding the max ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

POSITIVE OUTPUT VOLTAGE

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. In order to achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistors tolerance errors. To generate a negative reference, the reference can be level shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and -2.5V respectively as shown in Figure 10.

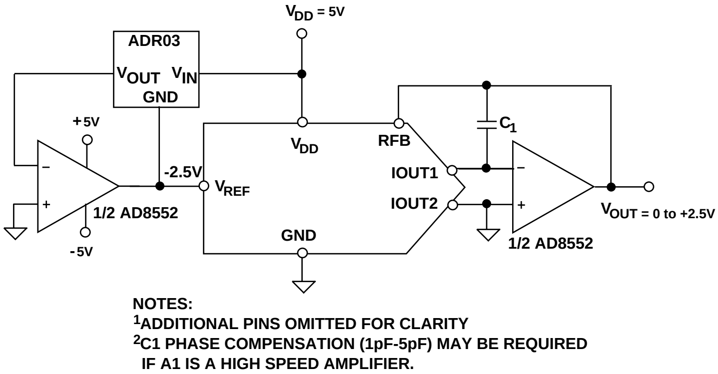


Figure 10. Positive Voltage output with minimum of components.

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can also be achieved in a single stage. It is important to take into consideration the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the RFB resistor will causing mis-matches in the Temperature coefficients resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 11 is a recommended method of increasing the gain of the circuit. R1, R2 and R3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of great than 1 are required.

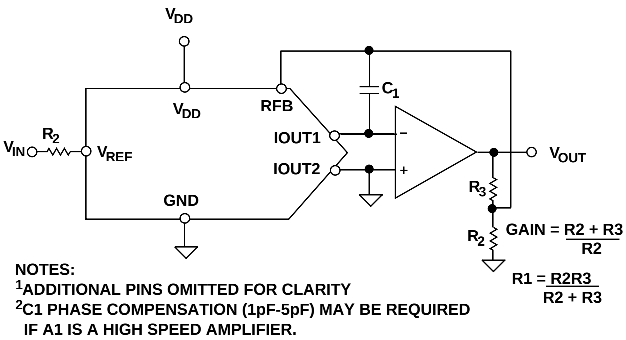


Figure 11. Increasing Gain of Current Output DAC

USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current Steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op-amp and R_{FB} is used as the input resistor as shown in Figure 12, then the output voltage is inversely proportional to the digital input fraction D. For D = $1-2^{n}$ the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1-2^{-n})$$

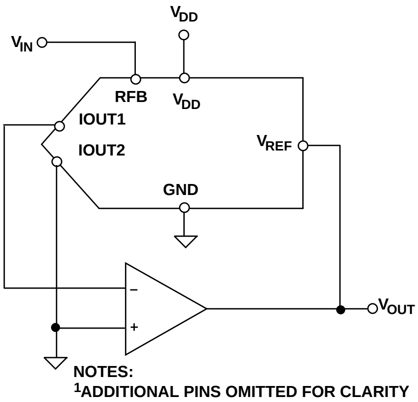


Figure 12. Current Steering DAC used as a divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the arnplifier does not saturate and also that the required accuracy is met. For example, an eight bit DAC driven with the binary code 10H (00010000), i.e., 16 decimal, in the circuit of Figure 12 should cause the output voltage to be sixteen times V_{IN}. However, if the DAC has a linearity specification of +/- 0.5LSB then D can in fact have the weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage will be in the range $15.5V_{IN}$ to $16.5V_{IN}$—an error of + 3% even though the DAC itself has a maximum error of 0.2%.

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction D of the current into the V_{REF} terminal is routed to the I_{OUT1} terminal, the output voltage has to change as follows:

Output Error Voltage Due to Dac Leakage

$$= (Leakage \times R)/D$$

where R is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10nA, R = 10 kilohm and a gain (i.e., 1/D) of 16 the error voltage is 1.6mV.

REFERENCE SELECTION

When selecting a reference for use with the AD5426 series of current output DACs, pay attention to the references output voltage temperature coefficient specification. This parameter not only affects the full scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1LSB over the temperature range 0-50°C dictates that the maximum *system drift* with temperature should be less than 78ppm/°C. A 12-Bit system with the same temperature range to overall specification within 2LSBs requires a maximum drift of 10ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized. Table IV. suggests some of the suitable references available from Analog Devices

Table IV. Listing of suitable ADI Precision References recommended for use with AD5426/32/43 DACs.

Reference	Output Voltage	Initial Tolerance	Temperature Drift	0.1Hz to 10Hz noise	Package
ADR01	10 V	0.1%	3ppm/°C	20µVp-p	SC70, TSOT, SOIC
ADR02	5 V	0.1%	3ppm/°C	10µVp-p	SC70, TSOT, SOIC
ADR03	2.5 V	0.2%	3ppm/°C	10µVp-p	SC70, TSOT, SOIC
ADR425	5V	0.04%	3ppm/°C	3.4µVp-p	MSOP, SOIC

Table V. Listing of some precision ADI Op Amps suitable for use with AD5426/32/43 DACs.

Part #	Max Supply Voltage V	V_{OS}(max)µV	I_B(max) nA	GBP MHz	Slew Rate V/µs	t_{SETTLE} with AD5443
OP97	±20	25	0.1	0.9	0.2	
OP1177	±18	60	2	1.3	0.7	
AD8551	±6	5	0.05	1.5	0.4	

Table VI. Listing of some High Speed ADI Op Amps suitable for use with AD5426/32/43 DACs.

Part #	Max Supply Voltage V	BW @ A_{CL} MHz	Slew Rate V/µs	t_{SETTLE} with AD5443	V_{OS}(max)µV	I_B(max) nA
AD8065	±12	145	180		1500	0.01
AD8021	±12	200	100		1000	1000
AD8038	±5	350	425		3000	0.75
AD9631	±5	320	1300		10000	7000

that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which if large enough could cause the DAC to be non-monotonic.

The input bias curent of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor R_{FB}. Most op amps have input bias currents low enough to prevent any significant errors in 12-Bit applications.

Common mode rejection of the op amp is important in voltage switching circuits, since it produces a code dependent error at the voltage output of the circuit. Most op amps have adequate common mode rejection for use at 8-, 10- and 12-Bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND) they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low inputs capacitance buffer amplifiers and careful board design.

Most single supply circuits include ground as part of the analog signal range, which in turns requires an ampliferthat can handle rail to rail signals, there is a large range of single supply amplifiers available from Analog Devices.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to this family of DACs is vias a serial bus that uses standard protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire interface consisting of a clock signal, a data signal and a synchronisation signal. The AD5426/32/43 requires a 16-Bit word with the default being data valid on the falling edge of SCLK, but this is changable via the control bits in the data word.

ADSP-21xx to AD5426/32/43 Interface

The ADSP-21xx family of DSPs are easily interface to this family of DACs without the need for extra glue logic. Figure 13. shows an example of an SPI interface between the DAC and the ADSP-2191M. SCK of the DSP drives the serial data line, DIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case $\overline{\text{SPIxSEL}}$.

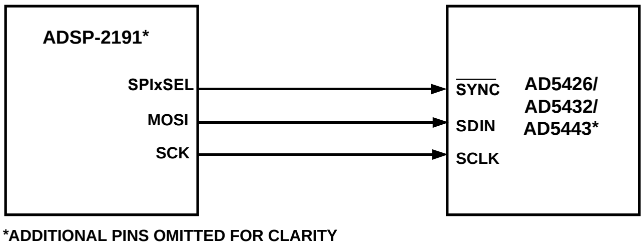


Figure 13. ADSP-2191 SPI to AD5426/AD5432/AD5443 Interface.

A serial interface between the DAC and DSP SPORT is shown in figure 14. In this interface example, SPORT0 is used to transfer data to the DAC shift register. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. In a write sequence, data is clocked out on each rising edge of the DSPs serial clock and clocked into the DAC input shift register on the falling edge of its SCLK. The update of the DAC output takes place on the rising edge of the $\overline{\text{SYNC}}$ signal.

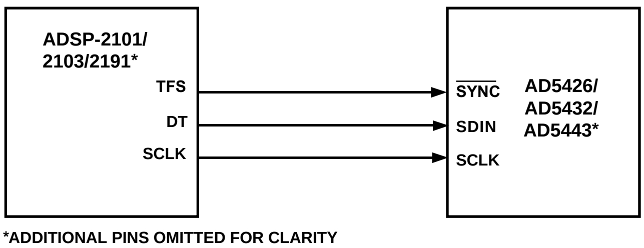


Figure 14. ADSP-2101/ADSP2013/ADSP2191 SPORT to AD5426/AD5432/AD5443 Interface.

Communication between two devices at a given clock speed is possible when the following specs are compatible: frame sync delay and frame sync setup and hold, data delay and data setup and hold, and SCLK width. The DAC interface expects a *t4* ($\overline{\text{SYNC}}$ falling edge to SCLK falling edge set-up time) of 13 ns minimum. Consult the ADSP-21xx User Manual for information on clock and frame sync frequencies for the SPORT Register.

The SPORT Control Register should be set up as follows:

TFSW = 1, Alternate Framing

INVTFS = 1, Active Low Frame Signal

DTYPE = 00, Right Justify Data

ISCLK = 1, Internal Serial Clock

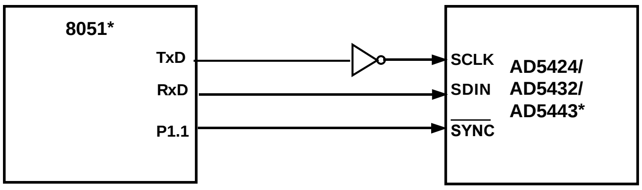
TFSR = 1, Frame Every Word

ITFS = 1, Internal Framing Signal

SLEN = 1111, 16-Bit Data-Word

80C51/80L51 to AD5426/AD5432/AD5443 Interface

A serial interface between the DAC and the 8051 is shown in Figure 15. TXD of the 8051 drives SCLK of the DAC serial interface, while RXD drives the serial data line, DIN. P3.3 is a bit-programmable pin on the serial port and is used to drive $\overline{SYNC}$. When data is to be transmitted to the switch, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data correctly to the DAC, P3.3 is left low after the first 8 bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result, no glue logic is required between the DAC and micro-controller interface. P3.3 is taken high following the completion of this cycle. The 8051 provides the LSB of its SBUF Register as the first bit in the data stream. The DAC input register requires its data with the MSB as the first bit received. The transmit routine should take this into account.

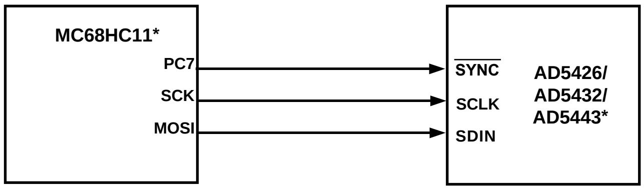


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 15. 80C51/80L51 to AD5426/AD5432/AD5443 interface

MC68HC11 Interface to AD5426/AD5432/AD5443 Interface

Figure 16 shows an example of a serial interface between the DAC and the MC68HC11 microcontroller.
The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see 68HC11 User Manual. SCK of the 68HC11 drives the SCLK of the DAC interface, the MOSI output drives the serial data line (D_{IN}) of the AD5516. The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5516, the $\overline{SYNC}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the DAC, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.



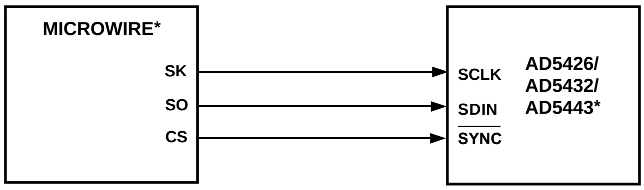
*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 16. 68HC11/68L11 to AD5426/AD5432/AD5443 interface.

If the user wishes to verify the data previously written to the input shift register, the SDO line could be connected to MISO of the MC68HC11, and with $\overline{SYNC}$ low, the shift register would clock data out on the rising edges of SCLK.

Microwire to AD5426/AD5432/AD5443 Interface

Figure 17 shows an interface between teh DAC and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock, SK, and is clocked into the DAC input shift register on the rising edge of SK, which corresponds to the falling edge of the DACs SCLK.

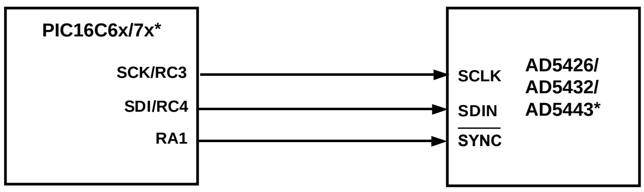


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 17. MICROWIRE to AD5426/AD5432/AD5443 Interface

PIC16C6x/7x to AD5426/AD5432/AD5443

The PIC16C6x/7x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit (CKP) = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user PIC16/17 Microcontroller User Manual. In this example I/O port RA1 is being used to provide a $\overline{SYNC}$ signal and enable the serial port of the DAC. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two consecutive write operations are required. Figure 18 shows the connection diagram.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 18. PIC16C6x/7x to AD5426/AD5432/AD5443 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5426/AD5432/AD5443 is mounted should be designed so that the analog and digital sections are separated, and cofined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a doublesided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize on high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

EVALUATION BOARD FOR THE AD5426/AD5432/ AD5443 SERIES OF DACS

The board consists of a 12-Bit AD5443 and a current to voltage amplifer AD8065. Included on the evaluation board is a 4V reference ADR425. An external reference may also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self installing PC software to control the DAC. The software simply allows the user to write a code to the device.

OPERATING THE EVALUATION BOARD

Power Supplies

The board requires +/-12V, and +5V supplies. The +12 V V_{DD} and Vss are used to power the output amplifier, while the +5V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10µF tantalum and 0.1µF ceramic capacitors.

Link1 (LK1) is provided to allow selection between the on board reference (ADR425) or an external reference applied through J2. For the AD5426/32/43 use Link2 in the SDO position.

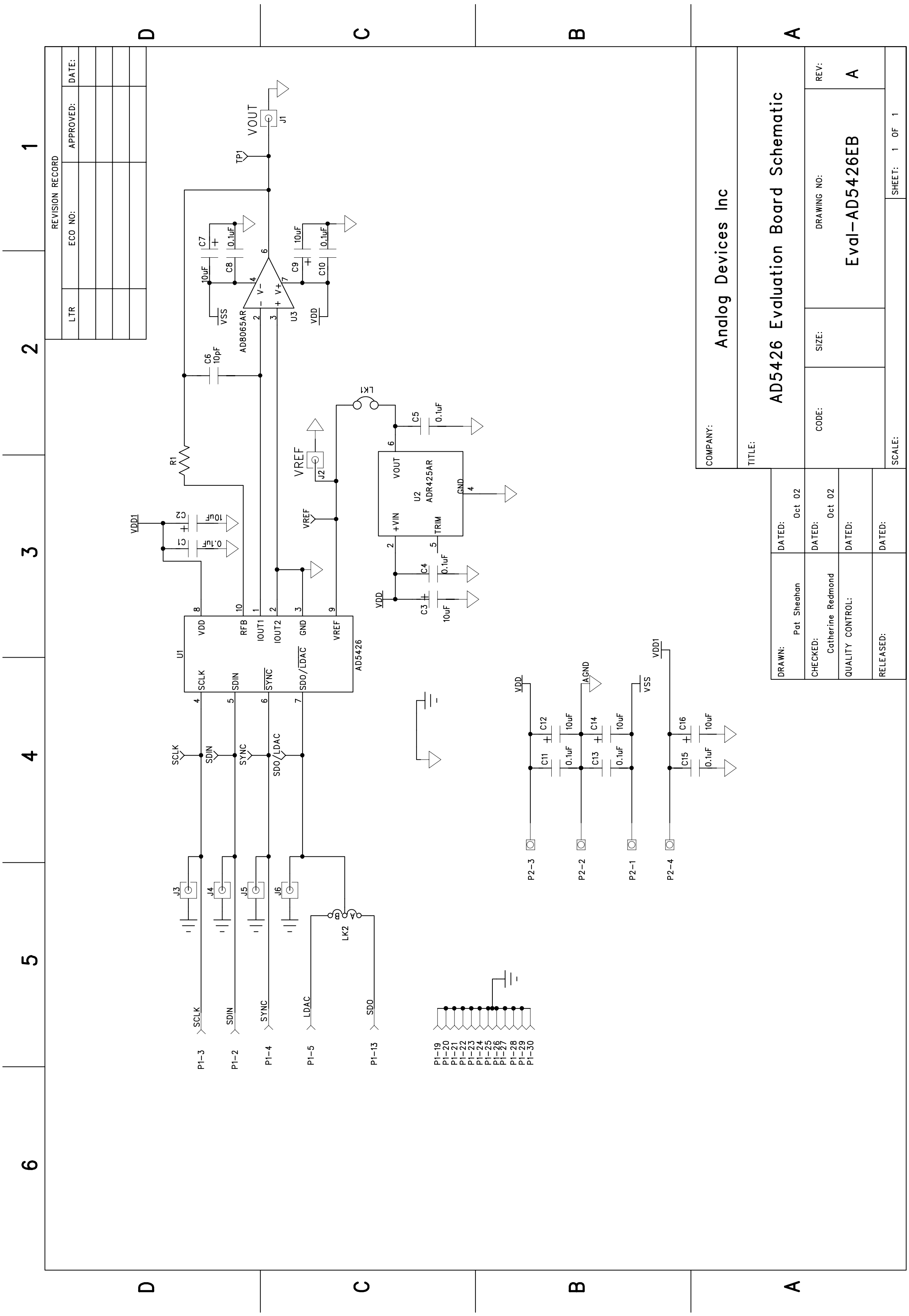
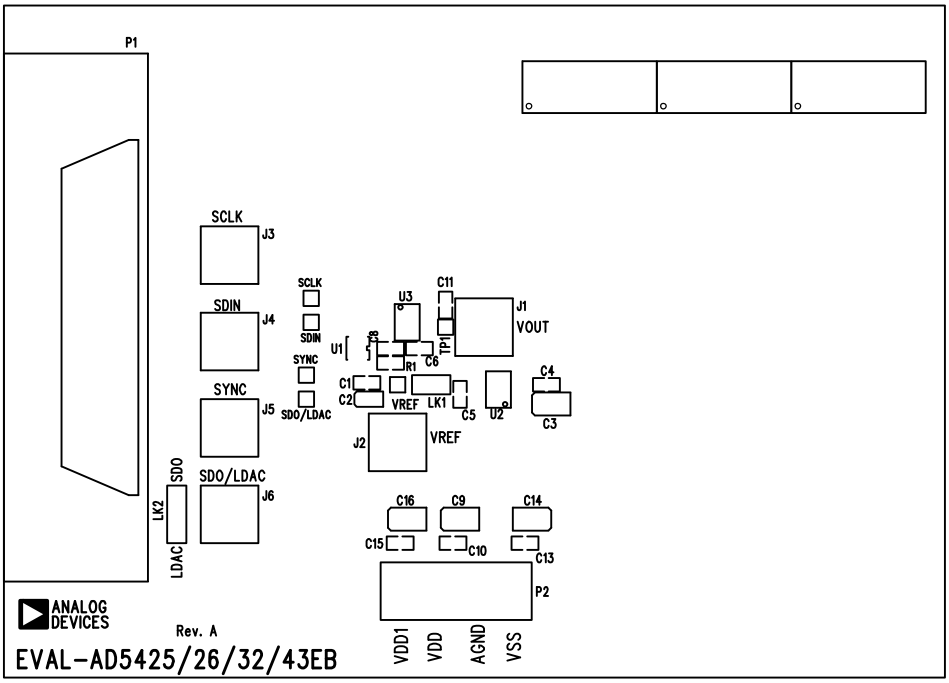
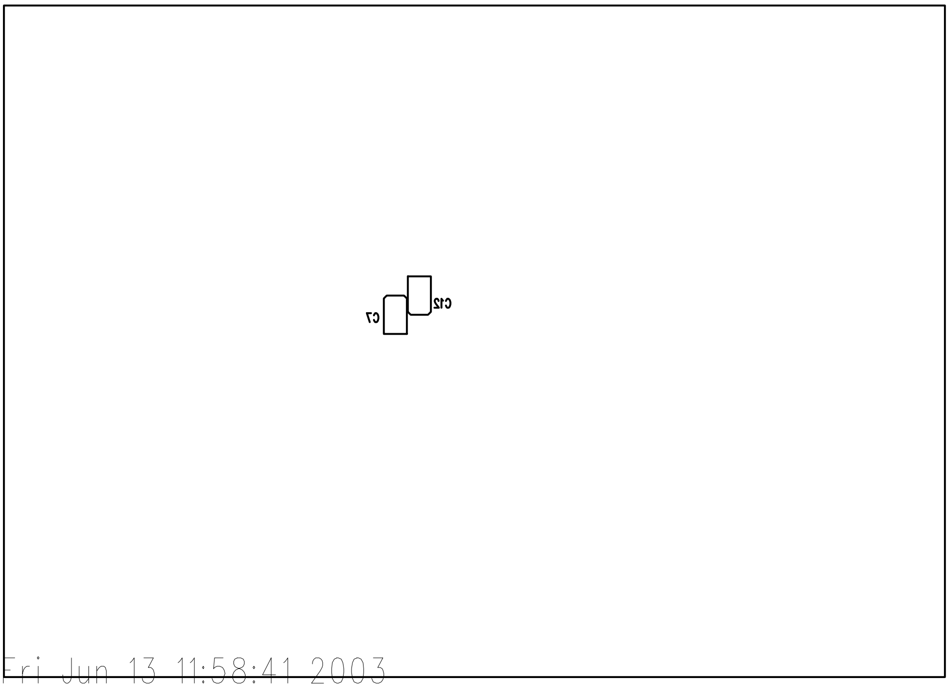


Figure 19. Schematic of AD5426/32/43 evaluation board.



Eval–AD5426EB (Rev. A) – Component Side View

Silkscreen



Eval–AD5426EB (Rev. A) – Component Side View

Figure 20. Silkscreen

Overview of AD54xx devices

Part #	Resolution	#DACs	INL	t_S	Interface	Package	Features
AD5403[1]	8	2	±0.5	20ns	Parallel	CP-40	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5410[1]	8	1	±0.5	20ns	Serial	RU-16	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5413[1]	8	2	±0.5	20ns	Serial	RU-24	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5424[2]	8	1	±0.5	20ns	Parallel	RU-16, CP-20	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5425[2]	8	1	±0.5	20ns	Serial	RM-10	Byte Load,10 MHz BW, 50 MHz Serial
AD5426[2]	8	1	±0.5	20ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5428[2]	8	2	±0.5	20ns	Parallel	RU-20	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5429[2]	8	2	±0.5	20ns	Serial	RU-10	10 MHz BW, 50 MHz Serial
AD5450[2]	8	1	±0.25	40ns	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5404[1]	10	2	±1	25ns	Parallel	CP-40	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5411[1]	10	1	±1	25ns	Serial	RU-16	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5414[1]	10	2	±1	25ns	Serial	RU-24	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5432[2]	10	1	±1	25ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5433[2]	10	1	±1	25ns	Parallel	RU-20, CP-20	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5439[2]	10	2	±1	25ns	Serial	RU-16	10 MHz BW, 50 MHz Serial
AD5440[2]	10	2	±1	25ns	Parallel	RU-24	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5451[2]	10	1	±0.25	40ns	Serial	RJ-8	10 MHz BW, 50 MHz Serial
AD5405[2]	12	2	± 2	30ns	Parallel	CP-40	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5412[1]	12	1	±2	30ns	Serial	RU-16	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5415[2]	12	2	±2	30ns	Serial	RU-24	10 MHz BW, 50 MHz Serial, 4- Quadrant Multiplying Resistors
AD5443[2]	12	1	± 2	30ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5445[2]	12	1	± 2	30ns	Parallel	RU-20, CP-20	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5447[2]	12	2	± 2	30ns	Parallel	RU-24	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5449[2]	12	2	± 2	30ns	Serial	RU-16	10 MHz BW, 10 ns $\overline{CS}$ Pulse Width
AD5452[2]	12	1	±0.5	40ns	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz Serial
AD5453[2]	14	1	±2	40ns	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz Serial

[1]Future parts, contact factory for availability
[2]In development, contact factory for availability

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10 Lead MSOP (RM-10)