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Dual, Current-Output Serial-Input, 16-/14-Bit DAC AD5545/AD5555

Preliminary Technical Data

FEATURES

16-bit Resolution AD5545 14-bit Resolution AD5555 ±2 LSB INL AD5545 ±1, ±1.5 LSB DNL AD5545 2mA Full Scale Current ± 20%, with V_{RFF}=10V

0.5µs Settling Time 2Q Multiplying Reference-input 4Hz BW 3-Wire Interface Compact TSSOP-16 Package

APPLICATIONS Automatic Test Equipment Instrumentation Digitally Controlled Calibration Industrial Control PLCs

GENERAL DESCRIPTION

The AD5545, 16-bit, current-output, digital-to-analog converter is designed to operate from a single +5 volt supply.

The applied external reference input voltage VREF determines the full-scale output-current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I to V precision amplifier.

A serial-data interface offers high-speed, three-wire micro controller compatible inputs using serial-data-in (SDI), clock (CLK), and $\overline{(CS)}$. Additional LDAC function allows simultaneous update operation.

The AD5545/AD5555 are packaged in the low profile compact TSSOP-16 package.

FUNCTIONAL DIAGRAMS



ORDERING GUIDE

	INL	DNL	RES	TEMP	Package	Package
MODEL	LSB	LSB	(bits)	RANGE	Description	Option
AD5545BRU	±2	±1	16	40 / +85°C	TSSOP-16	RU-16
AD5555CRU	±1	±1	14	40 / +85°C	TSSOP-16	RU-16

The AD5545 contains 3131 transistors.

The die size measures xx mil X xx mil, xxxx sqmil.

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AD5545/AD5555

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10% or V_{DD} = 3V±10%, V_{SS} = 0V, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full . مالد .

REFERENCE INPUT V_{REF} Range V_{REF} Input Resistance R_{REF} Input Capacitance ² C_{REF} ANALOG OUTPUTOutput CurrentOutput CurrentIourData = Full Scale2Output CurrentIourLogic Input Low Voltage V_{IL} Logic Input Capacitance ² C_{IL} Clock Input Frequency f_{CLK} Clock Nidth High t_{CH} Clock Kidth Low 10 Ross0Sto Clock Set Up t_{CSH} Clock to CS Hold t_{CSH} Data Setup t_{DH} Data Setup t_{DH} Digna Ange $V_{DD RANGE}$ Power Supply Range $V_{DD RANGE}$ Power Dissipation P_{DISS} Logic Inputs = 0V 0.055 Numax	Operating temperature Range, ur	less otherwise i			
ResolutionNAD5545, 1 LSB $= V_{REF} 2^{16} = 153\mu$ W when $V_{REF} = 10V$ 16BitsResolutionNAD5555, 1 LSB $= V_{REF} 2^{14} = 610\mu$ V when $V_{REF} = 10V$ 14BitsRelative AccuracyINLAD5555 Grade: C ± 2 LSB maxDifferential NonlinearityDNLMonotonic ± 1 LSB maxOutput Leakage Current J_{0T} Data = 0000 _h , $T_A = 7_A$ MAX20nA maxOutput Leakage Current J_{0T} Data = 0000 _h , $T_A = 7_A$ MAX20nA maxFull-Scale Gain Error G_{FSE} Data = Full Scale $\pm 1/\pm 4$ mV_{typmax} Full-Scale Tempco ² TCV _{FS} 1 $ppm^{\circ}C$ typ REFERENCE INPUT VREF-12/+12V min/maxInput Resistance R_{REF} 5k ohn typ ⁴ Input Capacitance ² C_{0TT} Code Dependent20Output CurrentIourData = Full Scale2mA typOutput CurrentIourData = Full Scale2mA typOutput CurrentIourData = Full Scale2mA typOutput CurrentIourData = Full Scale2MA typLogic Input Leakage CurrentI _{IL} 0.0pF typLOGIC INPUTS & OUTPUTLogic Input High VoltageV max2.4V minInput Leakage CurrentI _{IL} 10 μ max10 μ maxInput Leakage CurrentI _{IL} 10n s min10n s minCock Input High VoltageV _{IL} 0.5 <th></th> <th></th> <th>CONDITION</th> <th>5V±10%</th> <th>UNITS</th>			CONDITION	5V±10%	UNITS
ResolutionNAD5555, 1 LSB = $V_{REF} 2^{14} = 610 \mu V$ when $V_{REF} = 10V$ 14BitsRelative AccuracyINLAD5555 Grade: B ± 1 LSB maxDifferential NonlinearityDNLMonotonic ± 1 LSB maxOutput Leakage Current I_{OUT} Data = 0000 _H , T _A = 25°C10nA maxFull-Scale Gain ErrorG _{FSE} Data = 0000 _H , T _A = 7, MAX20nA maxFull-Scale Gain ErrorG _{FSE} Data = Full Scale $\pm 1/\pm 4$ mV typ/maxFull-Scale Gain ErrorG _{FSE} Data = Full Scale $\pm 1/\pm 4$ mV typ/maxFull-Scale Tempco ² TCV _{FS} 1ppm/°C typREFERENCE INPUTV $-12/\pm 12$ V min/maxInput ResistanceR _{REF} $-12/\pm 12$ V min/maxInput Capacitance ² C _{REF} 5k ohm typ ⁴ Output Capacitance ² C _{OUT} Code Dependent200Output Capacitance ² O _{GUT} Code Dependent200Logic Input High VoltageV _{IL} 0.8V maxLogic Input High VoltageV _{IL} 10 μ A maxInput Capacitance ² C _{IL} 10pF maxLogic Input High VoltageV _{IL} 10pF maxLogic Input High VoltageV _{IL} 10pF maxLogic Input Leakage CurrentI _L 10pF maxLogic Input High VoltageV _{IL} 10pF maxLogic Input High VoltageV _{LL} 10ns minInput Capacitance ² C _L 10 <td< td=""><td>STATIC PERFORMANCE¹</td><td></td><td></td><td></td><td></td></td<>	STATIC PERFORMANCE ¹				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Resolution				
$ \begin{array}{ccccc} \mbox{Relative Accuracy} & INL & AD5555 \mbox{Grade: C} & \pm 1 & LSB \mbox{max} \\ \mbox{Differential Nonlinearity} & DNL & Monotonic & \pm 1 & LSB \max \\ \mbox{Duput Leakage Current} & I_{OUT} & Data = 0000_{\rm H}, T_{\rm A} = 25^{\circ}{\rm C} & 10 & nA \mbox{max} \\ \mbox{Output Leakage Current} & I_{OUT} & Data = 0000_{\rm H}, T_{\rm A} = T_{\rm A} \mbox{MAX} & 20 & nA \mbox{max} \\ \mbox{Full-Scale Gain Error} & G_{FSE} & Data = Full Scale & \pm 1/24 & mV \mbox{typmax} \\ \mbox{Full-Scale Gain Error} & G_{FSE} & Data = Full Scale & \pm 1/24 & mV \mbox{typmax} \\ \mbox{Full-Scale Tempco}^2 & TCV_{FS} & 1 & ppm^{\circ/2} \mbox{typmax} \\ \mbox{Full-Scale Tempco}^2 & TCV_{FS} & -12/+12 & V \mbox{minmax} \\ \mbox{RefF Range} & V_{REF} & -12/+12 & V \mbox{minmax} \\ \mbox{Input Resistance} & R_{REF} & 5 & k \mbox{hmyp}^4 \\ \mbox{Input Capacitance}^2 & C_{RFF} & -5 & pf \mbox{typ} \\ \mbox{Output Current} & I_{OUT} & Data = Full Scale & 2 & mA \mbox{typ} \\ \mbox{Output Current} & I_{OUT} & Data = Full Scale & 2 & mA \mbox{typ} \\ \mbox{Output Capacitance}^2 & C_{GaT} & Code \mbox{Dependent} & 200 & pf \mbox{typ} \\ \mbox{Logic Input Low Voltage} & V_{IL} & 0.8 & V \mbox{max} \\ \mbox{Logic Input Low Voltage} & V_{IL} & 0.8 & V \mbox{max} \\ \mbox{Input Capacitance}^2 & C_{IL} & 10 & pF \mbox{max} \\ \mbox{Input Leakage Current} & I_{IL} & 10 & \muA \mbox{max} \\ \mbox{Input Leakage Current} & I_{IL} & 10 & pF \mbox{max} \\ \mbox{Input Leakage Current} & I_{IL} & 10 & ns \mbox{min} \\ \mbox{Clock Widh High} & \mbox{ty} \\ \mbox{Clock Set Up} & \mbox{tys} & 0 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & ns \mbox{min} \\ \mbox{Clock Set Up} & \mbox{tys} & 5 & $					
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	•				
Full-Scale Gain ErrorGrste Grste Data = Full Scale $\pm 1/\pm 4$ mV typ/maxFull-Scale Tempco ² TCV _{FS} 1 $ppm/^{O}C$ typ REFERENCE INPUT -12/+12V min/maxNameName5k ohm typ ⁴ Input ResistanceR _{REF} 5pF typ ANALOG OUTPUT 05pF typOutput Caracitance ² C _{OUT} Data = Full Scale2 ANALOG OUTPUT 0200pF typOutput Caracitance ² C _{OUT} Code Dependent200Logic Input S& OUTPUT0.8V maxLogic Input Low VoltageV _{IL} 0.8V maxLogic Input High VoltageV _{IL} 0.8V maxLogic Input High VoltageV _{IL} 10pF maxInput Capacitance ² C _{IL} 10pF maxLock Kidth Lowt _{CL} 10ns minClock Night Leakage CurrentI _{IL} 10ns minClock Kidth Lowt _{CL} 10ns minClock Kidth Lowt _{CL} 0ns minClock Set Upt _{CSS} 0ns minData Setupt _{DS} 5ns minData Setupt _{DS} 5ns minData Holdt _{DH} 10ns minSuper Supply RangeV _{DD RANGE} 0010Power DissipationP _{DISS} Logic Inputs = 0V0.055mW max					
Full-Scale Tempco ² TCV FS1ppm/°C typ ppm/°C typ REFERENCE INPUT V_{REF} Range V_{REF} $-12/+12$ V min/maxInput Resistance R_{REF} 5 k ohm typ ⁴ Input Capacitance ² C_{REF} 5 pF typ ANALOG OUTPUT Output Current I_{OUT} Data = Full Scale 2 $Output Capacitance2C_{OUT}Code Dependent200pF typLOGIC INPUTLogic Input Low VoltageV_{IL}0.8V maxLogic Input Low VoltageV_{IL}0.8V maxLogic Input High VoltageV_{IL}10\muA maxInput Capacitance2C_{IL}10\mu maxInput Capacitance2C_{IL}10\mu maxInput Capacitance2C_{IL}10\mu maxInput Capacitance2C_{IL}10\mu maxInput Capacitance2C_{IL}10\mu maxInput Capacitance2C_{IL}10n minClock Input Frequencyf_{CLK}10n minClock Ket Upt_{CBH}10n minClock Ket Upt_{CSH}0n minData Setupt_{DS}5n minData Holdt_{DH}10n minData Holdt_{DH}10n minSupply CurrentI_{DD}Logic Inputs = 0V10Power Dissipation<$					nA max
REFERENCE INPUTNote of the input the	Full-Scale Gain Error	G _{FSE}	Data = Full Scale	±1/±4	mV typ/max
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Full-Scale Tempco ²	TCV _{FS}		1	ppm/°C typ
$\begin{array}{c c c c c c c c c c c c c c c c c c c $					
Input Capacitance ² C_{REF} 5pF typANALOG OUTPUTIoUTData = Full Scale2mA typOutput CurrentIoUTData = Full Scale200pF typLOGIC INPUTS & OUTPUTUCode Dependent200pF typLogic Input Low VoltageV _{IL} 0.8V maxLogic Input High VoltageV _{IL} 0.8V maxInput Capacitance ² C _{IL} 10 μ A maxInput Capacitance ² C _{IL} 10pF maxInput Capacitance ² C _{IL} 10pF maxClock Input Frequencyf _{CLK} 40MHzClock Night Hight _{CH} 10ns minClock Set Upt _{CSS} 0ns minClock Vidth Lowt _{CS} 0ns minClock to CS Holdt _{CSH} 10ns minData Holdt _{DH} 10ns minSUPPLY CHARACTERISTICS10ns minPower Supply RangeV _{DD RANGE} 4.5/5.5V min/maxPower DissipationP _{DISS} Logic Inputs = 0V0.055mW max		V_{REF}			
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LOGIC INPUTS & OUTPUTLogic Input Low Voltage V_{IL} 0.8V maxLogic Input High Voltage V_{IH} 2.4V minInput Leakage Current I_{IL} 10 μA maxInput Capacitance ² C_{IL} 10pF maxINTERFACE TIMING ^{2,3} 10pF maxClock Input Frequency f_{CLK} 40MHz10ns minClock Width Low t_{CH} 10Clock Set Up t_{CSS} 0Clock Kot S Hold t_{CSH} 10Data Hold t_{DH} 10SUPPLY CHARACTERISTICS4.5/5.5V min/maxPower Supply Range $V_{DD RANGE}$ 4.5/5.5Power Dissipation P_{DISS} Logic Inputs = 0VPower Dissipation P_{DISS} Logic Inputs = 0VOutput I_{DD} Logic Inputs = 0V0.055M max	Output Current	I _{OUT}	Data = Full Scale	2	mA typ
$\begin{array}{cccccccc} \mbox{Logic Input Low Voltage} & V_{IL} & & & & & & & & & & & & & & & & & & &$			Code Dependent	200	pF typ
$\begin{array}{cccccccccccccccccccccccccccccccccccc$					
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		V _{IL}		0.8	V max
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Logic Input High Voltage	V_{IH}		2.4	V min
INTERFACE TIMING 2.340Clock Input Frequency f_{CLK} Clock Width High t_{CH} Clock Width Low t_{CL} Clock Width Low t_{CL} Clock Width Low t_{CL} Clock Set Up t_{CSS} Clock Ket Up t_{CSH} Clock to CS Hold t_{CSH} Data Setup t_{DS} Data Hold t_{DH} SUPPLY CHARACTERISTICSPower Supply Range $V_{DD RANGE}$ Power Dissipation P_{DISS} Logic Inputs = 0V 0.055 mW max	Input Leakage Current	I _{IL}		10	μA max
$\begin{array}{c c c c c c c } Clock Input Frequency & f_{CLK} & & & & & & & & & & & & & & & & & & &$		C _{IL}		10	pF max
$\begin{array}{c c c c c c c } Clock Width High & t_{CH} & 10 & ns min \\ \hline Clock Width Low & t_{CL} & 10 & ns min \\ Clock Width Low & t_{CL} & 0 & ns min \\ CS to Clock Set Up & t_{CSS} & 0 & ns min \\ Clock to CS Hold & t_{CSH} & 10 & ns min \\ Data Setup & t_{DS} & 5 & ns min \\ \hline Data Hold & t_{DH} & 10 & ns min \\ \hline \textbf{SUPPLY CHARACTERISTICS} & 4.5/5.5 & V min/max \\ Power Supply Range & V_{DD RANGE} & 4.5/5.5 & V min/max \\ Power Dissipation & P_{DISS} & Logic Inputs = 0V & 0.055 & mW max \\ \hline \end{array}$	INTERFACE TIMING ^{2,3}				
$\begin{array}{c c c c c c c c } Clock Width Low & t_{CL} & 10 & ns min \\ CS to Clock Set Up & t_{CSS} & 0 & ns min \\ Clock to CS Hold & t_{CSH} & 10 & ns min \\ Data Setup & t_{DS} & 5 & ns min \\ Data Hold & t_{DH} & 10 & ns min \\ \hline {\mbox{SUPPLY CHARACTERISTICS}} & 4.5/5.5 & V min/max \\ Power Supply Range & V_{DD RANGE} & 4.5/5.5 & V min/max \\ Power Dissipation & P_{DISS} & Logic Inputs = 0V & 0.055 & mW max \\ \hline {\mbox{Min}} & {\mbo$		f _{CLK}		-	MHz
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	-	t _{CH}		10	ns min
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Clock Width Low	t _{CL}		10	ns min
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	CS to Clock Set Up	t _{CSS}		0	ns min
Data Hold t_{DH} 10ns minSUPPLY CHARACTERISTICSPower Supply Range $V_{DD RANGE}$ 4.5/5.5V min/maxPositive Supply Current I_{DD} Logic Inputs = 0V10 $\mu A \max$ Power Dissipation P_{DISS} Logic Inputs = 0V0.055mW max	Clock to CS Hold	t _{CSH}			
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Power Supply Range $V_{DD RANGE}$ 4.5/5.5V min/maxPositive Supply Current I_{DD} Logic Inputs = 0V10 μA maxPower Dissipation P_{DISS} Logic Inputs = 0V0.055mW max	Data Hold	t _{DH}		10	ns min
Positive Supply Current I_{DD} Logic Inputs = 0V10 $\mu A \max$ Power Dissipation P_{DISS} Logic Inputs = 0V0.055mW max	SUPPLY CHARACTERIST	TICS			
Power Dissipation P_{DISS} Logic Inputs = 0V0.055mW max					V min/max
		I _{DD}		10	μA max
Power Supply Sensitivity PSS $\Delta V_{DD} = \pm 5\%$ 0.006 %/% max	Power Dissipation	P _{DISS}	Logic Inputs $= 0V$	0.055	mW max
	Power Supply Sensitivity	PSS	$\Delta V_{DD} = \pm 5\%$	0.006	%/% max

NOTES:

All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP1177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C These parameters are guaranteed by design and not subject to production testing. All input control signals are specified with $t_R = t_F = 2.5$ ns (10% to 90% of +3V) and timed from a voltage level of 1.5V. 1.

2.

3.

All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier. 4.

AD5545/AD5555

ELECTRICAL CHARACTERISTICS at $V_{DD} = 5V \pm 10\%$, $I_{OUT} = Virtual GND$, GND=0V, $V_{REF} = 10V$,

 T_A = Full Operating Temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
AC CHARACTERISTICS				
Output Voltage Settling Time	ts	To $\pm 0.1\%$ of Full Scale, Data = Zero Scale to Full Scale		
		to Zero Scale	0.5	µs typ
Reference Multiplying BW	BW	$V_{REF} = 5V_{P-P}$, Data = Full Scale	4	MHz typ
DAC Glitch Impulse	Q	$V_{REF} = 0V$, Data Zero Scale to Mid Scale to Zero Scale	7	nV-s typ
Feed Through Error	V_{OUT}/V_{REF}	Data = Zero Scale, V_{REF} = 100mVrms, same channel	-65	dB
Digital Feed Through	Q	$CS = 1$, and $f_{CLK} = 1MHz$	7	nV-s typ
Total Harmonic Distortion	THD	$V_{REF} = 5V_{P-P}$, Data = Full Scale, f=1KHz	-73	dB typ
Output Spot Noise Voltage	e _N	f = 1 kHz, BW = 1Hz	4	nV/ rt Hz

NOTES:

 All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C

2. These parameters are guaranteed by design and not subject to production testing.

3. All input control signals are specified with $t_{\rm R} = t_{\rm F} = 2.5$ ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.

4. All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier.

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND0.3V, +8V
V _{REF} to GND18V, 18V
Logic Inputs to GND0.3V, +8V
V(I _{OUT}) to GND–0.3V, V _{DD} + 0.3V
Input Current to Any Pin except Supplies ±50mA
Package Power Dissipation $(T_J MAX - T_A)/THETA_{JA}$
Thermal Resistance THETA _{JA}
16-lead TSSOP 150°C/W
Maximum Junction Temperature (T _J MAX)150°C
Operating Temperature Range
Models A, B, C40°C to $+85^{\circ}$ C
Storage Temperature Range65°C to +150°C
Lead Temperature:
RU-16 (Vapor Phase, 60 secs)+215°C
RU-16 (Infrared, 15 secs)+220°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



AD5545/AD5555





Figure 2. AD5555 Timing Diagram

Tabl	le 1. AI	05545 C	Contro	ol-Logic T	Fruth Table		
CS	CLK	LDAC	RS	MSB	Serial Shift Register Function	Input Register Function	DAC Register
Н	Х	Н	Н	Х	No Effect	Latched	Latched
L	L	Н	Η	Х	No Effect	Latched	Latched
L	\uparrow_+	Н	Н	Х	Shift-Register-Data advanced one bit	Latched	Latched
L	Η	Н	Н	Х	No Effect	Latched	Latched
\uparrow_+	L	Н	Н	Х	No Effect	Selected DAC Updated	Latched
						with current SR contents	
Η	Х	L	Η	Х	No Effect	Latched	Transparent
Η	Х	Н	Η	Х	No Effect	Latched	Latched
Н	Х	\uparrow_+	Н	Х	No Effect	Latched	Latched
Н	Х	Н	L	0	No Effect	Latched Data = $0000_{\rm H}$	Latched Data = $0000_{\rm H}$
Н	Х	Н	L	Н	No Effect	Latched Data = $8000_{\rm H}$	Latched Data = $8000_{\rm H}$

Table 2. AD5555 Control-Logic Truth Table

CS	CLK	LDAC	RS	MSB	Serial Shift Register Function	Input Register Function	DAC Register
Н	Х	Н	Н	Х	No Effect	Latched	Latched
L	L	Н	Н	Х	No Effect	Latched	Latched
L	\uparrow_+	Н	Н	Х	Shift-Register-Data advanced one bit	Latched	Latched
L	Н	Н	Н	Х	No Effect	Latched	Latched
\uparrow_+	L	Н	Н	Х	No Effect	Selected DAC Updated	Latched
						with current SR contents	
Η	Х	L	Η	Х	No Effect	Latched	Transparent
Η	Х	Н	Η	Х	No Effect	Latched	Latched
Н	Х	\uparrow_+	Н	Х	No Effect	Latched	Latched
Н	Х	Н	L	0	No Effect	Latched Data = $0000_{\rm H}$	Latched Data = $0000_{\rm H}$
Η	Х	Н	L	Н	No Effect	Latched Data = $2000_{\rm H}$	Latched Data = $2000_{\rm H}$

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- 1. SR = Shift Register
- 2. 1+ positive logic transition; X Don't Care
- 3. At power ON both the Input Register and the DAC Register are loaded with all zeros.

Table 3. AD5545 Serial Input Register Data Format, Data is loaded in the MSB-First Format.

	MSE	3																LSB
Bit Position	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: Only the last 18 bits of data clocked into the serial register (Address + Data) are inspected when the CS line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5545 shift register are ignored, only the last 18 bits clocked in are used. If double buffered data is not needed, the LDAC pin can be tied logic low to disable the DAC Registers.

Table 4. AD5555 Serial Input Register Data Format, Data is loaded in the MSB-First Format.

	MSE	3														LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: Only the last 16 bits of data clocked into the serial register (Address + Data) are inspected when the CS line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D13-D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5555 shift register are ignored, only the last 16 bits clocked in are used. If double buffered data is not needed, the LDAC pin can be tied logic low to disable the DAC Registers.

Table 5. Address Decode:

<u>A1</u>	<u>A0</u>	DAC Decoded
0	0	NONE
0	1	DAC A
1	0	DAC B
1	1	DAC A and B

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AD5545/AD5555 Ad5544/Ad5554 PIN DESCRIPTION

<u>PIN#</u> 1	<u>Name</u> R _{FB} A	<u>Function</u> Establish voltage output for DAC A by connecting to external amplifier output
2	V _{REF} A	DAC A Reference voltage input terminal. Establishes DAC A Full-Scale output voltage. Pin can be tied to V_{DD} pin.
3	I _{OUT} A	DAC A current output.
4	A _{GND} A	DAC A analog ground.
5	A _{GND} B	DAC B analog ground.
6	I _{OUT} B	DAC B current output.
7	V _{REF} B	DAC B Reference voltage input terminal.
		Establishes DAC B Full-Scale output voltage.
		Pin can be tied to V _{DD} pin.
8	R _{FB} B	Establish voltage output for DAC B by
		connecting to external amplifier output.
9	SDI	Serial Data Input, input data loads directly into
		the shift register.
10	RS	Reset pin, active low input. Input registers and
		DAC registers are set to all zeros or half-scale
		code ($8000_{\rm H}$ for AD5545) and ($2000_{\rm H}$ for
		AD5555) determined by the voltage on the

CIRCUIT OPERATION

The AD5545/AD5555 contains a 16-/14-bit, current-output, digital-to-analog converter, a serial input register, and a DAC register. Both parts use a 3-wire serial data interface.

D/A Converter Section

The DAC architecture uses a current-steering R-2R ladder design. Figure 3 shows the typical equivalent DAC. The DAC contains a matching feedback resistor for use with an external I to V converter amplifier. The R_{FB} pin is connected to the output of the external amplifier. The I_{OUT} terminal is connected to the inverting input of the external amplifier. These DACs are designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal 5 k Ω feedback resistor. If users are attempting to measure the value of R_{FB} , power must be applied to V_{DD} in order to achieve continuity. The V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register according to equation [1 &2] determines the DAC output voltage:

$V_{OUT} = -V_{REF} * D / 65,536$	Equation 1
$V_{OUT} = -V_{REF} * D / 16,384$	Equation 2

Note that the output full-scale polarity is opposite to the V_{REF} polarity for DC reference voltages.

MSB pin. Register Data = 0000_{H} when MSB = 0. Register Data = 8000_{H} for AD5545 and 2000_{H} for AD5555 when MSB = 1.

- CSChip Select, active low input. Disables shift
register loading when high. Transfers Serial
Register Data to the Input Register when
CS/LDAC returns High. Does not effect LDAC
operation.DGNDDigital Ground Pin.
- V_{DD} Positive power supply input. Specified range
- 14 MSB of operation $+5V\pm10\%$ or $+3V\pm10\%$ MSB bit set pin during a reset pulse (RS) or at system power ON if tied to ground or V_{DD}.
- 15 Load DAC Register strobe, level sensitive active low. Transfers all Input Register data to DAC registers. Asynchronous active low input. See Control Logic Truth Table for operation.
 16 CLK Clock input, positive edge clocks data into

16 CLK shift register.



DIGITAL INTERFACE CONNECTIONS OMITTED FOR CLARITY SWITCHES S1 & S2 ARE CLOSED, V_{DD} MUST BE POWERED

Figure 3. Equivalent R-2R DAC Circuit

These DACs are also designed to accommodate AC reference input signals. The AD5545 will accommodate input reference voltages in the range of -12 to +12 volts. The reference voltage inputs exhibit a constant nominal input-resistance value of 5K ohms, $\pm 30\%$. The DAC output (I_{OUT}) is code-dependent producing various output resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5545 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. In order to maintain good analog performance, power supply bypassing of 0.01uF in parallel with 1uF is recommended. Under these conditions clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used. It is best to derive the AD5545's +5V supply from the systems analog supply voltages. (Don't use the digital 5V supply). See figure 4.

AD5545/AD5555



Figure 4. Recommended System Connections

SERIAL DATA INTERFACE

The AD5545 uses a 3-wire (CS, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 18bit data-word format. The MSB bit is loaded first. Table 2 defines the 18 data-word bits. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the INTERFACE TIMING SPECIFICATIONS. Only the last 18-bits clocked into the serial register will be interrogated when the CS pin is strobed to transfer the serial register data to the DAC register. Since most micro controllers' output serial data in 8-bit bytes, three right justified data bytes can be written to the AD5545. After loading the serial register the rising edge of CS transfers the serial register data to the DAC register, during this strobe the CLK should not be toggled.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in figure 7.

16-Lead TSSOP



Dimensions shown in inches and (mm).





Figure 7. Equivalent ESD Protection Circuits