a

Dual, Current-Output Serial-Input, 16-/14-Bit DAC

Preliminary Technical Data — AD5545/AD5555

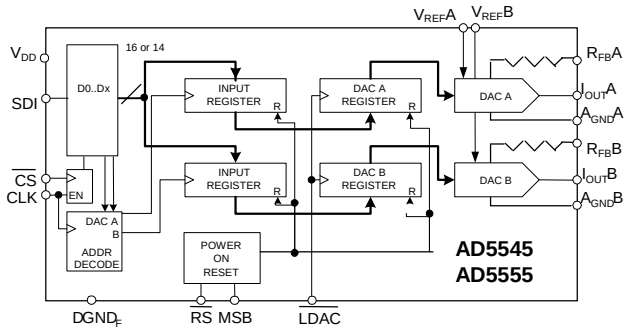
FEATURES

16-bit Resolution AD5545
14-bit Resolution AD5555
±2 LSB INL AD5545
±1, ±1.5 LSB DNL AD5545
2mA Full Scale Current ± 20%, with V_{REF}=10V
0.5µs Settling Time
2Q Multiplying Reference-input 4Hz BW
3-Wire Interface
Compact TSSOP-16 Package

APPLICATIONS

Automatic Test Equipment
Instrumentation
Digitally Controlled Calibration
Industrial Control PLCs

FUNCTIONAL DIAGRAMS



GENERAL DESCRIPTION

The AD5545, 16-bit, current-output, digital-to-analog converter is designed to operate from a single +5 volt supply.

The applied external reference input voltage VREF determines the full-scale output-current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I to V precision amplifier.

A serial-data interface offers high-speed, three-wire micro controller compatible inputs using serial-data-in (SDI), clock (CLK), and ($\overline{CS}$). Additional LDAC function allows simultaneous update operation.

The AD5545/AD5555 are packaged in the low profile compact TSSOP-16 package.

ORDERING GUIDE

	INL	DNL	RES	TEMP	Package	Package
MODEL	LSB	LSB	(bits)	RANGE	Description	Option
AD5545BRU	±2	±1	16	40 / +85°C	TSSOP-16	RU-16
AD5555CRU	±1	±1	14	40 / +85°C	TSSOP-16	RU-16

The AD5545 contains 3131 transistors.
The die size measures xx mil X xx mil, xxxx sqmil.

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AD5545/AD5555

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10% or V_{DD} = 3V±10%, V_{SS} = 0V, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
STATIC PERFORMANCE[1]				
Resolution	N	AD5545, 1 LSB = $V_{REF}/2^{16}$ = 153µV when V_{REF} = 10V	16	Bits
Resolution	N	AD5555, 1 LSB = $V_{REF}/2^{14}$ = 610µV when V_{REF} = 10V	14	Bits
Relative Accuracy	INL	AD5545 Grade: B	±2	LSB max
Relative Accuracy	INL	AD5555 Grade: C	±1	LSB max
Differential Nonlinearity	DNL	Monotonic	±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = 25°C	10	nA max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = T_A MAX	20	nA max
Full-Scale Gain Error	G_{FSE}	Data = Full Scale	±1/±4	mV typ/max
Full-Scale Tempco[2]	TCV_{FS}		1	ppm/°C typ
REFERENCE INPUT				
V_{REF} Range	V_{REF}		-12/+12	V min/max
Input Resistance	R_{REF}		5	k ohm typ[4]
Input Capacitance[2]	C_{REF}		5	pF typ
ANALOG OUTPUT				
Output Current	I_{OUT}	Data = Full Scale	2	mA typ
Output Capacitance[2]	C_{OUT}	Code Dependent	200	pF typ
LOGIC INPUTS & OUTPUT				
Logic Input Low Voltage	V_{IL}		0.8	V max
Logic Input High Voltage	V_{IH}		2.4	V min
Input Leakage Current	I_{IL}		10	µA max
Input Capacitance[2]	C_{IL}		10	pF max
INTERFACE TIMING [2, 3]				
Clock Input Frequency	f_{CLK}		40	MHz
Clock Width High	t_{CH}		10	ns min
Clock Width Low	t_{CL}		10	ns min
CS to Clock Set Up	t_{CSS}		0	ns min
Clock to CS Hold	t_{CSH}		10	ns min
Data Setup	t_{DS}		5	ns min
Data Hold	t_{DH}		10	ns min
SUPPLY CHARACTERISTICS				
Power Supply Range	$V_{DD\ RANGE}$		4.5/5.5	V min/max
Positive Supply Current	I_{DD}	Logic Inputs = 0V	10	µA max
Power Dissipation	P_{DISS}	Logic Inputs = 0V	0.055	mW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	%/% max

NOTES:

1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP1177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C
2. These parameters are guaranteed by design and not subject to production testing.
3. All input control signals are specified with $t_R = t_F$ = 2.5ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
4. All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier.

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10%, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating Temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
AC CHARACTERISTICS				
Output Voltage Settling Time	t_S	To ±0.1% of Full Scale, Data = Zero Scale to Full Scale to Zero Scale	0.5	µs typ
Reference Multiplying BW	BW	V_{REF} = $5V_{P-P}$, Data = Full Scale	4	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0V, Data Zero Scale to Mid Scale to Zero Scale	7	nV-s typ
Feed Through Error	V_{OUT}/V_{REF}	Data = Zero Scale, V_{REF} = 100mVrms, same channel	-65	dB
Digital Feed Through	Q	CS = 1, and f_{CLK} = 1MHz	7	nV-s typ
Total Harmonic Distortion	THD	V_{REF} = $5V_{P-P}$, Data = Full Scale, f=1KHz	–73	dB typ
Output Spot Noise Voltage	e_N	f = 1kHz, BW = 1Hz	4	nV/ rt Hz

NOTES:

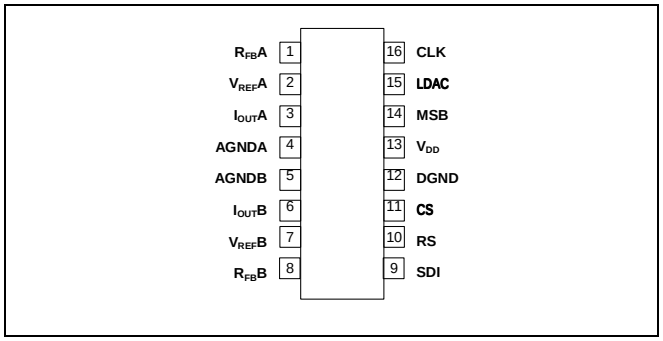
1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5545 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C
2. These parameters are guaranteed by design and not subject to production testing.
3. All input control signals are specified with t_R = t_F = 2.5ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
4. All AC Characteristic tests are performed in a closed loop system using an OP42 I-to-V converter amplifier.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... –0.3V, +8V
V_{REF} to GND .....–18V, 18V
Logic Inputs to GND..... –0.3V, +8V
$V(I_{OUT})$ to GND .....–0.3V, V_{DD} + 0.3V
Input Current to Any Pin except Supplies..... ±50mA
Package Power Dissipation ..... $(T_{J\ MAX} – T_A)/ THETA_{JA}$
Thermal Resistance $THETA_{JA}$
16-lead TSSOP..... 150°C/W
Maximum Junction Temperature ($T_{J\ MAX}$) ..... 150°C
Operating Temperature Range
Models A, B, C .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature:
RU-16 (Vapor Phase, 60 secs) ..... +215°C
RU-16 (Infrared, 15 secs)..... +220°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



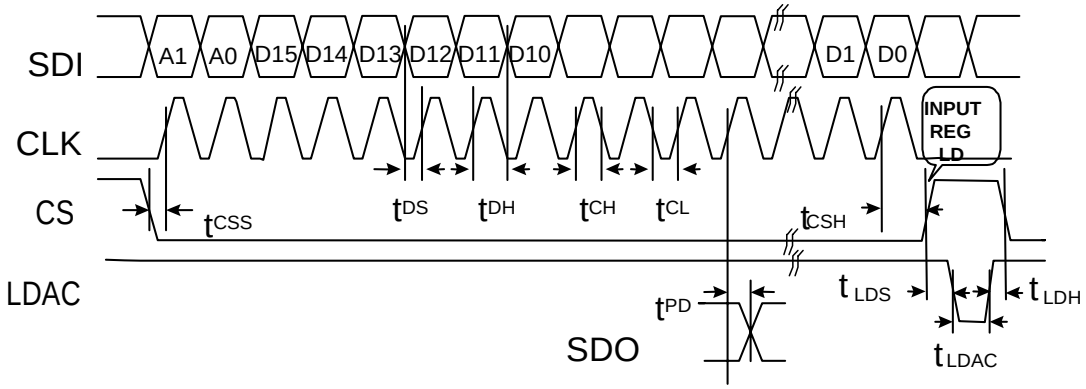


Figure 1. AD5545 Timing Diagram

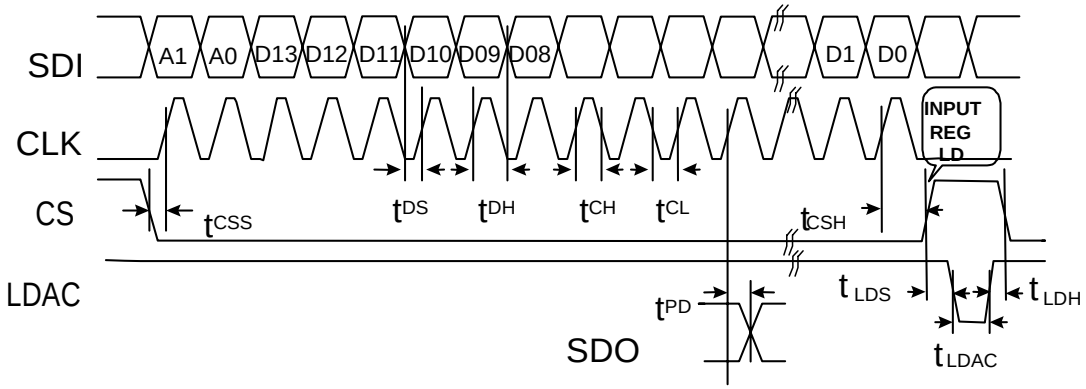


Figure 2. AD5555 Timing Diagram

Table 1. AD5545 Control-Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift-Register-Data advanced one bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with current SR contents	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0000_H	Latched Data = 0000_H
H	X	H	L	H	No Effect	Latched Data = 8000_H	Latched Data = 8000_H

Table 2. AD5555 Control-Logic Truth Table

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	Serial Shift Register Function	Input Register Function	DAC Register
H	X	H	H	X	No Effect	Latched	Latched
L	L	H	H	X	No Effect	Latched	Latched
L	↑+	H	H	X	Shift-Register-Data advanced one bit	Latched	Latched
L	H	H	H	X	No Effect	Latched	Latched
↑+	L	H	H	X	No Effect	Selected DAC Updated with current SR contents	Latched
H	X	L	H	X	No Effect	Latched	Transparent
H	X	H	H	X	No Effect	Latched	Latched
H	X	↑+	H	X	No Effect	Latched	Latched
H	X	H	L	0	No Effect	Latched Data = 0000_H	Latched Data = 0000_H
H	X	H	L	H	No Effect	Latched Data = 2000_H	Latched Data = 2000_H

Notes:

1. SR = Shift Register
2. ↑+ positive logic transition; X Don't Care
3. At power ON both the Input Register and the DAC Register are loaded with all zeros.

Table 3. AD5545 Serial Input Register Data Format, Data is loaded in the MSB-First Format.

	MSB																LSB
Bit Position	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: Only the last 18 bits of data clocked into the serial register (Address + Data) are inspected when the CS line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5545 shift register are ignored, only the last 18 bits clocked in are used. If double buffered data is not needed, the $\overline{\text{LDAC}}$ pin can be tied logic low to disable the DAC Registers.

Table 4. AD5555 Serial Input Register Data Format, Data is loaded in the MSB-First Format.

	MSB															LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: Only the last 16 bits of data clocked into the serial register (Address + Data) are inspected when the CS line's positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D13-D0) to the decoded DAC-Input-Register address determined by bits A1 and A0. Any extra bits clocked into the AD5555 shift register are ignored, only the last 16 bits clocked in are used. If double buffered data is not needed, the $\overline{\text{LDAC}}$ pin can be tied logic low to disable the DAC Registers.

Table 5. Address Decode:

A1	A0	DAC Decoded
0	0	NONE
0	1	DAC A
1	0	DAC B
1	1	DAC A and B

AD5544/AD5554 PIN DESCRIPTION

PIN#	Name	Function
1	$R_{FB}A$	Establish voltage output for DAC A by connecting to external amplifier output
2	$V_{REF}A$	DAC A Reference voltage input terminal. Establishes DAC A Full-Scale output voltage. Pin can be tied to V_{DD} pin.
3	$I_{OUT}A$	DAC A current output.
4	$A_{GND}A$	DAC A analog ground.
5	$A_{GND}B$	DAC B analog ground.
6	$I_{OUT}B$	DAC B current output.
7	$V_{REF}B$	DAC B Reference voltage input terminal. Establishes DAC B Full-Scale output voltage. Pin can be tied to V_{DD} pin.
8	$R_{FB}B$	Establish voltage output for DAC B by connecting to external amplifier output.
9	SDI	Serial Data Input, input data loads directly into the shift register.
10	$\overline{RS}$	Reset pin, active low input. Input registers and DAC registers are set to all zeros or half-scale code (8000_H for AD5545) and (2000_H for AD5555) determined by the voltage on the MSB pin. Register Data = 0000_H when MSB = 0. Register Data = 8000_H for AD5545 and 2000_H for AD5555 when MSB = 1.
11	$\overline{CS}$	Chip Select, active low input. Disables shift register loading when high. Transfers Serial Register Data to the Input Register when CS/LDAC returns High. Does not effect LDAC operation.
12	DGND	Digital Ground Pin.
13	V_{DD}	Positive power supply input. Specified range of operation +5V±10% or +3V±10%
14	MSB	MSB bit set pin during a reset pulse (RS) or at system power ON if tied to ground or V_{DD}.
15	$\overline{LDAC}$	Load DAC Register strobe, level sensitive active low. Transfers all Input Register data to DAC registers. Asynchronous active low input. See Control Logic Truth Table for operation.
16	CLK	Clock input, positive edge clocks data into shift register.

CIRCUIT OPERATION

The AD5545/AD5555 contains a 16-/14-bit, current-output, digital-to-analog converter, a serial input register, and a DAC register. Both parts use a 3-wire serial data interface.

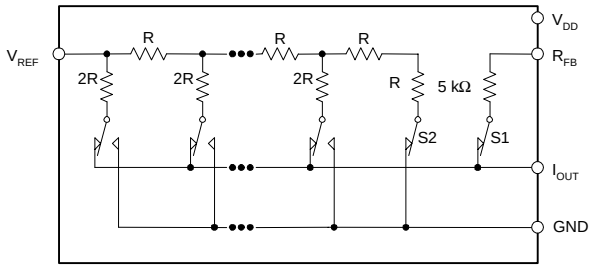
D/A Converter Section

The DAC architecture uses a current-steering R-2R ladder design. Figure 3 shows the typical equivalent DAC. The DAC contains a matching feedback resistor for use with an external I to V converter amplifier. The R_{FB} pin is connected to the output of the external amplifier. The I_{OUT} terminal is connected to the inverting input of the external amplifier. These DACs are designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches ON and OFF. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users are attempting to measure the value of R_{FB}, power must be applied to V_{DD} in order to achieve continuity. The V_{REF} input voltage and the digital data (D) loaded into the corresponding DAC register according to equation [1 &2] determines the DAC output voltage:

$$V_{OUT} = -V_{REF} * D / 65{,}536 \qquad \text{Equation 1}$$

$$V_{OUT} = -V_{REF} * D / 16{,}384 \qquad \text{Equation 2}$$

Note that the output full-scale polarity is opposite to the V_{REF} polarity for DC reference voltages.



DIGITAL INTERFACE CONNECTIONS OMITTED FOR CLARITY
SWITCHES S1 & S2 ARE CLOSED, V_{DD} MUST BE POWERED

Figure 3. Equivalent R-2R DAC Circuit

These DACs are also designed to accommodate AC reference input signals. The AD5545 will accommodate input reference voltages in the range of -12 to +12 volts. The reference voltage inputs exhibit a constant nominal input-resistance value of 5K ohms, ±30%. The DAC output (I_{OUT}) is code-dependent producing various output resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5545 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. In order to maintain good analog performance, power supply bypassing of 0.01uF in parallel with 1uF is recommended. Under these conditions clean power supply voltages (low ripple, avoid switching supplies) appropriate for the application should be used. It is best to derive the AD5545's +5V supply from the systems analog supply voltages. (Don't use the digital 5V supply). See figure 4.

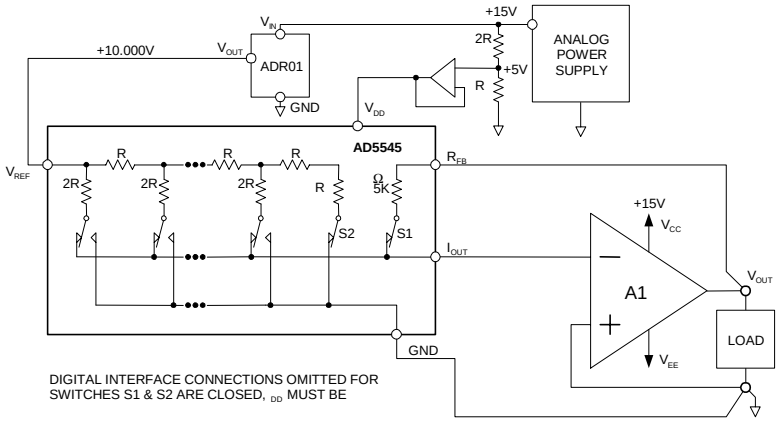


Figure 4. Recommended System Connections

SERIAL DATA INTERFACE

The AD5545 uses a 3-wire (CS, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 18-bit data-word format. The MSB bit is loaded first. Table 2 defines the 18 data-word bits. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the INTERFACE TIMING SPECIFICATIONS. Only the last 18-bits clocked into the serial register will be interrogated when the CS pin is strobed to transfer the serial register data to the DAC register. Since most micro controllers' output serial data in 8-bit bytes, three right justified data bytes can be written to the AD5545. After loading the serial register the rising edge of CS transfers the serial register data to the DAC register, during this strobe the CLK should not be toggled.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in figure 7.

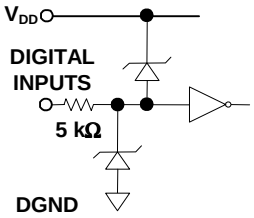


Figure 7. Equivalent ESD Protection Circuits

Mechanical Outline Dimensions

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)