Current-Output Parallel-Input, 16-/14-Bit DAC

Preliminary Technical Data — AD5546/AD5556

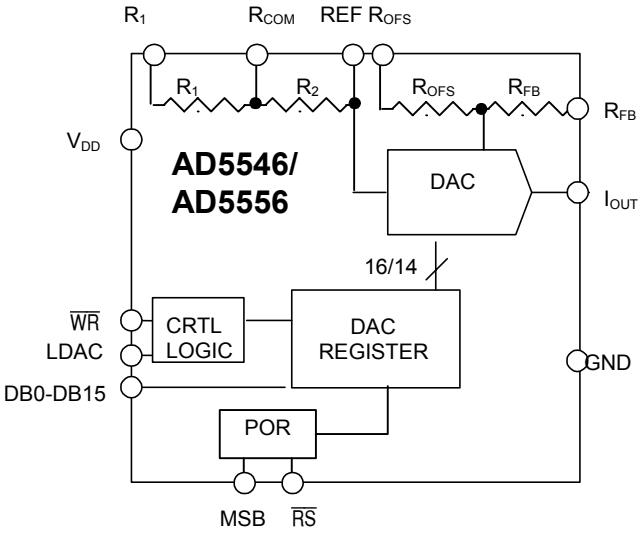
FEATURES

16-bit Resolution AD5546
14-bit Resolution AD5556
±1 LSB DNL
±1 or ±2 LSB INL
Low Noise 12nV/√Hz
Low Power, I_{DD}=10μA
0.5μs Settling Time
Built-in R_{FB} Facilitates Voltage Conversion
Built-in 4-Quadrant Resistors Allow 0 to 10V, 0 to –10V, or +/-10V Outputs
2mA Full Scale Current ± 20%, with V_{REF}=10V
Compact TSSOP-28 Packages

APPLICATIONS

Automatic Test Equipment
Instrumentation
Digitally Controlled Calibration
Digital Waveform Generation

FUNCTIONAL DIAGRAMS



GENERAL DESCRIPTION

The AD5546/AD5556 are precision 16/14-bit, low power, current-output, parallel input digital-to-analog converters. They are designed to operate from single +5V supply with ±10V multiplying reference for 4-Quadrant outputs.

The built-in 4-Quadrant resistors facilitate the resistance matching and temperature tracking that minimize the numbers of components needed for Multi-Quadrant applications. In addition, the feedback resistor (R_{FB}) also simplifies the I-V conversion with an external buffer.

The AD5546/AD5556 are packaged in compact TSSOP-28 package and the operating temperature ranges from –40°C to +85°C.

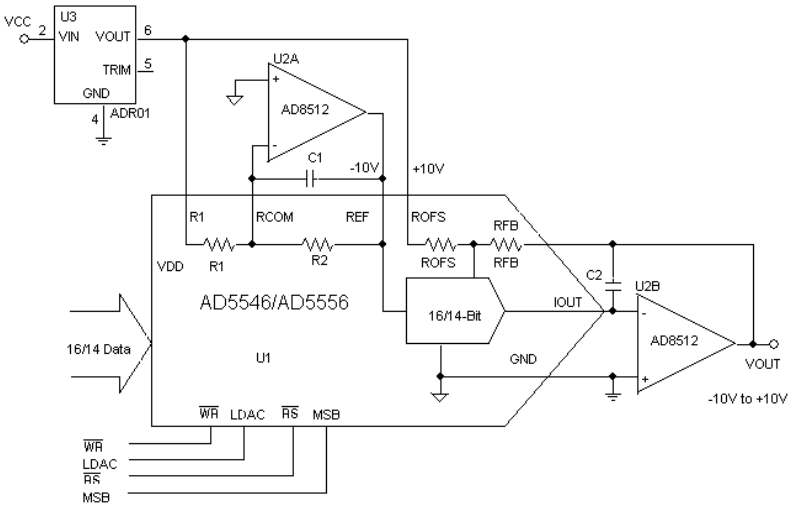


Figure 1. 16/14-Bit 4-Quadrant Multiplying DAC with Minimum of External Components

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ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10%, V_{SS} = 0V, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION		5V±10%	UNITS
STATIC PERFORMANCE[1]					
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153µV when V_{REF} = 10V	AD5546	16	Bits
Resolution	N	1 LSB = $V_{REF}/2^{14}$ = 610µV when V_{REF} = 10V	AD5556	14	Bits
Relative Accuracy	INL	Grade: AD5556C		±1	LSB max
Relative Accuracy	INL	Grade: AD5546B		±2	LSB max
Differential Nonlinearity	DNL	Monotonic		±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = 25°C		10	nA max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = T_A MAX		20	nA max
Full-Scale Gain Error	G_{FSE}	Data = $FFFF_H$		±1/±4	mV typ/max
Full-Scale Tempco[2]	TCV_{FS}			1	ppm/°C typ
REFERENCE INPUT					
V_{REF} Range	V_{REF}			-12/+12	V min/max
REF Input Resistance	REF			5	k ohm typ[4]
R1, R2 Resistance	R_1, R_2			10	k ohm typ[4]
Feedback and Offset Resistance	R_{FB}, R_{OFS}			10	k ohm typ[4]
Input Capacitance[2]	C_{REF}			5	pF typ
ANALOG OUTPUT					
Output Current	I_{OUT}	Data = $FFFF_H$		2	mA typ
Output Capacitance[2]	C_{OUT}	Code Dependent		200	pF typ
LOGIC INPUTS & OUTPUT					
Logic Input Low Voltage	V_{IL}			0.8	V max
Logic Input High Voltage	V_{IH}			2.4	V min
Input Leakage Current	I_{IL}			10	µA max
Input Capacitance[2]	C_{IL}			10	pF max
INTERFACE TIMING [2, 3]					
Data to $\overline{C}$ Setup Time	t_{DS}			25	ns min
Data to $\overline{WR}$ Hold Time	t_{DH}			0	ns min
$\overline{WR}$ Pulse Width	t_{WR}			25	ns min
LDAC Pulse Width	t_{LDAC}			25	ns min
Reset Pulse Width	t_{RS}			25	ns min
$\overline{WR}$ to LDAC Delay Time	t_{LWD}			0	ns min
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$			4.5/5.5	V min/max
Positive Supply Current	I_{DD}	Logic Inputs = 0V		10	µA max
Power Dissipation	P_{DISS}	Logic Inputs = 0V		0.055	mW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.006	%/% max

NOTES:

1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5546 R_{FB} terminal is tied to the amplifier output. The opamp +IN is grounded and the DAC I_{OUT} is tied to the opamp –IN. Typical values represent average readings measured at 25°C
2. These parameters are guaranteed by design and not subject to production testing.
3. All input control signals are specified with t_R = t_F = 2.5ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
4. All AC Characteristic tests are performed in a closed loop system using an AD841 I-to-V converter amplifier.

ELECTRICAL CHARACTERISTICS at V_{DD} = 5V±10%, I_{OUT} = Virtual GND, GND=0V, V_{REF} = 10V, T_A = Full Operating Temperature Range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	5V±10%	UNITS
AC CHARACTERISTICS[4]				
Output Voltage Settling Time	t_S	To ±0.1% of Full Scale, Data = 0000_H to $FFFF_H$ to 0000_H	0.5	µs typ
Reference Multiplying BW	BW	V_{REF} = $5V_{P-P}$, Data = $FFFF_H$	4	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0V, Data 0000_H to 8000_H to 0000_H	7	nV-s typ
Feed Through Error	V_{OUT}/V_{REF}	Data = 0000_H, V_{REF} = 100mVrms, same channel	-65	dB
Digital Feed Through	Q	$\overline{WR}$ = 1, LDAC =1, and f_{CLK} = 1MHz	7	nV-s typ
Total Harmonic Distortion	THD	V_{REF} = $5V_{P-P}$, Data = $FFFF_H$, f=1KHz	-85	dB typ
Output Spot Noise Voltage	e_N	f = 1kHz, BW = 1Hz	12	nV/ rt Hz

NOTES:

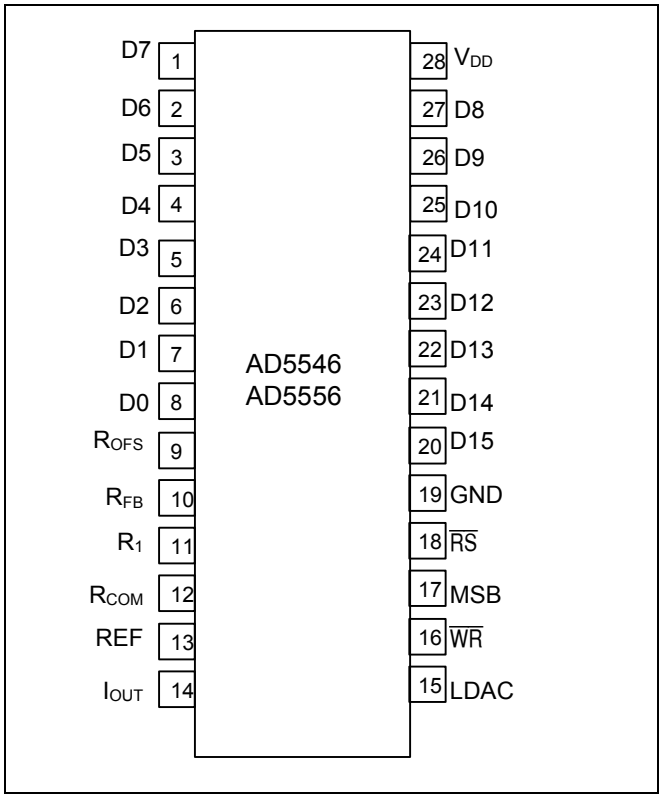
1. All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 I-to-V converter amplifier. The AD5546 R_{FB} terminal is tied to the amplifier output. The opamp +IN is grounded and the DAC I_{OUT} is tied to the opamp –IN. Typical values represent average readings measured at 25°C.
2. These parameters are guaranteed by design and not subject to production testing.
3. All input control signals are specified with t_R = t_F = 2.5ns (10% to 90% of +3V) and timed from a voltage level of 1.5V.
4. All AC Characteristic tests are performed in a closed loop system using an AD841 I-to-V converter amplifier.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... –0.3V, +8V
R_{FB}, R_{OFS}, R_1, R_{COM}, and REF to GND ..... –18V, 18V
Logic Inputs to GND ..... –0.3V, +8V
$V(I_{OUT})$ to GND ..... –0.3V, V_{DD} + 0.3V
Input Current to Any Pin except Supplies ..... ±50mA
Package Power Dissipation..... $(T_{J\ MAX} – T_A)/ THETA_{JA}$
Thermal Resistance $THETA_{JA}$ ..... 128°C
Maximum Junction Temperature ($T_{J\ MAX}$) ..... 150°C
Operating Temperature Range
Models B, C ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature:
Vapor Phase, 60 secs ..... +215°C
Infrared, 15 secs..... +220°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



TSSOP-28

PIN DESCRIPTION

PIN#	Name	Function
1-8	D7 to D0	Digital Input Data Bits D7 to D0
9	R_{OFS}	Bipolar Offset Resistor
10	R_{FB}	Internal matching Feedback Resistor. Connects to external opamp output for I-V conversion.
11	R_1	4-Quandrant Resistor R1.
12	R_{COM}	Reference Input and 4-Quadrant Resistor R2.
13	REF	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
14	I_{OUT}	DAC current-output. Connects to inverting terminal of external precision I to V opamp for voltage output.
15	LDAC	Digital Input Load DAC Control.
16	$\overline{WR}$	Write control digital input in active low. Transfers shift-register data to DAC register on rising edge.
17	MSB	Power On Reset State. MSB=0 resets at zero-scale, MSB=1 resets at mid-scale.
18	$\overline{RS}$	Reset. Resets to zero-scale if MSB=0 and resets to mid-scale if MSB=1
19	GND	Analog and Digital Grounds.
20-27	D15 to D8	Digital Input Data Bits D15 to D8
28	V_{DD}	Positive power supply input. Specified range of operation +5V ±10%.

ORDERING GUIDE

Model	RES (Bit)	DNL (LSB)	INL (LSB)	TEMP	Package Description	Package Option
AD5546BRU	16	±1	±2	-40 / +85°C	TSSOP-28	RU-28
AD5556CRU	14	±1	±1	-40 / +85°C	TSSOP-28	RU-28

The AD5546 contains 1624 transistors. The die size measures 62 mil X 94 mil, 5828 sq mil.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5546/AD5556 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

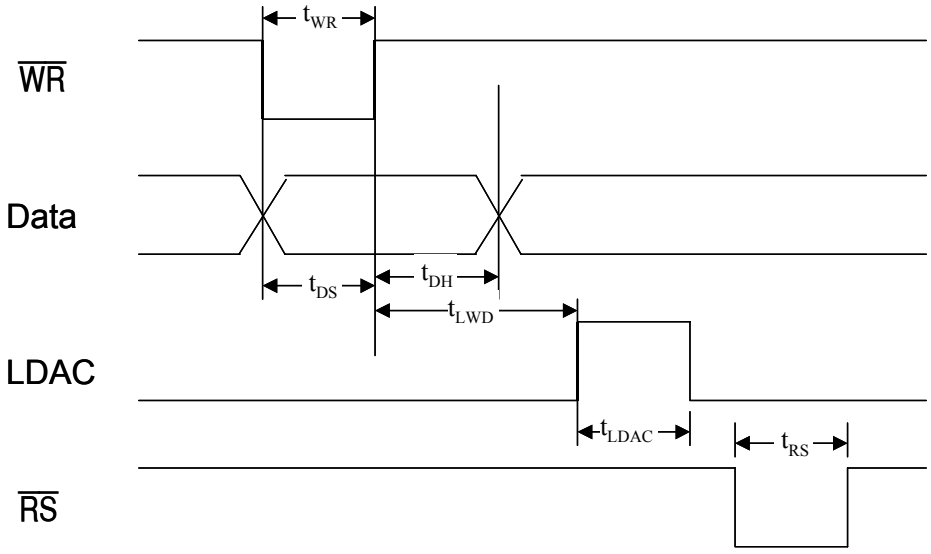


Figure 2. AD5546/AD5556 Timing Diagram

Table I. AD5546 Serial Input Register Data Format; Data is loaded in the MSB-First Format.

	MSB															LSB
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table II. AD5556 Serial Input Register Data Format; Data is loaded in the MSB-First Format.

	MSB													LSB
Bit Position	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data Word	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A full 16-bit data word can be loaded into AD5556 serial input register, but only the last 14-bits entered will be transferred to the DAC register when $\overline{WR}$ returns to logic high.

Table III. Control Inputs

$\overline{RS}$	$\overline{WR}$	LDAC	Register Operation
0	X	X	Reset Output to 0 with MSB=0 and MS with MSB=1
1	0	0	Load Input Register with Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1	0	1	Input and DAC Register are Transparent
1	⎍	⎍	When LDAC and $\overline{WR}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC Register on the rising edge of the pulse
1	1	0	No Register Operation

CIRCUIT OPERATION

The AD5546/AD5556 contains a 16-/14-bit, current-output, digital-to-analog converter with parallel input data interface.

D/A Converter Section

The DAC architecture uses a current-steering R-2R ladder design. Figure 3 shows the typical equivalent DAC structure. The DAC contains a matching feedback resistor for use with an external opamp, Figure 4. With R_{FB} and I_{OUT} terminals connect to the opamp output and inverting node respectively, a precision voltage output can be achieved as:

$V_{OUT} = -V_{REF} * D / 65,536$ (AD5546) (1)

$V_{OUT} = -V_{REF} * D / 16,384$ (AD5556) (2)

Note that the output voltage polarity is opposite to the V_{REF} polarity for DC reference voltages.

These DACS are designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the internal logic to drive the DAC switches ON and OFF states.

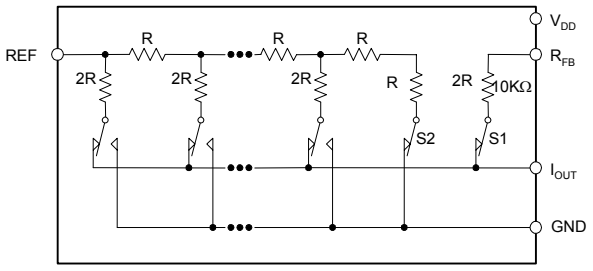


Figure 3. Equivalent R-2R DAC Circuit

Note that a matching switch is used in series with the internal 10kΩ feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} in order to achieve continuity.

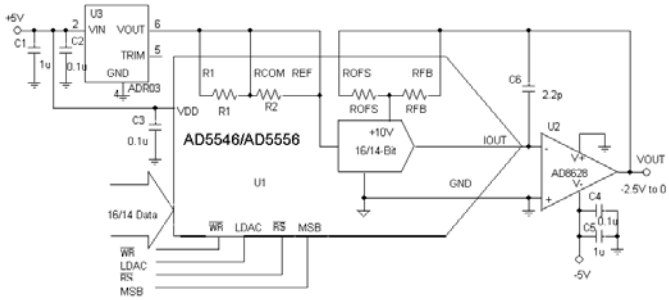


Figure 4. Unipolar 2-Quadrant Multiplication, V_{OUT}=0 to -V_{REF}

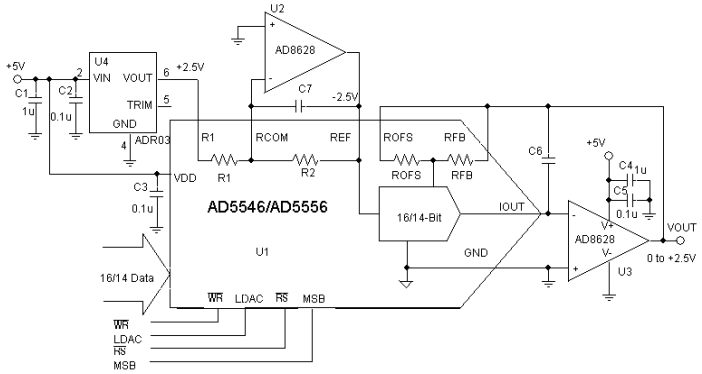


Figure 5. Unipolar 2-Quadrant Multiplication, V_{OUT}=0 to +V_{REF}

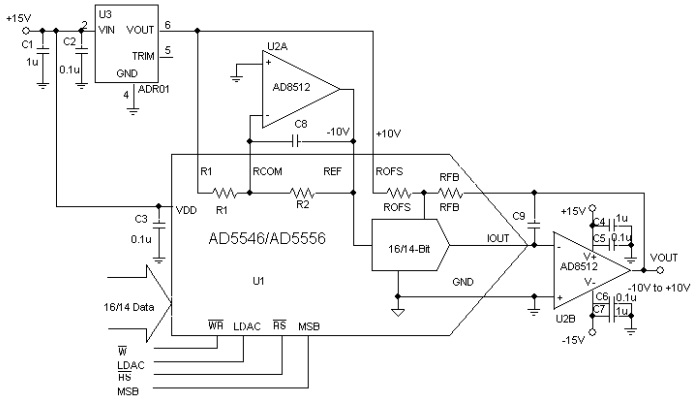


Figure 6. 4-Quadrant Multiplication, V_{OUT}=-V_{REF} to +V_{REF}

These DACs are also designed to accommodate AC reference input signals. The AD5546 will accommodate input reference voltages in the range of -12 to +12 volts. The reference voltage inputs exhibit a constant nominal input-resistance value of 5kΩ, ±30%. The DAC output (I_{OUT}) is code-dependent producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5546 on the amplifiers inverting input node. The feedback resistance in parallel with the DAC ladder resistance dominates output voltage noise. In order to maintain good analog performance, power supply bypassing of 0.01µF to 0.1µF ceramic or chip capacitors in parallel with a 1µF tantulum capacitor is recommended. Due to degradation of power supply rejection ratio in frequency, users should not use switching regulator as the source of power supply.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zeners connected to ground (GND) and V_{DD} as shown in Figure 4.

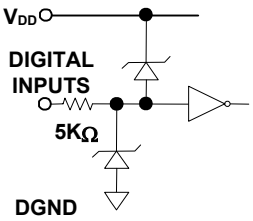


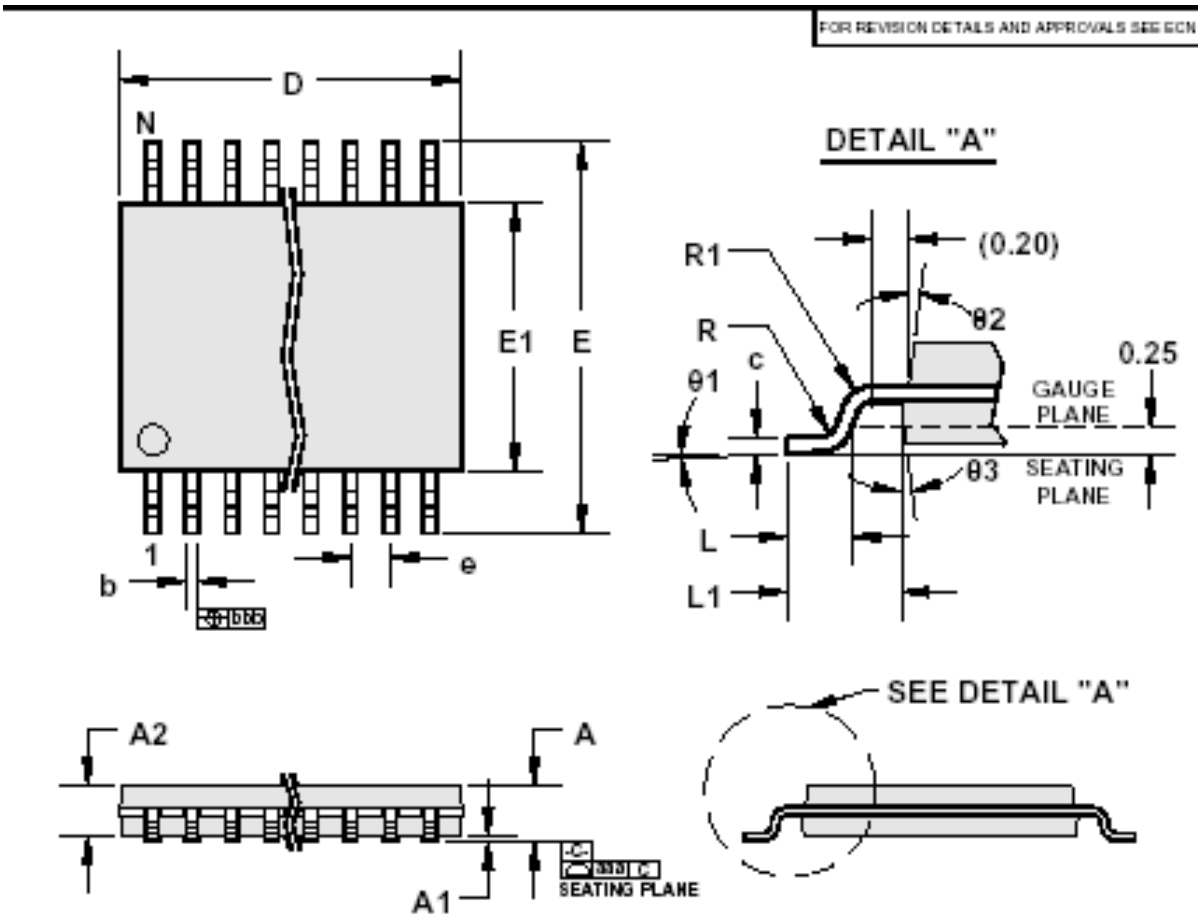
Figure 7. Equivalent ESD Protection Circuits

PCB Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum-lead length PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01uF-0.1uF disc or chip ceramics capacitors. Low-ESR 1uF to 10 uF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error.

Mechanical Outline Dimensions



# of LDS	D		
	Min	Nom	Max
8	2.90	3.00	3.10
14	4.90	5.00	5.10
16	4.90	5.00	5.10
20	6.40	6.50	6.60
24	7.70	7.80	7.90
28	9.60	9.70	9.80

Dim	Min.	Nom.	Max
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
b	0.19		0.30
c	0.09		0.20
L	0.45	0.60	0.75
L1		1.0 REF	
R	0.09		
R1	0.09		
θ1	0°		8°
θ2		12° REF	
θ3		12° REF	
aaa		0.10	
bbb		0.10	

NOTES:

1. Controlling Dimensions are in mm.
2. All Dimensions per JEDEC Standards MO-153

Title: TSSOP 4.40mm
Package Outline