

Low Cost, Low Power, True RMS-to-DC Converter

AD737*

FEATURES

Computes:

True rms Value Average Rectified Value Absolute Value

Provides:

200 mV Full-Scale Input Range
(Larger Inputs with Input Attenuator)
Direct Interfacing with 3 1/2 Digit
CMOS A/D Converters
High Input Impedance of 10¹² O

High Input Impedance of $10^{12} \Omega$ Low Input Bias Current: 25 pA Max

High Accuracy: ± 0.2 mV $\pm 0.3\%$ of Reading

RMS Conversion with Signal Crest Factors up to 5
Wide Power Supply Range: ±2.5 V to ±16.5 V

Low Power: 160 μA Max Supply Current

No External Trims Needed for Specified Accuracy AD736—A General-Purpose, Buffered Voltage

Output Version Also Available

GENERAL DESCRIPTION

The AD737 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ± 0.2 mV $\pm 0.3\%$ of reading with sine wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms precision rectifiers in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac-coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of $100~\mu V$ rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200~mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output. This allows the device to be highly compatible with high input impedance A/D converters.

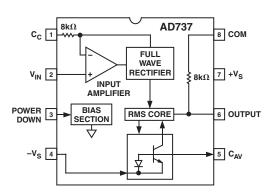
Requiring only 160 μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery-powered

*Protected under U.S. Patent Number 5,495,245.

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FUNCTIONAL BLOCK DIAGRAM



applications. This converter also provides a power-down feature that reduces the power supply standby current to less than $30 \,\mu\text{A}$.

The AD737 allows the choice of two signal input terminals: a high impedance ($10^{12}\,\Omega$) FET input that directly interfaces with high Z input attenuators and a low impedance (8 k Ω) input that allows the measurement of 0.9 V input levels while operating from the minimum power supply voltage of ± 2.5 V. The two inputs may be used either single-ended or differentially.

The AD737 achieves 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW.

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of -20° C to $+85^{\circ}$ C. The AD737JR-5 is tested with supply voltages of ± 2.5 V dc. The AD737A and AD737B grades are rated over the industrial temperature range of -40° C to $+85^{\circ}$ C.

The AD737 is available in three low cost, 8-lead packages: PDIP, SOIC, and CERDIP.

PRODUCT HIGHLIGHTS

- 1. The AD737 is capable of computing the average rectified value, absolute value, or true rms value of various input signals.
- 2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
- 3. The low power consumption of 0.72 mW makes the AD737 suitable for battery-powered applications.

AD737—SPECIFICATIONS (@ 25°C, ± 5 V supplies, except AD737J-5, ± 2.5 V, $C_{AV} = 33$ μF , $C_{C} = 10$ μF , f = 1 kHz, sine wave input applied to Pin 2, unless otherwise specified.)

			737 J/AD			37 K/AD 7		1	AD737J-		
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Typ	Max	Unit
TRANSFER FUNCTION					V_{OUT}	$=\sqrt{Avg}$	$\left(V_{IN}^{2}\right)$				
CONVERSION ACCURACY Total Error	E_{IN} = 0 to 200 mV rms $\pm V_S$ = ± 2.5 V $\pm V_S$ = ± 2.5 V, Input to Pin 1		0.2/0.3	0.4/0.5		0.2/0.2	0.2/0.3			0.4/0.5 0.4/0.5	POR
T to T	$E_{IN} = 200 \text{ mV} - 1 \text{ V rms}$		-1.2	± 2.0		-1.2	± 2.0				POR
$T_{ m MIN}$ to $T_{ m MAX}$ A and B Grades J and K Grades	E_{IN} = 200 mV rms E_{IN} = 200 mV rms, $\pm V_S$ = ±2.5 V		0.007	0.5/0.7		0.007	0.3/0.5		0.02		±mV/±POR ±POR/°C
vs. Supply Voltage $\pm V_S = \pm 2.5 \text{ V to } \pm 5 \text{ V}$ $\pm V_S = \pm 5 \text{ V to } \pm 16.5 \text{ V}$ DC Reversal Error, DC-Coupled	$E_{IN} = 200 \text{ mV rms}$ $V_{IN} = 600 \text{ mV dc}$	0	-0.18 +0.06 1.3	-0.3 +0.1 2.5	0	-0.18 +0.06 1.3	-0.3 +0.1 2.5	0	-0.18 +0.06	-0.3 +0.1	%/V %/V POR
Nonlinearity ² Input to Pin 1, AC-Coupled ³	V_{IN} = 200 mV dc, $\pm V_S$ = ± 2.5 V E_{IN} = 0 to 200 mV rms E_{IN} = 100 mV rms E_{IN} = 100 mV rms, after correction	0	+0.25	+0.35	0	+0.25	+0.35		1.7	2.5	POR
Total Error, External Trim	$\pm V_S = \pm 2.5 \text{ V}$ $E_{IN} = 0 \text{ to } 200 \text{ mV rms}$		0.1/0.2			0.1/0.2			0.02 0.1/0.2	0.1	POR ±mV/±POR
ADDITIONAL CREST FACTOR ERROR ⁴ Crest Factor = 1 to 3	$C_{AV} = C_F = 100 \mu F$ $C_{AV} = 22 \mu F$, $C_F = 100 \mu F$, $\pm V_S =$ $\pm 2.5 \text{ V}$, Input to Pin 1 $C_{AV} = C_F = 100 \mu F$		0.7			0.7			1.7		% %
INPUT CHARACTERISTICS High Z Input (Pin 2) Signal Range Continuous RMS Level Peak Transient Input	$\pm V_{S} = +2.5 \text{ V}$ $\pm V_{S} = +2.8 \text{ V}, -3.2 \text{ V}$ $\pm V_{S} = \pm 5 \text{ V to } \pm 16.5 \text{ V}$ $\pm V_{S} = +2.5 \text{ V},$ Input to Pin 1 $\pm V_{S} = +2.8 \text{ V}, -3.2 \text{ V}$ $\pm V_{S} = \pm 5 \text{ V}$ $\pm V_{S} = \pm 16.5 \text{ V}$	±0.9 ±4.0	±2.7	200 1		±0.9 ±4.0	200 1 ±2.7	±0.6		200	mV rms mV rms V rms V v
Input Resistance Input Bias Current Low Z Input (Pin 1) Signal Range Continuous RMS Level	$\pm V_S = \pm 5 \text{ V}$ $\pm V_S = +2.5 \text{ V}$ $\pm V_S = +2.8 \text{ V}, -3.2 \text{ V}$		10 ¹² 1	25 300		10 ¹² 1	25 300		10 ¹² 1	25 300	Ω pA mV rms mV rms
Peak Transient Input			±1.7 ±3.8 ±11	1		±1.7 ±3.8 ±11	1		±1.7		V rms V V V
Input Resistance Maximum Continuous Nondestructive Input, All Supply Voltages Input Offset Voltage ⁵ vs. Temperature vs. Supply	AC-Coupled $V_S = \pm 2.5 \text{ V to } \pm 5 \text{ V}$ $V_S = \pm 5 \text{ V to } \pm 16.5 \text{ V}$	6.4	8 8 80 50	9.6 ±12 ±3 30 150	6.4	8 8 80 50	9.6 ±12 ±3 30 150	6.4	8 8 80	9.6 ±12 ±3 30	$\begin{array}{c} k\Omega \\ \\ V \ p-p \\ mV \\ \mu V/^{\circ}C \\ \mu V/V \\ \mu V/V \end{array}$

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		AD737J/AD737A		AD737K/AD737B			AD737J-5				
Parameter	Conditions	Min	-	Max	Min	Typ	Max	Min	Тур	Max	Unit
OUTPUT CHARACTERISTICS	No Load										
Output Voltage Swing	$\pm V_S = +2.8 \text{ V}, -3.2 \text{ V}$	1.6	-1.7		-1.6	-1.7					V
. 0 0	$\pm V_S = \pm 5 \text{ V}$	-3.3	-3.4		-3.3	-3.4					V
	$\pm V_S = \pm 16.5 \text{ V}$	-4	-5		-4	-5					V
	$\pm V_S = \pm 2.5 \text{ V}, \text{ (Pin 1)}$							-1.1	-0.9		V
Output Resistance	dc	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE											
High Impedance Input (Pin 2)											
For 1% Additional Error	$V_{IN} = 1 \text{ mV rms}$		1			1			1		kHz
	$V_{IN} = 10 \text{ mV rms}$		6			6			6		kHz
	$V_{IN} = 100 \text{ mV rms}$		37			37			37		kHz
	$V_{IN} = 200 \text{ mV rms}$		33			33			33		kHz
For 3 dB Bandwidth	$V_{IN} = 1 \text{ mV rms}$		5			5			5		kHz
	$V_{IN} = 10 \text{ mV rms}$		55			55			55		kHz
	$V_{IN} = 100 \text{ mV rms}$		170			170			170		kHz
	$V_{IN} = 200 \text{ mV rms}$		190			190			190		kHz
Low Z Input (Pin 1)											
For 1% Additional Error	$V_{IN} = 1 \text{ mV rms}$		1			1			1		kHz
	$V_{IN} = 10 \text{ mV rms}$		6			6			6		kHz
	$V_{IN} = 40 \text{ mV rms}$								25		kHz
	$V_{IN} = 100 \text{ mV rms}$		90			90			90		kHz
	$V_{IN} = 200 \text{ mV rms}$		90			90			90		kHz
For 3 dB Bandwidth	$V_{IN} = 1 \text{ mV rms}$		5			5			5		kHz
	$V_{IN} = 10 \text{ mV rms}$		55			55			55		kHz
	$V_{IN} = 100 \text{ mV rms}$		350			350			350		kHz
	$V_{IN} = 200 \text{ mV rms}$		460			460			460		kHz
POWER DOWN											
Disable Voltage			0			0					V.
Input Current, PD Enabled	$+V_{PD} = +V_{S}$		11			11					μA
POWER SUPPLY											
Operating Voltage Range		+2.8/-3.2	±5	± 16.5	+2.8/-3.2		±16.5	±2.5	±5	± 16.5	V
Current	No Input		120	160		120	160		120	160	μA
	Rated Input		170	210		170	210		170	210	μA
	Power Down		25	40		25	40		25	40	μΑ
TEMPERATURE RANGE					See the O	rderin	g Guide				

NOTES

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¹POR = % of Reading.

²Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 V and 200 mV rms.

³After fourth order error correction using the equation $y = -0.31009x^4 - 0.21692x^3 - 0.06939x^2 + 0.99756x + 11.1 \times 10^{-6}$, where y is the corrected result and x is the device output between 0.01 V and 0.3 V.

⁴Crest factor error is specified as the additional error resulting from the specific crest factor, using a 200 mV rms signal as a reference. The crest factor is defined as V_{PEAK}/V rms.
⁵DC offset does not limit ac resolution.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS1

Supply Voltage
Internal Power Dissipation ² 200 mW
Input Voltage
Output Short-Circuit Duration Indefinite
Differential Input Voltage $\dots + V_S$ and $-V_S$
Storage Temperature Range (Q)65°C to +150°C
Storage Temperature Range (N, R)65°C to +125°C
Lead Temperature Range (Soldering 60 sec) 300°C
ESD Rating

NOTES

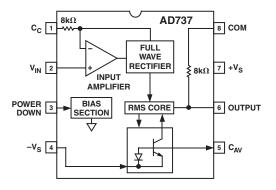
¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²8-Lead PDIP Package: $\theta_{IA} = 165^{\circ}$ C/W.

8-Lead CERDIP Package: $\theta_{JA} = 110^{\circ}\text{C/W}$.

8-Lead SOIC: $\theta_{JA} = 155^{\circ}\text{C/W}$.

PIN CONFIGURATION PDIP (N-8), CERDIP (Q-8), SOIC (R-8)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD737AQ	–40°C to +85°C	CERDIP	Q-8
AD737BQ	−40°C to +85°C	CERDIP	Q-8
AD737JN	0°C to 70°C	PDIP	N-8
AD737JR	0°C to 70°C	SOIC	R-8
AD737JR-REEL	0°C to 70°C	13" Tape and Reel	R-8
AD737JR-REEL7	0°C to 70°C	7" Tape and Reel	R-8
AD737JR-5	0°C to 70°C	SOIC	R-8
AD737JR-5-REEL	0°C to 70°C	13" Tape and Reel	R-8
AD737JR-5-REEL7	0°C to 70°C	7" Tape and Reel	R-8
AD737KN	0°C to 70°C	PDIP	N-8
AD737KR	0°C to 70°C	SOIC	R-8
AD737KR-REEL	0°C to 70°C	13" Tape and Reel	R-8
AD737KR-REEL7	0°C to 70°C	7" Tape and Reel	R-8

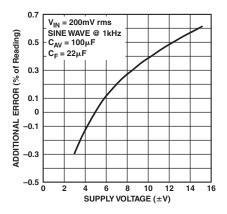
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD737 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

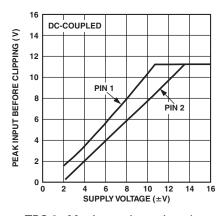


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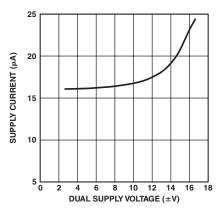
Typical Performance Characteristics—AD737



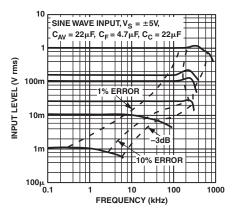
TPC 1. Additional Error vs. Supply Voltage



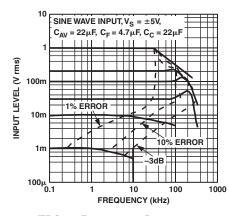
TPC 2. Maximum Input Level vs. Supply Voltage



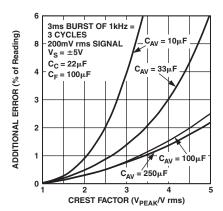
TPC 3. Power-Down Current vs. Supply Voltage



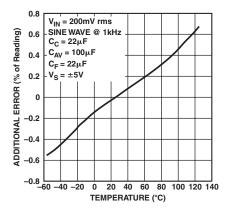
TPC 4. Frequency Response Driving Pin 1



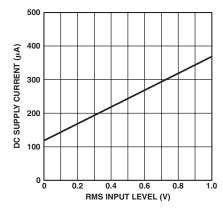
TPC 5. Frequency Response Driving Pin 2



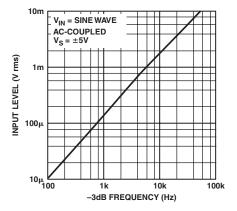
TPC 6. Additional Error vs. Crest Factor vs. C_{AV}



TPC 7. Additional Error vs. Temperature

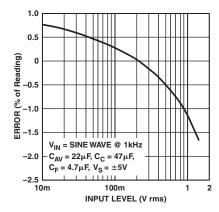


TPC 8. DC Supply Current vs. RMS Input Level

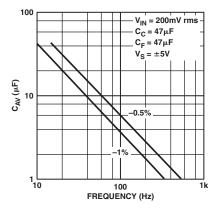


TPC 9. RMS Input Level (Pin 2) vs. –3 dB Frequency

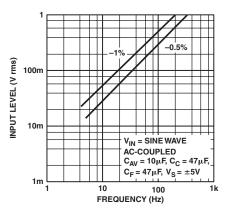
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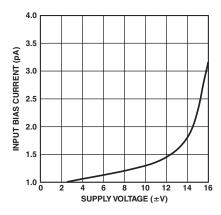
TPC 10. Error vs. RMS Input Voltage (Pin 2) Using Circuit of Figure 6



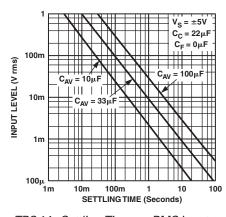
TPC 11. C_{AV} vs. Frequency for Specified Averaging Error



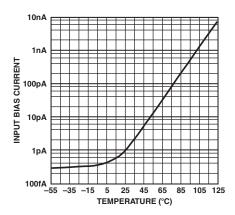
TPC 12. RMS Input Level vs. Frequency for Specified Averaging Error



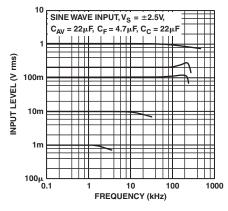
TPC 13. Pin 2 Input Bias Current vs. Supply Voltage



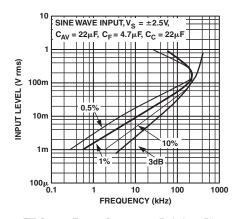
TPC 14. Settling Time vs. RMS Input Level for Various Values of C_{AV}



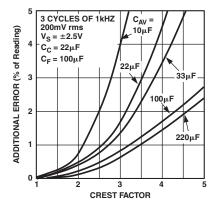
TPC 15. Pin 2 Input Bias Current vs. Temperature



TPC 16. Frequency Response Driving Pin 1

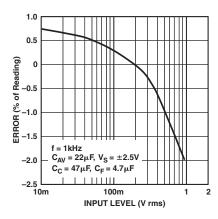


TPC 17. Error Contours Driving Pin 1



TPC 18. Additional Crest Factor Error for Various Values of C_{AV}

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TPC 19. Error vs. Input Voltage Driving Pin 1

CALCULATING SETTLING TIME USING TPC 14

TPC 14 may be used to closely approximate the time required for the AD737 to settle when its input level is reduced in amplitude. The net time required for the rms converter to settle is the difference between two times extracted from the graph—the initial time minus the final settling time. As an example, consider the following conditions: a 33 µF averaging capacitor, an initial rms input level of 100 mV, and a final (reduced) input level of 1 mV. From TPC 14, the initial settling time (where the 100 mV line intersects the 33 µF line) is around 80 ms. The settling time corresponding to the new or final input level of 1 mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value is 8 seconds minus 80 ms, which is 7.92 seconds. Note that because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., not the settling time to 1%, 0.1%, and so on, of the final value). Also, this graph provides the worst-case settling time, since the AD737 settles very quickly with increasing input levels.

TYPES OF AC MEASUREMENT

The AD737 is capable of measuring ac signals by operating as either an average responding or a true rms-to-dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac and dc) voltage or current by full wave rectifying and low-pass filtering the input signal; this approximates the average. The resulting output, a dc average level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine wave voltage is 0.636 that of $V_{\rm PEAK}$; the corresponding rms value is 0.707 times $V_{\rm PEAK}$. Therefore, for sine wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the average value, true rms measurement is a universal language among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of a dc voltage; an ac signal of 1 V rms produces the same amount of heat in a resistor as a 1 V dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as

$$V rms = \sqrt{Avg(V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are smart rectifiers; they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error depends on the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine wave voltages and then is used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table I).

Table I. Error Introduced by an Average Responding Circuit When Measuring Common Waveforms

Waveform Type 1 V Peak Amplitude	Crest Factor (V _{PEAK} /V rms)	True RMS Value (V)	Average Responding Circuit Calibrated to Read RMS Value of Sine Waves Will Read (V)	Reading Error Using Average Responding Circuit (%)
Undistorted Sine Wave	1.414	0.707	0.707	0
Symmetrical Square Wave	1.00	1.00	1.11	11.0
Undistorted Triangle Wave	1.73	0.577	0.555	-3.8
Gaussian Noise				
(98% of Peaks <1 V)	3	0.333	0.295	-11.4
Rectangular	2	0.5	0.278	-44
Pulse Train	10	0.1	0.011	-89
SCR Waveforms				
50% Duty Cycle	2	0.495	0.354	-28
25% Duty Cycle	4.7	0.212	0.150	-30

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AD737 THEORY OF OPERATION

As shown by Figure 1, the AD737 has four functional subsections: input amplifier, full-wave rectifier, rms core, and bias section. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide dynamic range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators. The input signal may be either dc-coupled or ac-coupled to the input amplifier. Unlike other rms converters, the AD737 permits both direct and indirect ac coupling of the inputs. AC coupling is provided by placing a series capacitor between the input signal and Pin 2 (or Pin 1) for direct coupling and between Pin 1 and ground (while driving Pin 2) for indirect coupling.

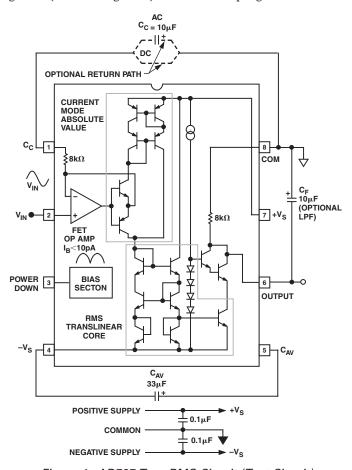


Figure 1. AD737 True RMS Circuit (Test Circuit)

The output of the input amplifier drives a full-wave precision rectifier, which in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging, and square rooting are performed, using an external averaging capacitor, C_{AV} . Without C_{AV} , the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 2).

A final subsection, the bias section, permits a power-down function. This reduces the idle current of the AD737 from 160 μA down to a mere 30 μA . This feature is selected by tying Pin 3 to the +Vs terminal. In the average responding connection, all of the averaging is carried out by an RC post filter consisting of an 8 k Ω internal scale-factor resistor connected between Pins 6 and 8 and an external averaging capacitor, C_F . In the rms circuit, this additional filtering stage helps reduce any output ripple that was not removed by the averaging capacitor, C_{AV} .

RMS MEASUREMENT—CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV} , holds the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant increases exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging decrease while the time it takes for the circuit to settle to the new rms level increases. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV} , a trade-off between computational accuracy and settling time is required.

RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION

Because the average responding connection shown in Figure 2 does not use an averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of $C_{\rm F}$ and the internal 8 $k\Omega$ output scaling resistor.

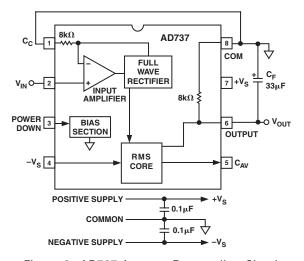


Figure 2. AD737 Average Responding Circuit

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 3 shows the typical output waveform of the AD737 with a sine wave input voltage applied. As with all real-world devices, the ideal output of $V_{\rm OUT}$ = $V_{\rm IN}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.

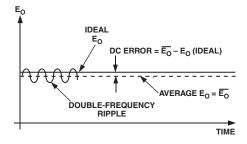


Figure 3. Output Waveform for Sine Wave Input Voltage

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of the

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averaging capacitor used—no amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value. The ac error component, an output ripple, may be easily removed by using a large enough post filtering capacitor, C_F .

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors $C_{\rm AV}$ and $C_{\rm F}$. This combined error, representing the maximum uncertainty of the measurement, is termed the averaging error and is equal to the peak value of the output ripple plus the dc error. As the input frequency increases, both error components decrease rapidly; if the input frequency doubles, the dc error and ripple reduce to one quarter and one half of their original values, respectively, and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (Crest Factor = V_{PEAK}/V rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (\geq 2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms

0-100 mV

0-200 mV

0-100 mV

Audio Applications

Speech

Music

require a long averaging time constant (to average out the long time periods between pulses). TPC 6 shows the additional error versus the crest factor of the AD737 for various values of $C_{\rm AV}$.

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}), AND FILTERING (C_F) CAPACITORS

Table II provides practical values of C_{AV} and C_{F} for several common applications.

The input coupling capacitor, C_C , in conjunction with the 8 k Ω internal input scaling resistor, determines the -3 dB low frequency roll-off. This frequency, F_L , is equal to

$$F_L = \frac{1}{2\pi (8,000) (The Value of C_C in Farads)}$$

Note that at F_L , the amplitude error is approximately -30% (-3 dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one tenth of the lowest frequency to be measured.

In addition, if the input voltage has more than 100 mV of dc offset, then the ac coupling network at Pin 2 should be used in addition to capacitor C_C .

Application	RMS Input Level	Cutoff (-3 dB)	Max Crest Factor	C _{AV}	C_{F}	Settling Time* to 1%
General-Purpose	0-1 V	20 Hz	5	150 μF	10 μF	360 ms
RMS Computation		200 Hz	5	15 μF	1 μF	36 ms
	0-200 mV	20 Hz	5	33 μF	10 μF	360 ms
		200 Hz	5	3.3 μF	1 μF	36 ms
General-Purpose	0-1 V	20 Hz		None	33 μF	1.2 sec
Average		200 Hz		None	3.3 μF	120 ms
Responding						
	0-200 mV	20 Hz		None	33 μF	1.2 sec
		200 Hz		None	3.3 μF	120 ms
SCR Waveform	0-200 mV	50 Hz	5	100 μF	33 μF	1.2 sec
Measurement		60 Hz	5	82 μF	27 μF	1.0 sec

5

5

3

10

50 uF

47 µF

1.5 μF

100 μF

33 uF

27 µF

 $0.5 \, \mu F$

68 µF

1.2 sec

1.0 sec

18 ms

2.4 sec

Table II. AD737 Capacitor Selection Chart

50 Hz

60 Hz

300 Hz

20 Hz

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^{*}Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times are greater for decreasing amplitude input signals.

Applications Circuits

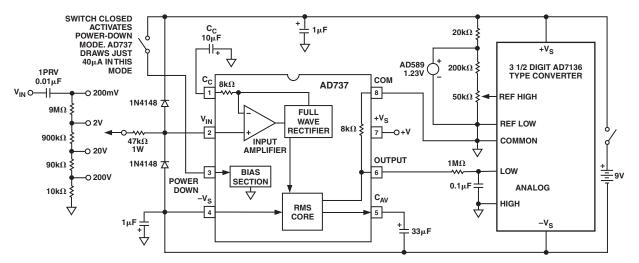


Figure 4. 3 1/2 Digit DVM Circuit

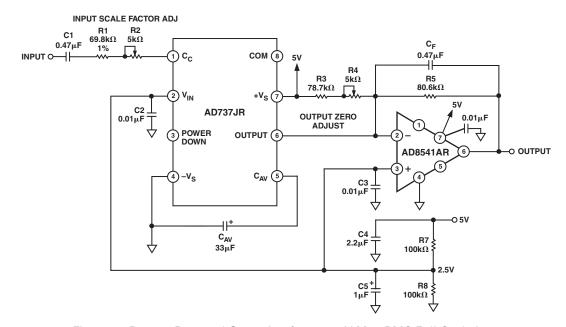


Figure 5. Battery-Powered Operation for 200 mV Max RMS Full-Scale Input

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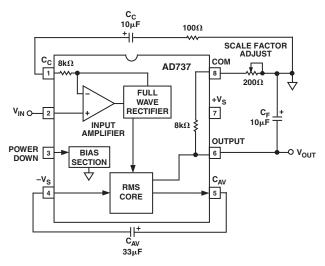


Figure 6. External Scale Factor Trim

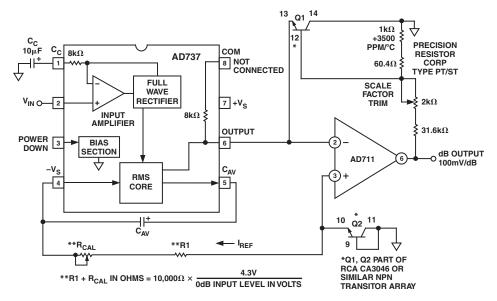


Figure 7. dB Output Connection

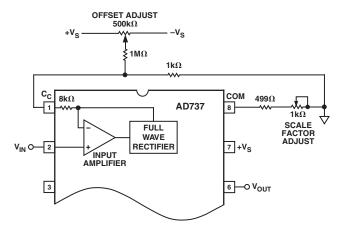


Figure 8. DC-Coupled V_{OS} and Scale Factor Trims

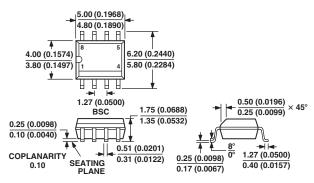
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OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC] Narrow Body

(R-8)

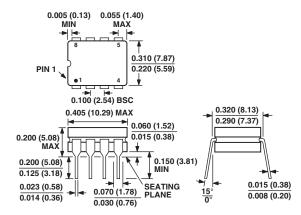
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)

Dimensions shown in inches and (millimeters)

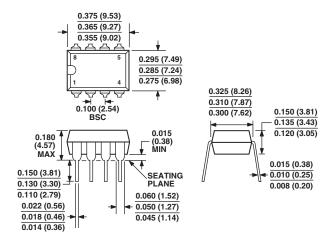


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual-In-Line Package [PDIP]

(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
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Revision History

Location	Page
6/03—Data Sheet changed from REV. D to REV. E.	
Added AD737JR-5	Universal
Changes to FEATURES	
Changes to GENERAL DESCRIPTION	
Changes to SPECIFICATIONS	
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to ORDERING GUIDE	4
Added TPCs 16 through 19	6
Changes to Figures 1 and 2	
Changes to Figure 8	
Updated OUTLINE DIMENSIONS	
12/02—Data Sheet changed from REV. C to REV. D.	
Changes to FUNCTIONAL BLOCK DIAGRAM	
Changes to PIN CONFIGURATION	
Figure 1 replaced	
Changes to Figure 2	
Figure 5 replaced	
Changes to Application Circuits Figures 4, 6–8	
OUTLINE DIMENSIONS updated	

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