ANALOG DEVICES

Low Power, 16/24-Bit Sigma-Delta ADC

Preliminary Data Sheet

AD7788/AD7789

FEATURES
AD7788 Has 16-Bit Resolution
AD7789 Has 24-Bit Resolution
POWER
    Specified for Single 3 V and 5 V Operation
    Normal: 65 µA typical
Power-Down: 1 µA
RMS Noise: 1.5 µV
AD7788: 16-Bit p-p Resolution
AD7789: 19-Bit p-p Resolution (21.5 Bits Effective
    Resolution)
Simultaneous 50 Hz and 60 Hz Rejection
Internal Clock Oscillator
VDD Monitor Channel
10-Lead µSOIC Package

INTERFACE
3-Wire Serial
SPI™, QSPI™, MICROWIRE™ and DSP-Compatible
Schmitt Trigger on SCLK

APPLICATIONS
SMART Transmitters
Battery Applications
Portable Instrumentation
Sensor Measurement
Temperature Measurement
Pressure Measurements
Weigh Scales
4 to 20 mA Loops

GENERAL DESCRIPTION

The AD7788/AD7789 are low-power, complete analog front ends for low frequency measurement applications. The AD7789 contains a 24-bit $\Sigma-\Delta$ ADC with one differential input. The AD7788 is a 16-bit version of the AD7789.

The device operates from an internal clock. Therefore, the user does not have to supply a clock source to the device. The output data rate is 16.6 Hz which gives simultaneous 50 Hz/ 60 Hz rejection.

The part operates from a single 3 V or 5 V supply. When operating from a 3 V supply, the power dissipation for the part is 195 µW typical. The AD7788/AD7789 is housed in a 10-lead µSOIC package.

FUNCTIONAL BLOCK DIAGRAM
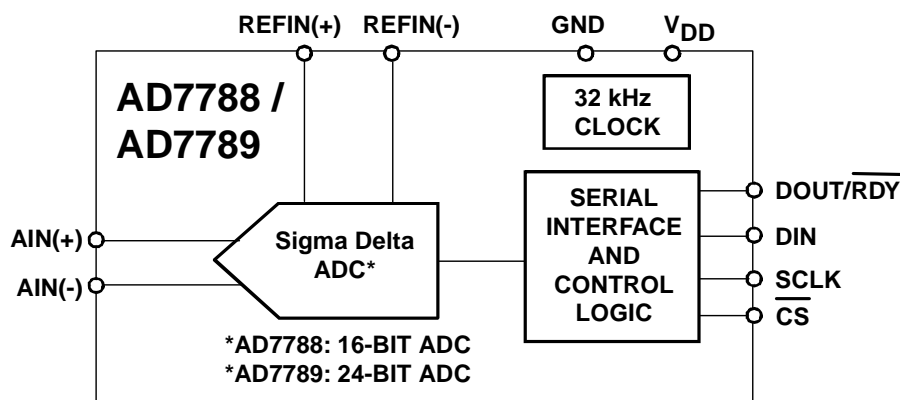
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MICROWIRE is a trademark of National Semiconductor Corporation.

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AD7789–SPECIFICATIONS[1]

(VDD = +2.7 V to +3.6 V or +4.75 V to +5.25 V; REFIN (+) = +2.5 V; REFIN(-) = GND; GND = 0 V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD7789B	Units	Test Conditions/Comments
ADC CHANNEL SPECIFICATION			
Output Update Rate	16.6	Hz nom	
ADC CHANNEL			
No Missing Codes[2]	24	Bits min	
Resolution	19	Bits p-p	
Output Noise	1.5	µV RMS typ	
Integral Nonlinearity[2]	± 15	ppm of FSR Max	
Offset Error	± 3	µV typ	
Offset Error Drift vs. Temperature	± 10	nV/^{O}C typ	
Full-Scale Error[3]	± 10	µV typ	
Gain Drift vs. Temperature	± 0.5	ppm/^{O}C typ	
Power Supply Rejection	80	dB min	100 dB typ, AIN = 1 V
ANALOG INPUTS			
Differential Input Voltage Ranges	$\pm$REFIN	V nom	REFIN = REFIN(+) - REFIN(-)
Absolute AIN Voltage Limits[2]	GND - 30 mV	V min	
	V_{DD} + 30 mV	V max	
Analog Input Current			Input current varies with Input Voltage
Average Input Current	± 350	nA/V typ	
Average Input Current Drift	± 2	pA/V/^{O}C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	70	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
Common Mode Rejection			AIN = 1 V
@ DC	90	dB min	100 dB typ
@ 50 Hz, 60 Hz[2]	100	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) - REFIN(-)
Reference Voltage Range[2]	1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND - 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	± 0.01	nA/V/^{O}C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	70	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
Common Mode Rejection			AIN = 1 V
@ DC	110	dB typ	
@ 50 Hz, 60 Hz	110	dB typ	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz

NOTES

[1]Temperature Range -40 ºC to +85 ºC.
[2]Guaranteed by design and/or characterization data on production release.
[3]Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions.
Specifications subject to change without notice.

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AD7788–SPECIFICATIONS[1] (VDD = +2.7 V to +3.6 V or +4.75 V to +5.25 V; REFIN (+) = +2.5 V; REFIN(-) = GND; GND = 0 V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD7788B	Units	Test Conditions/Comments
ADC CHANNEL SPECIFICATION			
Output Update Rate	16.6	Hz nom	
ADC CHANNEL			
No Missing Codes[2]	16	Bits min	
Resolution	16	Bits p-p	
Output Noise	1.5	μV RMS typ	
Integral Nonlinearity[2]	±15	ppm of FSR Max	
Offset Error	±3	μV typ	
Offset Error Drift vs. Temperature	±10	nV/^{O}C typ	
Full-Scale Error[3]	±10	μV typ	
Gain Drift vs. Temperature	±0.5	ppm/^{O}C typ	
Power Supply Rejection	80	dB min	100 dB typ
ANALOG INPUTS			
Differential Input Voltage Ranges	$\pm$REFIN/GAIN	V nom	REFIN = REFIN(+) - REFIN(-)
Absolute AIN Voltage Limits[2]	GND - 30 mV	V min	
	V_{DD} + 30 mV	V max	
Analog Input Current			Input current varies with Input Voltage
Average Input Current	±350	nA/V typ	
Average Input Current Drift	±2	pA/V/^{O}C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	70	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
Common Mode Rejection			AIN = 1 V
@ DC	90	dB min	100 dB typ
@ 50 Hz, 60 Hz[2]	100	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
REFERENCE INPUT			
REFIN Voltage	2.5	V nom	REFIN = REFIN(+) - REFIN(-)
Reference Voltage Range[2]	1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND - 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	μA/V typ	
Average Reference Input Current Drift	±0.01	nA/V/^{O}C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	70	dB min	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz
Common Mode Rejection			AIN = 1 V
@ DC	110	dB typ	
@ 50 Hz, 60 Hz	110	dB typ	50 $\pm$ 1 Hz, 60 $\pm$ 1 Hz

NOTES

[1]Temperature Range -40 ºC to +85 ºC.

[2]Guaranteed by design and/or characterization data on production release.

[3]Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions.

Specifications subject to change without notice.

AD7788/AD7789–SPECIFICATIONS[1]

Parameter	AD7788B/ AD7789B	Units	Test Conditions/Comments
LOGIC INPUTS			
All Inputs Except SCLK[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	V_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	V_{DD} = 5 V
$V_{T(+)}$ - $V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	V_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	V_{DD} = 3 V
$V_{T(+)}$ - $V_{T(-)}$	0.3/0.85	V min/V max	V_{DD} = 3
Input Currents	±1	µA max	V_{IN} = V_{DD}
	TBD	µA max	V_{IN} = GND
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS			
V_{OH}, Output High Voltage[2]	V_{DD} - 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset Binary		
CLOCK OSCILLATOR			
Clock Frequency	32.768 ± 2%	kHz min/max	
Start-Up Time (at Power-On)	0.5	ms typ	
	1	ms max	
POWER REQUIREMENTS[3]			
Power Supply Voltage			
V_{DD} - GND	2.7/3.6	V min/max	V_{DD} = 3 V nom
	4.75/5.25	V min/max	V_{DD} = 5 V nom
Power Supply Currents			
I_{DD} Current	65	µA typ	3 V Power Supply
	75	µA typ	5 V Power Supply
	90	µA max	
I_{DD} (power-down mode)	1	µA typ	

NOTES
[1]Temperature Range -40 ºC to +85 ºC.
[2]Guaranteed by design and/or characterization data on production release.
[3]Digital inputs equal to V_{DD} or GND.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +2.7 V to +3.6 V or +4.75 V to +5.25 V; GND = 0 V, REFIN(+) = +2.5 V, REFIN(-) = GND, Input Logic 0 = 0 V, Input Logic 1 = V_{DD}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	30.5175	μs nom	Internal Clock Period
t_4	100	ns min	SCLK High Pulsewidth
t_5	100	ns min	SCLK Low Pulsewidth
Read Operation			
t_2	0	ns min	$\overline{CS}$ Falling Edge to DOUT/$\overline{RDY}$ Active Time
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_3[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.7 V to 3.6 V
t_6[5, 6]	10	ns min	Bus Relinquish Time after $\overline{CS}$ Inactive Edge
	80	ns max	
t_7	100	ns max	SCLK Inactive Edge to $\overline{CS}$ Inactive Edge
t_8	10	ns min	SCLK Inactive Edge to DOUT/$\overline{RDY}$ High
Write Operation			
t_9	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{10}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{11}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{12}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

NOTES

[1]Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2]See Figures 2 and 3.
[3]SCLK active edge is falling edge of SCLK.
[4]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[5]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6]$\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.
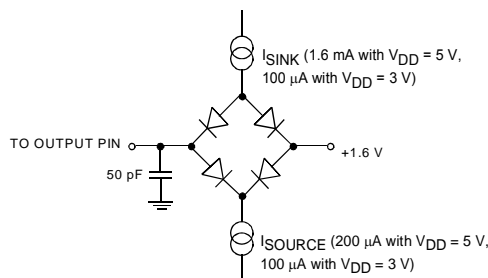

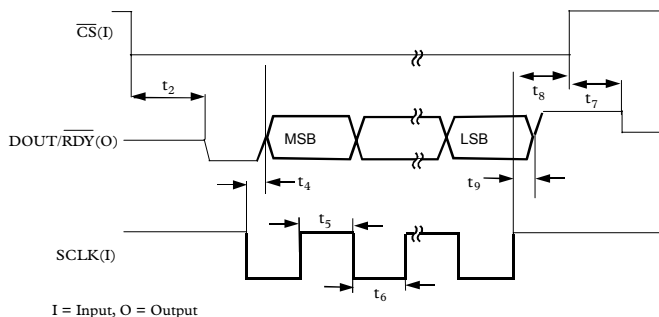Figure 1. Load Circuit for Timing Characterization
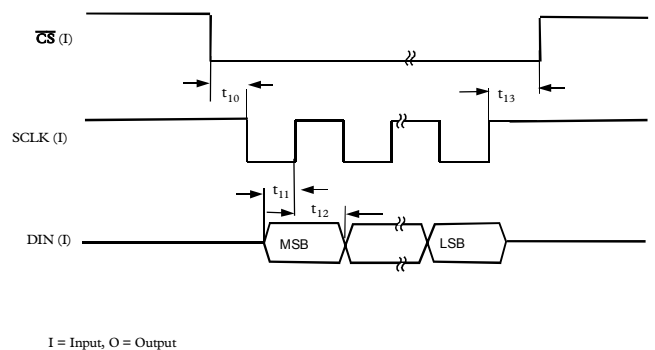

Figure 2. Read Cycle Timing Diagram

Figure 3. Write Cycle Timing Diagram

AD7788/AD7789

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to GND.. –0.3 V to +7 V
Analog Input Voltage to GND.......–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND...–0.3 V to V_{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite)................30 mA
Digital Input Voltage to GND.......–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range...............–40°C to +85°C
Storage Temperature Range.................–65°C to +150°C
Maximum Junction Temperature.......................+150°C
µSOIC Package
  θ_{JA} Thermal Impedance .206°C/W
  θ_{JC} Thermal Impedance . . . . .44°C/W
Lead Temperature, Soldering (10 sec) . . . . 300°C
  IR Reflow, Peak Temperature . . . . 220°C

NOTES
*Stresses above those listed under Absolute Maximum Ratings may cause permanent
 damage to the device. This is a stress rating only; functional operation of the device
 at these or any other conditions above those listed in the operational sections of this
 specification is not implied. Exposure to absolute maximum rating conditions for
 extended periods may affect device reliability.

PIN CONFIGURATION

SCLK	1		10	DIN
$\overline{CS}$	2	AD7788 /AD7789 TOP VIEW (Not To Scale)	9	DOUT/$\overline{RDY}$
AIN(+)	3		8	VDD
AIN(-)	4		7	GND
REF(+)	5		6	REF(-)
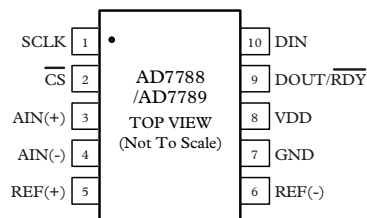
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7788BRM	–40°C to +85°C	10-Lead Micro Small Outline IC	RM-10
AD7789BRM	–40°C to +85°C	10-Lead Micro Small Outline IC	RM-10

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
accumulate on the human body and test equipment and can discharge without detection.
Although the AD7788/AD7789 features proprietary ESD protection circuitry,
permanent damage may occur on devices subjected to high energy electrostatic
discharges. Therefore, proper ESD precautions are recommended to avoid perfor-
mance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

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PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
7	GND	Ground Reference Point.
1	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a schmitt triggered input making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low allowing the ADC to operate in 3-wire mode with SCLK, DIN and DOUT used to interface with the device.
3	AIN(+)	Analog Input. AIN(+) is the positive terminal of the fully-differential analog input.
4	AIN(-)	Analog Input. AIN(-) is the negative terminal of the fully-differential analog input.
5	REFIN(+)	Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND + 1 V. The nominal reference voltage (REFIN(+) - REFIN(-)) is 2.5 V, but the part functions with a reference from 1 V to V_{DD}.
6	REFIN(-)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} - 1 V.
9	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose in this interface. When $\overline{CS}$ is low, it functions as a Serial Data Output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin when $\overline{CS}$ is low, going low to indicate the completion of a conversion. If the data is not read after the conversion, the data ready pin will go high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor indicating that valid data is available. Using an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information in placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. The end of a conversion is also indicated by the $\overline{RDY}$ bit in the Status register. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ pin is tri-stated but the $\overline{RDY}$ bit remains active.
10	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, the register selection bits of the Communications register identifying the appropriate register.
8	V_{DD}	Supply Voltage, 3 V or 5 V Nominal.

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers which are described in the following pages. In the following descriptions, Set implies a Logic 1 state and Cleared implies a Logic 0 state, unless otherwise stated.

Communications Register (RS1, RS0 = 0, 0)

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface and, on power-up or after a RESET, the ADC is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 1 outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	0(0)	RS1(0)	RS0(0)	R/$\overline{\text{W}}$(0)	CREAD(0)	CH1(0)	CH0(0)

Table 1.   Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the Communications Register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the WEN bit, the next seven bits will be loaded to the Communications Register.
CR6	0	This bit must be programmed with a logic 0 for correct operation.
CR5-CR4	RS1-RS0	Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 2.
CR3	R/$\overline{\text{W}}$	A zero in this bit location indicates that the next operation will be a write to a specified register. A one in this position indicates that the next operation will be a read from the designated register.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read i.e. the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied. The Communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 001111XX must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in the continuous read mode until an instruction is to be written to the device.
CR1-CR0	CH1-CH0	These bits are used to select the analog input channel. The differential channel can be selected (AIN(+)/AIN(-)) or an internal short (AIN(-)/AIN(-)) can be selected. Alternatively, the power supply can be selected i.e. the ADC can measure the voltage on the power supply which is useful to monitor power supply variation. The power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a 1.2V $\pm$ 5% on-chip reference as the reference source for the analog to digital conversion. Any change in channel resets the filter and a new conversion is started.

Table 2.   Register Selection Table

RS1	RS0	Register	Register Size
0	0	Communications Register during a Write Operation	8-Bit
0	0	Status Register during a Read Operation	8-Bit
0	1	Mode Register	8-Bit
1	0	Reserved	8-Bit
1	1	Data Register	16-Bit (AD7788) 24-Bit (AD7789)

Table 3.   Channel Selection Table

CH1	CH0	Channel
0	0	AIN(+) - AIN(-)
0	1	Reserved
1	0	AIN(-) - AIN(-)
1	1	V_{DD} Monitor

Status Register (RS1, RS0 = 0, 0; Power-on Reset = 00h)

The Status Register is an 8-bit read-only register. To access the ADC Status Register, the user must write to the Communications Register selecting the next operation to be a read and load bit RS2, RS1 and RS0 with 0, 0, 0. Table 4 outlines the bit designations for the Status Register. SR0 through SR7 indicate the bit loctions, SR denoting the bits are in the Status Register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/ reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{RDY}$(1)	ERR(0)	0(0)	0(0)	1(1)	WL(1/0)	CH1(0)	CH0(0)

Table 4.   Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{RDY}$	Ready bit for ADC. *Cleared* when data is written to the ADC data register. The $\overline{RDY}$ bit is *set* automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also *set* when the part is placed in powerdown mode. The end of a conversion is indicated by the DOUT/$\overline{RDY}$ pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{RDY}$ bit. *Set* to indicate that the result written to the ADC data register has been clamped to all zeros or all ones. Error sources include Overrange, Underrange. *Cleared* by a write operation to start a conversion.
SR5	0	This bit is automatically *cleared*.
SR4	0	This bit is automatically *cleared*.
SR3	1	This bit is automatically *set*.
SR2	1/0	This bit is automatically *cleared* if the device is an AD7788 and it is automically *set* if the device is an AD7789. This bit can be used to distinguish between the AD7788 and AD7789.
SR1-SR0	CH1-CH0	These bits indicate which channel is being converted by the ADC.

Mode Register (RS1, RS0 = 0, 1; Power-on Reset = 00h)

The Mode Register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for unipolar or bipolar mode or place the device is powerdown mode. Table 5 outlines the bit designations for the Mode register. MR0 through MR7 indicate the bit loctions, MR denoting the bits are in the Mode Register. MR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{RDY}$ bit.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
MD1(0)	MD0(0)	0(0)	0(0)	0(0)	U/$\overline{B}$ $(\overline{0})$	1(1)	0(0)

Table 5.   Mode Register Bit Designations

Bit Location	Bit Name	Description
MR7-MR6	MD1- MD0	Mode Select Bits. These bits select between continuous conversion mode, single conversion mode and standby mode. In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{RDY}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied or, alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period 2/fadc while subsequent conversions are available at a frequency of fadc. In single conversion mode, the ADC is placed in powerdown mode when conversions are not being performed. When single conversion mode is selected, the ADC powers up and performs a single conversion which occurs after a period 2/fadc. The conversion result in placed in the data register, $\overline{RDY}$ goes low and the ADC returns to powerdown mode. The conversion remains in the DATA register and $\overline{RDY}$ remains active (low) until another conversion is performed. See Table 6.
MR5-MR3	0	These bits must be programmed with a logic 0 for correct operation.
MR2	U/$\overline{B}$	Unipolar/Bipolar bit. *Set* by user to enable unipolar coding i.e. zero differential input will result in 0000 hex output and a full-scale differential input will result in FFFF hex output. *Cleared* by the user to enable bipolar coding. Negative full-scale differential input will result in an output code of 0000 hex, zero differential input will result in an output code of 8000 hex and a positive full-scale differential input will result in an output code of FFFF hex.
MR1	1	This bit must be programmed with a logic 1 for correct operation.
MR0	0	This bit must be programmed with a logic 0 for correct operation.

MD1	MD0	Mode
0	0	Continuous Conversion Mode (Default)
0	1	Reserved
1	0	Single Conversion Mode
1	1	Powerdown Mode

Table 6. Operating Modes

Data Register (RS1, RS0 = 1, 1; Power-on Reset = 0000h (AD7788) and 000000h (AD7789))

The conversion result from the ADC is stored in this data register. This is a read only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.