LC²MOS 12-Bit, 3.3 V Sampling ADC

AD7883

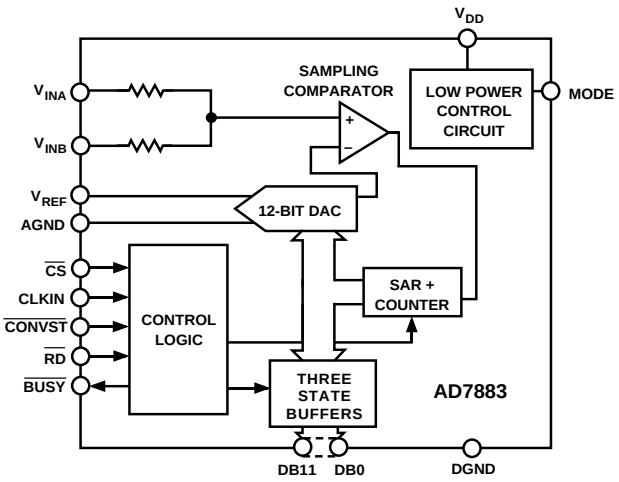
FEATURES

Battery-Compatible Supply Voltage: Guaranteed Specs for V_{DD} of 3 V to 3.6 V
12-Bit Monolithic A/D Converter
50 kHz Throughput Rate
15 μs Conversion Time
5 μs On-Chip Track/Hold Amplifier
Low Power
Power Save Mode: 1 mW typ
Normal Operation: 8 mW typ
70 dB SNR
Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS

Battery Powered Portable Systems
Laptop Computers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7883 is a high speed, low power, 12-bit A/D converter which operates from a single +3 V to +3.6 V supply. It consists of a 5 μs track/hold amplifier, a 15 μs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7883 features a total throughput time of 20 μs and can convert full power signals up to 25 kHz with a sampling frequency of 50 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7883 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7883 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. 3 V Operation
   The AD7883 is guaranteed and tested with a supply voltage of 3 V to 3.6 V. This makes it ideal for battery-powered applications where 12-bit A/D conversion is required.
2. Fast Conversion Time
   15 μs conversion time and 5 μs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
3. Low Power Consumption
   1 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.

REV. 0

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AD7883–SPECIFICATIONS (V_{DD} = +3 V to +3.6 V, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2 MHz, MODE = Logic High. All specifications T_{MIN} to T_{MAX} unless othewise noted.)

Parameter	B Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]			
Signal-to-Noise Ratio[3] (SNR)	69	dB min	Typically SNR Is 71 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Total Harmonic Distortion (THD)	–80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Peak Harmonic or Spurious Noise	–80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 50 kHz
Intermodulation Distortion (IMD)			
Second Order Terms	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
DC ACCURACY			
Resolution	12	Bits	All DC ACCURACY Specifications Apply for the Two Analog Input Ranges
Integral Nonlinearity	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±20	LSB max	
Bipolar Zero Error	±12	LSB max	
Unipolar Offset Error	±3	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	Volts	See Figure 4
	±V_{REF}	Volts	See Figure 5
Input Resistance	10	MΩ min	0 to V_{REF} Range
	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT			
V_{REF} (For Specified Performance)	V_{DD}	V	
I_{REF}	1.2	mA max	
LOGIC INPUTS			
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN			
Input High Voltage, V_{INH}	2.1	V min	
Input Low Voltage, V_{INL}	0.6	V max	
Input Current, I_{IN}	±10	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
MODE INPUT			
Input High Voltage, V_{INH}	V_{DD} –0.2	V	
Input Low Voltage, V_{INL}	0.2	V	
Input Current, I_{IN}	±100	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
DB11–DB0, $\overline{BUSY}$			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
DB11–DB0			
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
CONVERSION			
Conversion Time	15	µs max	f_{CLKIN} = 2 MHz
Track/Hold Acquisition Time	5	µs max	
POWER REQUIREMENTS			
V_{DD}	+3.3	V nom	+3 V to +3.6 V for Specified Performance
I_{DD}			
Normal Power Mode @ +25°C	3	mA max	Typically 2 mA; MODE = V_{DD}
T_{MIN} to T_{MAX}	4	mA max	Typically 2.5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	400	µA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 250 µA
T_{MIN} to T_{MAX}	800	µA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 300 µA
Power Dissipation			
Normal Power Mode @ +25°C	11	mW max	V_{DD} = 3.6 V: Typically 8 mW; MODE = V_{DD}
T_{MIN} to T_{MAX}	15	mW max	V_{DD} = 3.6 V: Typically 9 mW; MODE = V_{DD}
Power Save Mode @ +25°C	1.5	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V
T_{MIN} to T_{MAX}	3	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V

NOTES
[1]Temperature range is as follows: B Versions, –40°C to +85°C.
[2]V_{IN} = 0 to V_{REF}.
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{SS} = +3 V to +3.6 V, V_{REF} = V_{DD}, AGND = DGND = 0 V)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (All Versions)	Units	Conditions/Comments
t_1	50	60	ns min	$\overline{CONVST}$ Pulse Width
t_2	200	200	ns max	$\overline{CONVST}$ to $\overline{BUSY}$ Falling Edge
t_3	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	0	0	ns min	$\overline{CS}$ to RD Hold Time
t_6	**110**	**150**	ns min	$\overline{RD}$ Pulse Width
t_7[2]	**100**	**140**	ns max	Data Access Time after $\overline{RD}$
t_8[3]	**5**	**5**	ns min	Bus Relinquish Time after $\overline{RD}$
	90	**90**	ns max	

NOTES

[1]Timing specifications in **bold** print are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_7 is measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_8 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

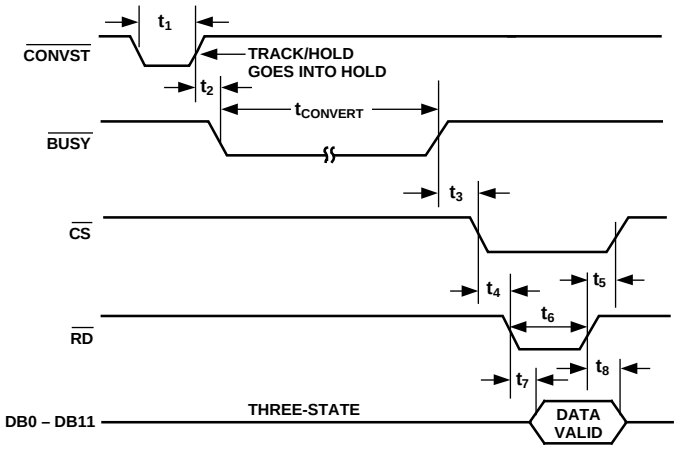


Figure 1. Timing Diagram

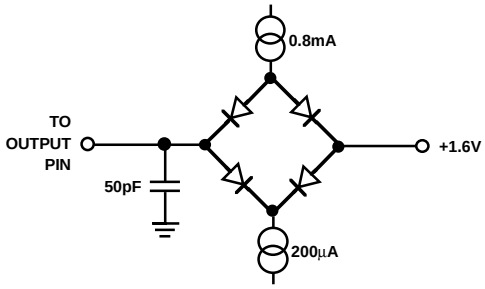


Figure 2. Load Circuit for Access and Relinquish Time

Table I. Truth Table

$\overline{CS}$	$\overline{CONVT}$	$\overline{RD}$	Function
1	1	X	Not Selected
1	↓	1	Start Conversion ↓
0	1	0	Enable ADC Data
0	1	1	Data Bus Three Stated

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7883BN	–40°C to +85°C	N-24
AD7883BR	–40°C to +85°C	R-24

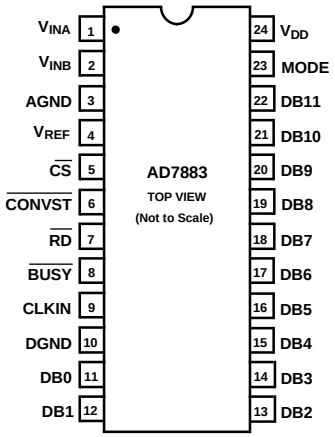
*N = Plastic DIP; R = SOIC (Small Outline Integrated Circuit).

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{INA}, V_{INB} to AGND (Figure 4) . . . . . –0.3 V to V_{DD} + 0.3 V
V_{INA} to AGND (Figure 5) . . . . . $-V_{DD}$ –0.3 V to V_{DD} + 0.3 V
V_{REF} to AGND . . . . . 0.3 V to V_{DD}
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Outputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7883 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	V_{INA}	Analog Input.
2	V_{INB}	Analog Input.
3	AGND	Analog Ground.
4	V_{REF}	Voltage Reference Input. This is normally tied to V_{DD}.
5	$\overline{CS}$	Chip Select. Active Low Logic input. The device is selected when this input is active.
6	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into hold mode and starts conversion. This input is asynchronous to the CLKIN and is independent of $\overline{CS}$ and $\overline{RD}$.
7	$\overline{RD}$	Read. Active Low Logic Input. This input is used in conjunction with $\overline{CS}$ low to enable data outputs.
8	$\overline{BUSY}$	Active Low Logic Output. This status line indicates converter status. $\overline{BUSY}$ is low during conversion.
9	CLKIN	Clock Input. TTL-compatible logic input. Used as the clock source for the A/D converter. The mark/space ratio of the clock can vary from 40/60 to 60/40.
10	DGND	Digital Ground.
11 . . . 22	DB0–DB11	Three-State Data Outputs. These become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
23	MODE	MODE Input. This input is used to put the device into the power save mode (MODE = 0 V). During normal operation, the MODE input will be a logic high (MODE = V_{DD}).
24	V_{DD}	Power Supply. This is nominally +3.3 V.

CIRCUIT INFORMATION

The AD7883 is a single supply 12-bit A/D converter. The part requires no external components apart from a 2 MHz external clock and power supply decoupling capacitors. It contains a 12-bit successive approximation ADC based on a fast-settling voltage output DAC, a high speed comparator and SAR, as well as the necessary control logic. The charge balancing comparator used in the AD7883 provides the user with an inherent track-and-hold function. The ADC is specified to work with sampling rates up to 50 kHz.

CONVERTER DETAILS

The AD7883 conversion cycle is initiated on the rising edge of the $\overline{\text{CONVST}}$ pulse, as shown in the timing diagram of Figure 1. The rising edge of the $\overline{\text{CONVST}}$ pulse places the track/hold amplifier into "HOLD" mode. The conversion cycle then takes between 26 and 28 clock periods. The maximum specified conversion time is 15 μs. During conversion the $\overline{\text{BUSY}}$ output will remain low, and the output databus drivers will be three-stated. When a conversion is completed, the $\overline{\text{BUSY}}$ output will go to a high level, and the result of the conversion can be read by bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low.

The track/hold amplifier acquires a 12-bit input signal in 5 μs. The overall throughput time for the AD7883 is equal to the conversion time plus the track/hold acquisition time. For a 2 MHz input clock the throughput time is 20 μs.

REFERENCE INPUT

For specified performance, it is recommended that the reference input be tied to V_{DD}. The part, however, will operate with a reference down to 2.5 V though with reduced performance specifications.

V_{REF} must not be allowed to go above V_{DD} by more than 100 mV.

ANALOG INPUT

The AD7883 has two analog input pins, V_{INA} and V_{INB}. Figure 3 shows the input circuitry to the ADC sampling comparator. The onboard attenuator network, made up of equal resistors, allows for various input ranges.

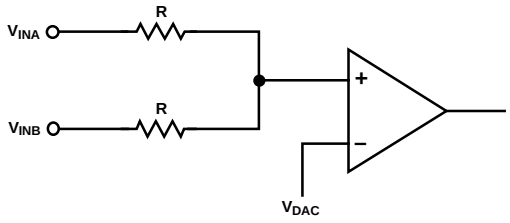


Figure 3. AD7883 Input Circuit

The AD7883 accommodates two separate input ranges, 0 to V_{REF} and $\pm V_{REF}$. The input configurations corresponding to these ranges are shown in Figures 4 and 5.

With $V_{REF} = V_{DD}$ and using a nominal V_{DD} of +3.3 V, the input ranges are 0 V to 3.3 V and ±3.3 V, as shown in Table II.

Table II. Analog Input Ranges

Analog Input Range	V_{REF}	Input Connections V_{INA}	Input Connections V_{INB}	Connection Diagram
0 V to +3.3 V	V_{DD}	V_{IN}	V_{IN}	Figure 4
±3.3 V	V_{DD}	V_{IN}	V_{REF}	Figure 5

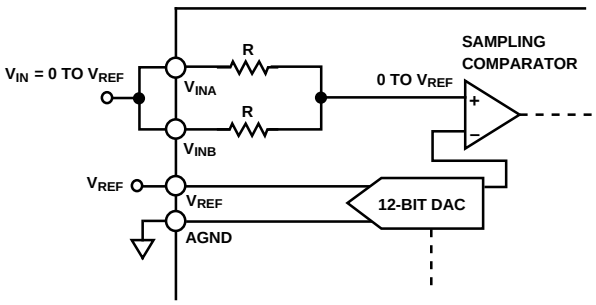


Figure 4. 0 to V_{REF} Unipolar Input Configuration

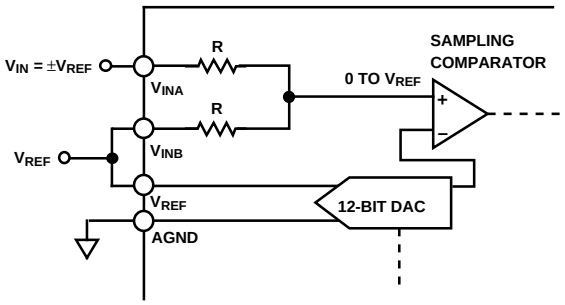


Figure 5. ±V_{REF} Bipolar Input Configuration

The AD7883 has one unipolar input range, 0 V to V_{REF}. Figure 4 shows the analog input for this range. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS –3/2 LSBs). The output code is straight binary with *1 LSB = FS/4096 = 3.3 V/4096 = 0.8 mV* when V_{REF} = 3.3 V. The ideal input/output transfer characteristic for the unipolar range is shown in Figure 6.

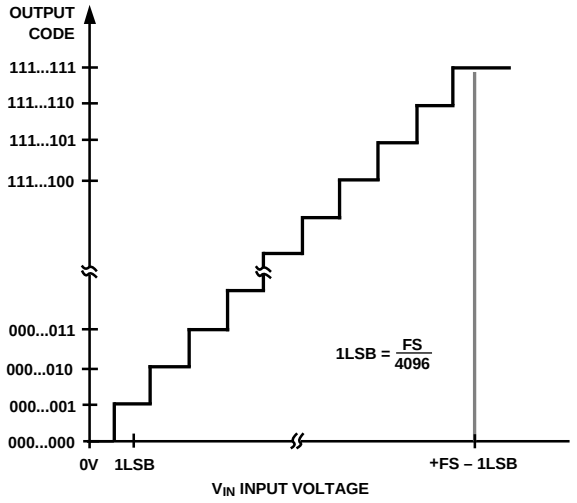


Figure 6. Unipolar Transfer Characteristics

Figure 5 shows the AD7883's $\pm V_{REF}$ bipolar analog input configuration. Once again the designed code transitions occur midway between successive integer LSB values. The output code is straight binary with *1 LSB = FS/4096 = 6.6 V/4096 = 1.6 mV*. The ideal bipolar input/output transfer characteristic is shown in Figure 7.

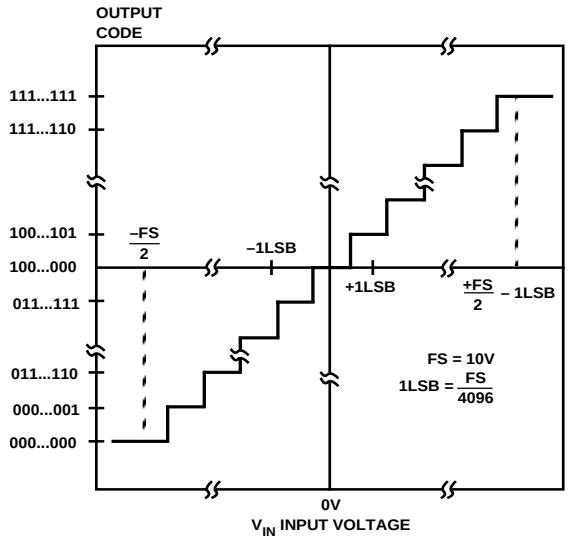


Figure 7. Bipolar Transfer Characteristic

CLOCK INPUT

The AD7883 is specified to operate with a 2 MHz clock connected to the CLKIN input pin. This pin may be driven directly by CMOS buffers. The mark/space ratio on the clock can vary from 40/60 to 60/40. As the clock frequency is slowed down, it can result in slightly degraded accuracy performance. This is due to leakage effects on the hold capacitor in the internal track-and-hold amplifier. Figure 8 is a typical plot of accuracy versus clock frequency for the ADC.

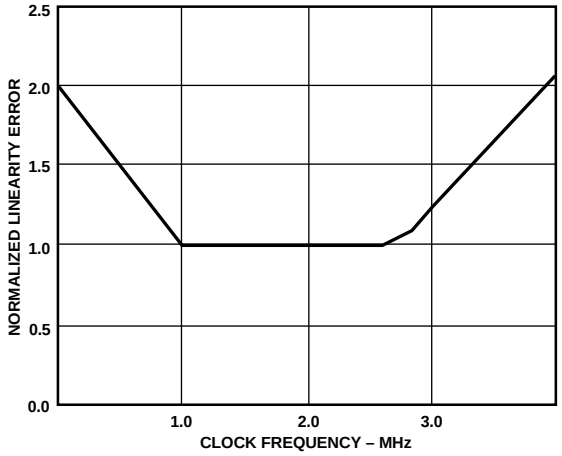


Figure 8. Normalized Linearity Error vs. Clock Frequency

TRACK/HOLD AMPLIFIER

The charge balanced comparator used in the AD7883 for the A/D conversion provides the user with an inherent track/hold function. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 5 μs. The overall throughput time is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2 MHz input clock, the throughput time is 20 μs.

The operation of the track/hold amplifier is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion, i.e., on the rising edge of $\overline{CONVST}$ as shown in Figure 1.

OFFSET AND FULL-SCALE ADJUSTMENT

In most Digital Signal Processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal range match the maximum possible dynamic range of the ADC. In such applications, offset and full-scale error will have to be adjusted to zero.

The following sections describe suggested offset and full-scale adjustment techniques which rely on adjusting the inherent offset of the op amp driving the input to the ADC as well as tweaking an additional external potentiometer as shown in Figure 9.

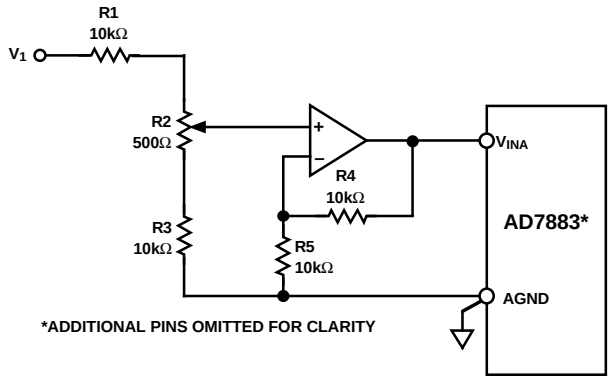


Figure 9. Offset and Full-Scale Adjust Circuit

Unipolar Adjustments

In the case of the 0 V to 3.3 V unipolar input configuration, unipolar offset error must be adjusted before full-scale error. Adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7883. This is done by applying an input voltage of 0.4 mV (1/2 LSB) to V_1 in Figure 9 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 3.2988 V (FS–3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Adjustments

Bipolar zero and full-scale errors for the bipolar input configuration of Figure 5 are adjusted in a similar fashion to the unipolar case. Again, bipolar zero error must be adjusted before full-scale error. Bipolar zero error adjustment is achieved by trimming the offset of the op amp driving the analog input of the AD7883 while the input voltage is 1/2 LSB below ground. This is done by applying an input voltage of –0.8 mV (1/2 LSB) to V_1 in Figure 9 and adjusting the op amp offset voltage until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 3.2988 V (FS/2–3/2 LSBs) is applied to V_1 and R2 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

DYNAMIC SPECIFICATIONS

The AD7883 is specified and tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7883 is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to noise ratio for a sine wave input is given by:

$$SNR = (6.02\ N + 1.76)\ dB \quad (1)$$

where N is the number of bits.

Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the V_{IN} input which is sampled at a 50 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 10 shows a typical 2048 point FFT plot of the AD7883 with an input signal of 2.5 kHz and a sampling frequency of 50 kHz. The SNR obtained from this graph is 71 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

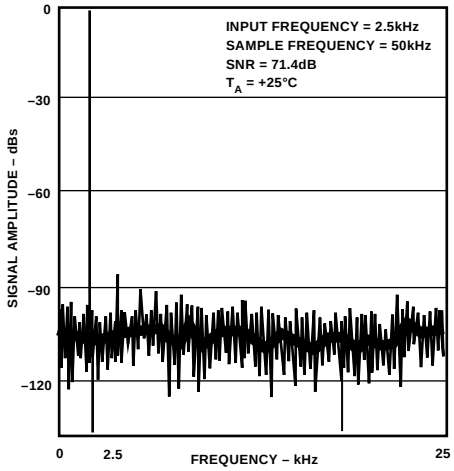


Figure 10. FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 11 shows a plot of effective number of bits versus input frequency for an AD7883 with a sampling frequency of 50 kHz. The effective number of bits typically remains better than 11.5 for frequencies up to 12 kHz.

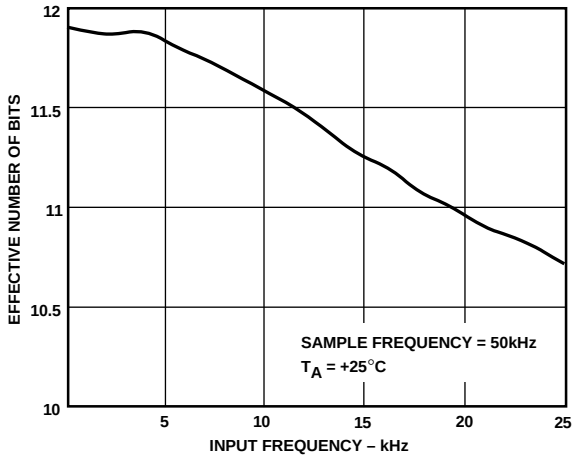


Figure 11. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7883, THD is defined as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \quad (3)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion, sine waves. Figure 12 shows a typical IMD plot for the AD7883.

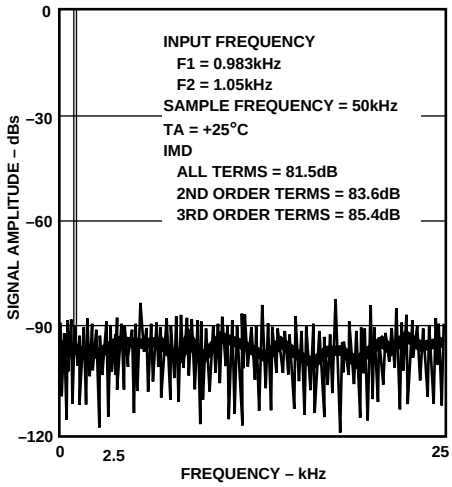


Figure 12. IMD Plot

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. The AD7883's comparator is required to make bit decisions on an LSB size of 0.8 mV. To achieve this, the designer must be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended, as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run digital tracks alongside analog signal tracks. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7883 AGND pin or as close as possible to the AD7883. Connect all other grounds and the AD7883 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

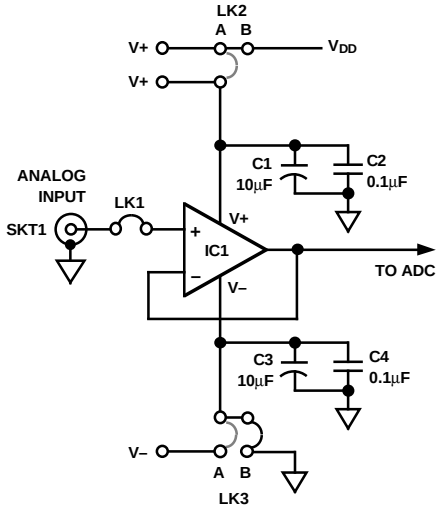


Figure 13. Analog Input Buffering

ANALOG INPUT BUFFERING

To achieve specified performance, it is recommended that the analog input (V_{INA}, V_{INB}) be driven from a low impedance source. This necessitates the use of an input buffer amplifier. The choice of op amp will be a function of the particular application and the desired analog input range.

The simplest configuration is the 0 V to V_{REF} range of Figure 4. A single supply op amp is recommended for such an implementation. This will allow for operation of the AD7883 in the 0 to V_{REF} unipolar range without supplying an external supply to V+ and V– of the op amp. Recommended single-supply op amps are the OP-195 and AD820.

In bipolar operation, positive and negative supplies must be connected to V+ and V– of the op amp.

The AD711 is a general purpose op amp which could be used to drive the analog input of the AD7883, in this input range.

POWER-DOWN CONTROL (MODE INPUT)

The AD7883 is designed for systems which need to have minimum power consumption. This includes such applications as hand held, portable battery powered systems and remote monitoring systems. As well as consuming minimum power under normal operating conditions, typically 8 mW, the AD7883 can be put into a power-down or sleep mode when not required to convert signals. When in this power-down mode, the AD7883 consumes 1 mW of power.

The AD7883 is powered down by bringing the MODE input pin to a Logic Low in conjunction with keeping the $\overline{RD}$ input control High. The AD7883 will remain in the power-down mode until MODE is brought to a Logic High again. The MODE input should be driven with CD4000 or HCMOS logic levels.

It is recommended that one "dummy" conversion be implemented before reading conversion data from the AD7883 after it has been in the powerdown mode. This is required to reset all internal logic and control circuitry. Allow one clock cycle before doing the dummy conversion. In a remote monitoring system where, say, 10 conversions are required to be taken with a sampling interval of 1 second, an additional 11th conversion must be carried out. Figure 14 gives a plot of power consumption as a function of time for such operation. The total conversion time for each cycle is 11×20 μs (where 20 μs is the time taken for a single conversion) corresponding to 2.2×10^{-4} secs.

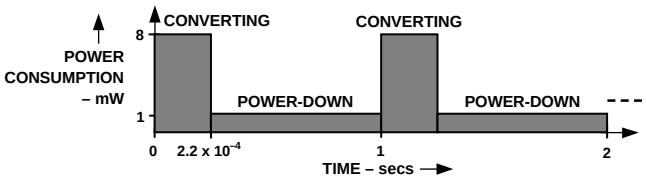


Figure 14. Power Consumption for Normal Operation and Power-Down Operation vs. Time

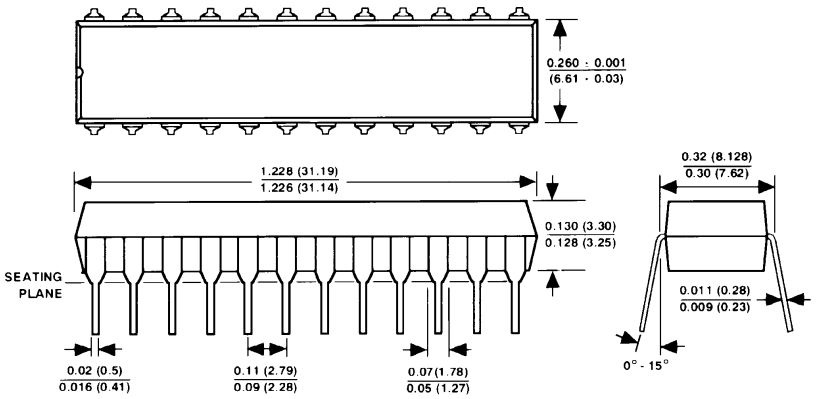
Hence:

$$\begin{aligned}\text{Average Power} &= \text{Power}_{\text{CONVERTING}} + \text{Power}_{\text{POWER-DOWN}}\\ &= \{8\text{ mW} \times (2.2 \times 10^{-4})\}\\ &+ \{1\text{ mW} \times (0.9998)\}\\ &= 1.0015\text{ mW}\end{aligned}$$

OUTLINE DIMENSIONS

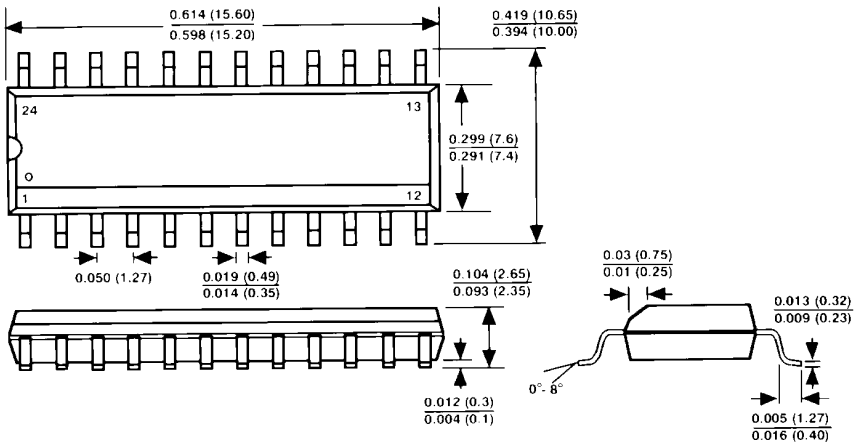
Dimensions shown in inches and (mm).

24-Lead Plastic DIP (N-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-385 10 REQUIREMENTS.

24-Lead SOIC (R-24)



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