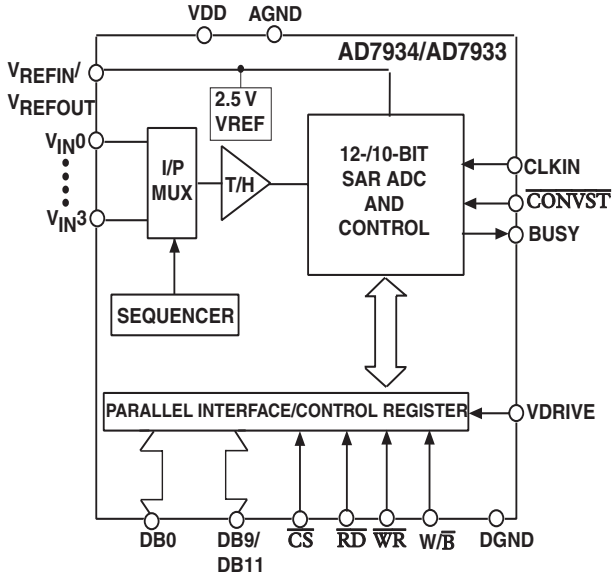
4-Channel, 1.5 MSPS, 12- & 10-Bit Parallel ADCs with a Sequencer

AD7934/AD7933

FEATURES

Fast Throughput Rate: 1.5 MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power:
8 mW max at 1.5 MSPS with 3V Supplies
16 mW max at 1.5 MSPS with 5V Supplies
4 Analog Input Channels with a Sequencer
Software Configurable Analog Inputs:
4-Channel Single Ended Inputs
2-Channel Fully Differential Inputs
2-Channel Pseudo Differential Inputs
Accurate On-chip 2.5 V Reference
Wide Input Bandwidth:
70dB SNR at 50kHz Input Frequency
No Pipeline Delays
High Speed Parallel Interface - Word/Byte Modes
Full Shutdown Mode: 1μA max
28-Pin TSSOP Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7934/AD7933 are 12- & 10-bit, high speed, low power, successive approximation (SAR) ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS. The parts contain a low noise, wide bandwidth, differential track/hold amplifier that can handle input frequencies up to 20MHz.

The AD7934/AD7933 feature 4 analog input channels with a channel sequencer to allow a pre-programmed selection of channels to be converted sequentially. These parts can operate with either Single-ended, Fully Differential or Pseudo Differential analog inputs. The analog input configuration is chosen by setting the relevant bits in the on-chip Control Register.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to Microprocessors and Dsps. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and the conversion is also initiated at this point.

The AD7934/AD7933 has an accurate on-chip 2.5 V reference that can be used as the reference source for the analog to digital conversion. Alternatively, this pin can be overdriven to provide an external reference in the range 100mV to 3.5 V.

These parts use advanced design techniques to achieve very low power dissipation at high throughput rates. They also feature flexible power management options.

An on-chip Control register allows the user to set up different operating conditions including analog input range and configuration, output coding, power management and channel sequencing.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption
   The AD7934/AD7933 offer 1.5 MSPS throughput with 8mW power consumption at V_{DD} = 3V.
2. Four Analog Inputs with a Channel Sequencer.
   A consecutive sequence of input channels can be selected, through which the AD7934/AD7933 will continuously cycle and convert on.
3. Accurate on-chip 2.5 V reference.
4. Software Configurable Analog Inputs
   Single-Ended, Pseudo Differential or Fully Differential analog inputs that are software selectable.
5. Single-supply Operation with V_{DRIVE} Function.
   The AD7934/AD7933 operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the parallel interface to connect directly to either 3V or 5 V proces sor systems independent of V_{DD}.
6. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106,U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD7934–SPECIFICATIONS[1]

(V_{DD} = V_{DRIVE}=2.7 V to 5.25V, V_{REFIN}/V_{REFOUT} = 2.5V unless otherwise noted, F_{CLKIN} = 20MHz, F_{SAMPLE} = 1.5 MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	BVersion[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} =50kHz Sine Wave
Signal to Noise + Distortion [2] (SINAD)	70	dB min	
Signal to Noise Ratio (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	-75	dB max	-80dB typ
Peak Harmonic or Spurious Noise (SFDR)[2]	-75	dB max	-82dB typ
Intermodulation Distortion (IMD)[2]			fa = 40.1kHz, fb = 51.5kHz
Second Order Terms	-85	dB typ	
Third Order Terms	-85	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	-82	dB typ	
Full Power Bandwidth	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[2]	±1	LSB max	
Differential Nonlinearity[2]	±0.95	LSB max	Guaranteed No Missed Codes to 12 Bits.
Total Unadjusted Error	TBD	LSB max	
0V to $V_{REF\ IN}$ Input Range[3]			Straight Binary Output Coding
Offset Error	±3	LSB max	
Offset Error Match	±0.5	LSB max	
Gain Error	±2	LSB max	
Gain Error Match	±0.6	LSB max	
0V to 2 x $V_{REF\ IN}$ Input Range[4]			-$V_{REF\ IN}$ to +$V_{REF\ IN}$ Biased about V_{REF} with Twos Complement Output Coding
Positive Gain Error	±2	LSB max	
Positive Gain Error Match	±0.6	LSB max	
Zero Code Error	±3	LSB max	
Zero Code Error Match	±1	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	V	RANGE bit in the Control register set to 1.
	0 to 2xV_{REF}	V	RANGE bit in the Control register set to 0. V_{DD}/V_{DRIVE} = 4.75 V to 5.25 V for 0-2V_{REF} range
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REFIN} Input Voltage	2.5[5]	V	±1% Specified Performance
DC Leakage Current	±1	µA max	
V_{REFOUT} Output Voltage	2.49/2.51	Vmin/max	
V_{REFOUT} Tempco	15	ppm/°C typ	
V_{REF} Output Impedance	10	Ω	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7xV_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3xV_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[6]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[6]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit in the control register set to 1.
	2s Complement		CODING bit in the control register set to 0.

AD7934–SPECIFICATIONS[1]

Parameter	B Version[1]	Units	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	12	CLKIN cycles (max)	
Track/Hold Acquisition Time	300	ns max	Sine Wave Input
	325	ns max	Full-Scale Step Input
Throughput Rate	1.5	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}			Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	0.5	mA typ	V_{DD} = 2.7V to 5.25V.
Normal Mode (Operational)	3.2	mA max	V_{DD} = 4.75V to 5.25V.
	2.6	mA max	V_{DD} = 2.7V to 3.6V.
Auto StandBy Mode	1.55	mA typ	
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	
	1	µA max	(Static)
Full Shut-Down Mode	1	µA max	SCLK On or Off.
Power Dissipation			
Normal Mode (Operational)	16	mW max	V_{DD} = 5V.
	8	mW max	V_{DD} = 3V.
Auto Standby-Mode (Static)	450	µW max	V_{DD} = 5V.
	270	µW max	V_{DD} = 3V.
Auto Shutdown-Mode (Static)	5	µW max	V_{DD} = 5V.
	3	µW max	V_{DD} = 3V.
Full Shutdown-Mode	5	µW max	V_{DD} = 5V.
	3	µW max	V_{DD} = 3V.

NOTES

[1]Temperature ranges as follows: B Versions: –40°C to +85°C.

[2]See Terminology Section.

[3]Bit 9 in the Control register set to 1

[4]Bit 9 in the Control register set to 0

[5]This device is operational with an external reference in the range 0.1 V to 3.5 V.

[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

AD7933–SPECIFICATIONS[1]

(V_{DD} = V_{DRIVE}=2.7 V to 5.25V, V_{REFIN}/V_{REFOUT} = 2.5V unless otherwise noted, F_{CLKIN} = 20MHz, F_{SAMPLE} = 1.5MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} =50kHz Sine Wave
Signal to Noise + Distortion [2] (SINAD)	60	dB min	
Signal to Noise Ratio (SNR)[2]	60	dB min	
Total Harmonic Distortion (THD)[2]	-73	dB max	
Peak Harmonic or Spurious Noise[2] (SFDR)	-73	dB max	
Intermodulation Distortion (IMD)[2]			fa = 40.1kHz, fb = 51.5kHz
Second Order Terms	-75	dB typ	
Third Order Terms	-75	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	-82	dB typ	
Full Power Bandwidth	20	MHz typ	@ 3 dB
	2.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[2]	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	Guaranteed No Missed Codes to 10 Bits.
Total Unadjusted Error	TBD	LSB max	
0V to $V_{REF\ IN}$ Input Range[3]			Straight Binary Output Coding
Offset Error	±3	LSB max	
Offset Error Match	±0.5	LSB max	
Gain Error	±2	LSB max	
Gain Error Match	±0.6	LSB max	
0V to 2 x $V_{REF\ IN}$ Input Range[4]			-$V_{REF\ IN}$ to +$V_{REF\ IN}$ Biased about V_{REF} with Twos Complement Output CodingOffset
Positive Gain Error	±2	LSB max	
Positive Gain Error Match	±0.6	LSB max	
Zero Code Error	±3	LSB max	
Zero Code Error Match	±1	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	V	RANGE bit in the Control register set to 1.
	0 to 2xV_{REF}	V	RANGE bit in the Control register set to 0. V_{DD}/V_{DRIVE} = 4.75 V to 5.25 V for 0-2V_{REF} range
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT/OUTPUT			
V_{REFIN} Input Voltage	2.5[5]	V	±1% Specified Performance
DC Leakage Current	±1	µA max	
V_{REFOUT} Output Voltage	2.49/2.51	Vmin/max	
V_{REFOUT} Tempco	15	ppm/°C typ	
V_{REF} Output Impedance	10	Ω	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7xV_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3xV_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[6]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[6]	10	pF max	
Output Coding	Straight (Natural) Binary		CODING bit in the control register set to 1.
	2s Complement		CODING bit in the control register set to 0.

AD7933–SPECIFICATIONS[1]

Parameter	B Version[1]	Units	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	12	CLKIN cycles (max)	
Track/Hold Acquisition Time	300	ns max	Sine Wave Input
	325	ns max	Full-Scale Step Input
Throughput Rate	1.5	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}			Digital I/Ps = 0V or V_{DRIVE}.
Normal Mode(Static)	0.5	mA typ	V_{DD} = 2.7V to 5.25V.
Normal Mode (Operational)	3.2	mA max	V_{DD} = 4.75V to 5.25V.
	2.6	mA max	V_{DD} = 2.7V to 3.6V.
Auto StandBy Mode	1.55	mA typ	
	90	µA max	(Static)
Auto Shutdown Mode	1	mA typ	
	1	µA max	(Static)
Full Shut-Down Mode	1	µA max	SCLK On or Off.
Power Dissipation			
Normal Mode (Operational)	16	mW max	V_{DD} = 5V.
	8	mW max	V_{DD} = 3V.
Auto Standby-Mode (Static)	450	µW max	V_{DD} = 5V.
	270	µW max	V_{DD} = 3V.
Auto Shutdown-Mode (Static)	5	µW max	V_{DD} = 5V.
	3	µW max	V_{DD} = 3V.
Full Shutdown-Mode	5	µW max	V_{DD} = 5V.
	3	µW max	V_{DD} = 3V.

NOTES
[1]Temperature ranges as follows: B Versions: –40°C to +85°C.
[2]See Terminology Section
[3]Bit 9 in the Control register set to 1
[4]Bit 9 in the Control register set to 0
[5]This device is operational with an external reference in the range 0.1 V to 3.5 V.
[6]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

AD7934/AD7933

TIMING SPECIFICATIONS[1,2,3]

(V_{DD} = V_{DRIVE}=2.7 V to 5.25V, V_{REFIN}/V_{REFOUT} = 2.5V unless otherwise noted, F_{CLKIN} = 20MHz, F_{SAMPLE} = 1.5MSPS; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7934	AD7933	Units	Description
f_{CLKIN} [4]	10	10	kHz min	
	20	20	MHz max	
t_{quiet}	100	100	ns min	Minimum time between conversions
$t_{convert}$	TBD	TBD	ns max	Conversion Time
t_1	100	100	ns min	$\overline{CONVST}$ pulsewidth
t_2	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_3	0	0	ns max	$\overline{CS}$ to $\overline{WR}$ hold time
t_4	55	55	ns min	$\overline{WR}$ Pulse Width
t_5	10	10	ns min	Data Setup time before $\overline{WR}$
t_6	5	5	ns min	Data Hold after $\overline{WR}$
t_7	1/2 t_{CLKIN}	1/2 t_{CLKIN}	ns min	New data valid before falling edge of BUSY
t_8	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_9	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ hold time
t_{10}	55	55	ns min	$\overline{RD}$ Pulse Width
t_{11} [5]	50	50	ns max	Data access time after $\overline{RD}$
t_{12} [6]	5	5	ns min	Bus relinquish time after $\overline{RD}$
	40	40	ns max	Bus relinquish time after $\overline{RD}$
t_{13}	15	15	ns min	HBEN to $\overline{RD}$ setup time
t_{14}	5	5	ns min	HBEN to $\overline{RD}$ hold time
t_{15}	60	60	ns min/max	Minimum time between Reads
t_{16}	0	0	ns min	HBEN to $\overline{WR}$ setup time
t_{17}	5	5	ns max	HBEN to $\overline{RD}$ setup time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.

[2]See Figure 1, Figure 20 and Figure 21.

[3]All timing specifications given above are with a 25pF load capacitance.

[4]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[5]The time required for the output to cross 0.4 V or 0.7 x V_{DRIVE} V.

[6]t_{12} is derived form the measured time taken by the data outputs to change 0.5 V. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_{12} quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

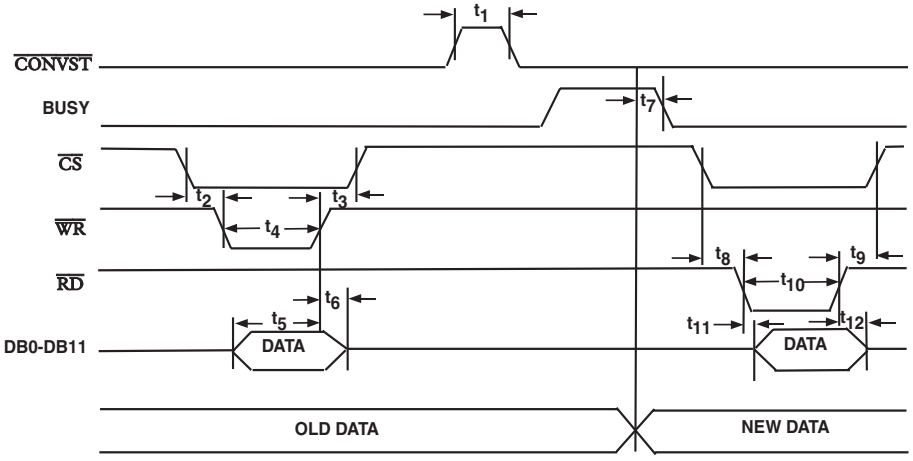


Figure 1. AD7934/AD7933 Parallel Interface

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND/DGND .....–0.3 V to 7 V
V_{DRIVE} to AGND/DGND .....–0.3 V to 7 V
Analog Input Voltage to AGND . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND .....–0.3 V to 7 V
V_{DRIVE} to V_{DD} ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to AGND –0.3 V to V_{DD} + 0.3 V
REF_{IN} to AGND .....–0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] .... ±10 mA
Operating Temperature Range
  Commercial (B Version) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
θ_{JA} Thermal Impedance ..... 97.9°C/W (TSSOP)
θ_{JC} Thermal Impedance ..... 14°C/W (TSSOP)
  Lead Temperature, Soldering
    Vapor Phase (60 secs) ..... +215°C
    Infared (15 secs) ..... +220°C
ESD ..... 1 kV

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Linearity Error (LSB)[1]	Package Option	Package Descriptions
AD7934	-40°C to +85°C	±1	RU-28	TSSOP
AD7933	-40°C to +85°C	±1	RU-28	TSSOP
EVAL-ADxxxxCB[2]	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

NOTES

[1]Linearity error here refers to integral linearity error.

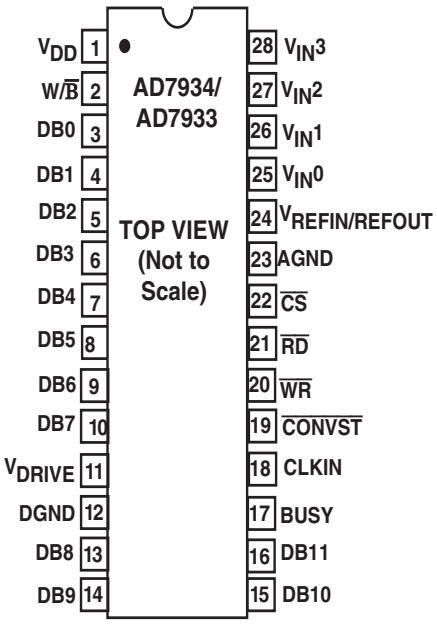
[2]This can be used as a stand-alone evaluation board or in conjunction with the Evaluation Board Controller for evaluation/demonstration purposes.

[3]Evaluation Board Controller. This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. The following needs to be ordered to obtain a complete evaluation kit: the ADC Evaluation Board (EVAL-ADxxxxCB), the EVAL-CONTROL BRD2 and a 12 V ac transformer. See the ADxxxx evaluation board technical note for more details.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7934/AD7933 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION TSSOP



PIN FUNCTION DESCRIPTION

Pin no.	Pin Mnemonic	Function
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7934/AD7933 is from +2.7V to +5.25V. The supply should be decoupled to AGND with a 0.1µF capacitor and a 10µF tantalum capacitor.
2	W/$\overline{B}$	Word/Byte Input. When this input is logic high, data is transferred to and from the AD7934/AD7933 in 12/10-bit words on pins DB0 to DB11/9. When this pin is logic low, byte transfer mode is enabled. Data and the channel ID is transferred on pins DB0 to DB7 and pin DB8/HBEN assumes its HBEN functionality.
3-10	DB0 to DB7	Data Bits 0 to 7. Three state parallel digital I/O pins that provide the conversion result and also allow the Control and Shadow registers to be programmed. These pins are controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. The logic high voltage level for these pins is determined by the V_{DRIVE} input.
11	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the parallel interface of the AD7934/AD7933 will operate.
12	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7934/AD7933. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
13	DB8/HBEN	Data Bit 8/High Byte Enable. When W/$\overline{B}$ is high, this pin acts as Data Bit 8, a three state I/O pin that is controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. When W/$\overline{B}$ is low, this pin acts as the high byte enable pin. When HBEN is low, the low byte of data being written to or read from the AD7934/AD7933 is on DB0 to DB7. When reading from the AD7933, the two LSBs in the low byte are zeros, followed by 6 bits of conversion data. When HBEN is high, the top 4 bits of the data being written to or read from the AD7934/AD7933 are on DB0 to DB3. When reading from the device, DB4 & DB5 of the high byte will contain the ID of the channel for which the conversion result corresponds.
14-16	DB9 to DB11	Data Bits 9 to 11. Three state parallel digital I/O pins that provide the conversion result and also allow the status and sequencer registers to be programmed. These pins are controlled by $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$. The logic high voltage level for these pins is determined by the V_{DRIVE} input. DB10 and DB11 are only used as inputs for the AD7933 10-bit ADC.

PIN FUNCTION DESCRIPTION

Pin no.	Pin Mnemonic	Function
17	BUSY	Busy Output. Logic output indicating the status of the conversion. The BUSY output goes high following the falling edge of $\overline{\text{CONVST}}$ and stays high for the duration of the conversion. Once the conversion is complete and the result is available in the output register, the BUSY output will go low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low.
18	CLKIN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7934 takes 12 clock cycles while conversion time for the AD7933 takes 10 clock cycles. The frequency of the master clock input therefore determines the conversion time and achievable throughput rate.
19	$\overline{\text{CONVST}}$	Conversion Start Input. Following power down, when operating in Auto-shutdown or Auto STBY modes, a rising edge on $\overline{\text{CONVST}}$ is used to power up the device. A falling edge on $\overline{\text{CONVST}}$ is used to initiate a conversion. The track/hold goes from track to hold mode on the falling edge of $\overline{\text{CONVST}}$ and the conversion process is initiated at this point.
20	$\overline{\text{WR}}$	Write Input. Active low logic input used in conjunction with $\overline{\text{CS}}$ to write data to the internal registers.
21	$\overline{\text{RD}}$	Read Input. Active low logic input used in conjunction with $\overline{\text{CS}}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
22	$\overline{\text{CS}}$	Chip Select. Active low logic input used in conjunction with $\overline{\text{RD}}$ and $\overline{\text{WR}}$ to Read conversion data or to Write data to the internal registers. When reading, data is placed on to the data bus following the falling edge of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$.
23	AGND	Analog Ground. This is the ground reference point for all analog circuitry on the AD7934/ AD7933. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
24	V_{REFIN}/V_{REFOUT}	Reference Input/Output. This pin is connected to the internal reference and is the reference source for the ADC. The nominal internal reference voltage is 2.5 V and this appears at this pin. This pin can be overdriven by an external reference. The input voltage range for the external reference is 0.1 V to 3.5 V.
25-28	$V_{IN}0$ - $V_{IN}3$	Analog Input 0 to Analog Input 3. Four analog input channels that are multiplexed into the on-chip track/hold. The analog inputs can be programmed to be four single ended inputs, two fully differential pairs or two pseudo differential pairs by setting the MODE bits in the Control register appropriately (see Table III). The analog input channel to be converted can either be selected by writing to the Address bits (ADD1 & ADD0) in the control register prior to the conversion, or the on-chip sequencer can be used. The address bits in conjunction with the SEQ0 and SEQ1 bits in the Control register allow the Sequencer to be programmed. The input range for all input channels can either be 0V to V_{REF} or 0V to 2 x V_{REF} and the coding can be binary or two's complement, depending on the states of the RANGE and CODING bits in the Control register. Any unsed input channels should be connected to AGND to avoid noise pickup.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1 LSB

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REFIN} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain error between any two channels.

Zero Code Error
This applies when using the 2's complement output coding option, in particular to the 2 x V_{REFIN} input range with -V_{REFIN} to +V_{REFIN} biased about the V_{REFIN} point. It is the deviation of the mid scale transition (all 0s to all 1s) from the ideal V_{IN} voltage, i.e. V_{REFIN} - 1 LSB.

Zero Code Error Match
This is the difference in Zero Code Error between any two channels.

Positive Gain Error
This applies when using the 2's complement output coding option, in particular to the 2 x V_{REFIN} input range with -V_{REFIN} to +V_{REFIN} biased about the V_{REFIN} point. It is the deviation of the last code transition (011. . .110) to (011 . . . 111) from the ideal (i.e., +V_{REFIN} - 1 LSB) after the Zero Code Error has been adjusted out.

Positive Gain Error Match
This is the difference in Positive Gain Error between any two channels.

Negative Gain Error
This applies when using the 2's complement output coding option, in particular to the 2 x V_{REFIN} input range with -V_{REFIN} to +V_{REFIN} biased about the V_{REFIN} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (i.e., -REF $_{IN}$ + 1 LSB) after the Zero Code Error has been adjusted out.

Negative Gain Error Match
This is the difference in Negative Gain Error between any two channels.

Channel-to-Channel Isolation
Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a fullscale 390 kHz sine wave signal to all 7 nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure is given worse case across all 8 channels for the AD7934/AD7933.

PSR (Power Supply Rejection)
Varations in power supply will affect the full scale transition, but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power-supply voltage from the nominal value. See Typical PerformancePlots.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode and the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\,N + 1.76)\,dB$$

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter, this is 61.96dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7934/AD7933, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

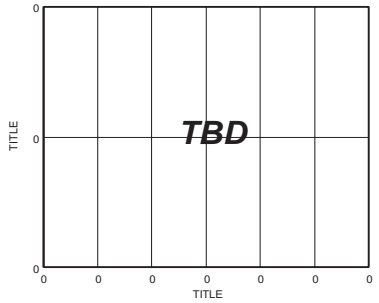
where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak

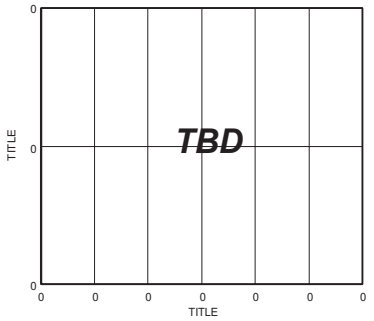
Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7934/AD7933 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

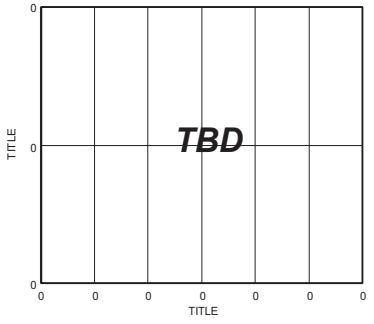
TYPICAL PERFORMANCE CHARACTERISTICS



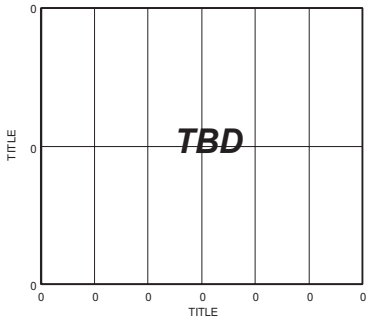
TPC1 PSRR versus Supply ripple Frequencywith supply decoupling



TPC2 PSRR versus Supply ripple Frequencywithout supply decoupling

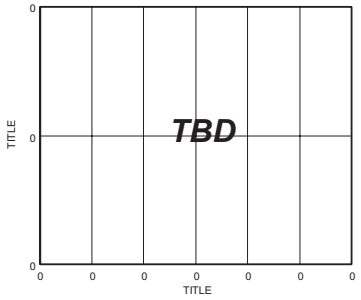


TPC3 Internal V_{REF} Error vs Temperature

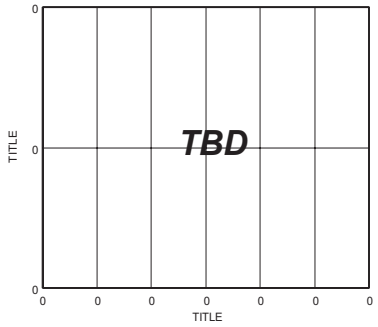


TPC4 V_{REF}out vs Rsource

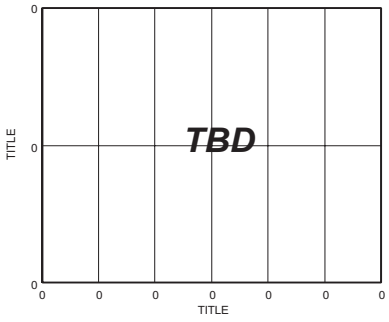
AD7934 Performance Curves



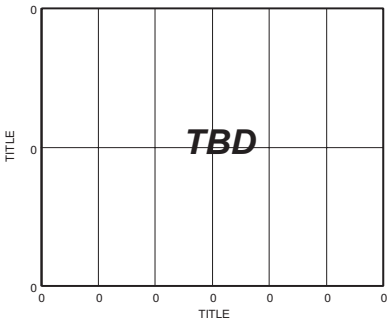
TPC5. SINAD vs Analog Input Frequency for various Supply Voltages



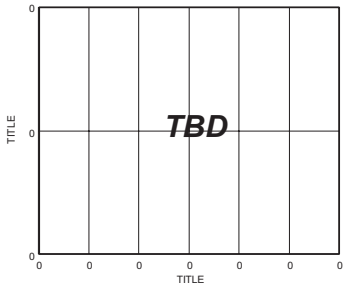
TPC6. FFT @ V_{DD} = 5V



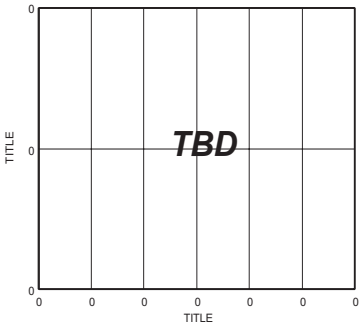
TPC7. Typical DNL @ V_{DD} = 5V



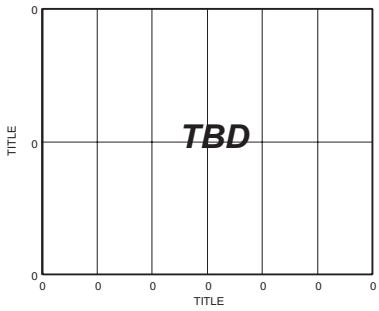
TPC8. Typical INL @ V_{DD} = 5V



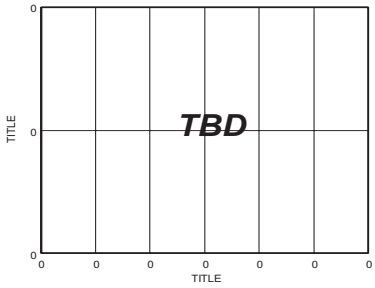
TPC9. Change in INL vs V_{REF} for V_{DD} = 5V



TPC10. Change in DNL vs V_{REF} for VDD = 5V

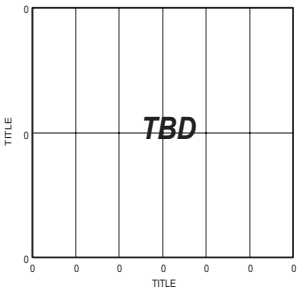


TPC11. Change in ENOB vs V_{REF} for VDD = 5V

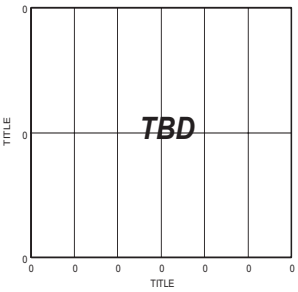


TPC12. Offset vs V_{REF}

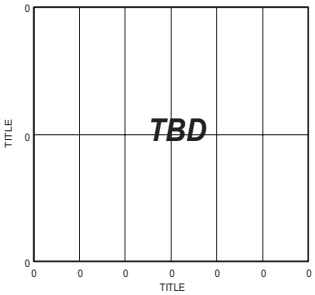
AD7933 Performance Curves



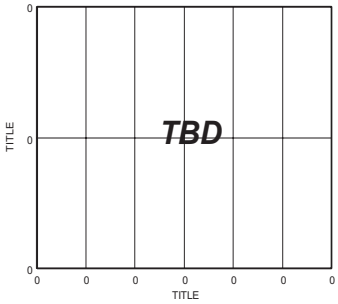
TPC13. Histogram of codes @ VDD = 5v



TPC13. FFT @ V_{DD} = 5V



TPC 14. Typical DNL @ V_{DD} = 5V



TPC 15. Typcial INL @ V_{DD} = 5V

CONTROL REGISTER

The Control Register on the AD7934/AD7933 is a 12-bit, write-only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins. The Control Register is shown below and the functions of the bits are described in Table I.

MSB											LSB
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PM1	PM0	CODING	REF	ZERO	ADD1	ADD0	MODE1	MODE0	SEQ0	SEQ1	RANGE

Table I. Control Register Bit Function Description

Bit	Mnemonic	Comment
11, 10	PM1 PM0	Power Management Bits. These two bits are used to select the power mode of operation. The user can choose between either normal mode or various power down modes of operation as shown in Table II.
9	CODING	This bit selects the output coding of the conversion result. If this bit is set to 0, the output coding will be 2s complement. If this bit is set to 1, the output coding will be straight binary.
8	REF	This bit selects whether the internal or an external reference is used to perform the conversion. If this bit is logic 0, the internal reference is selected and if it is 1, an external reference should be applied (see the Reference Section).
7	ZERO	This bit is not used and should always be set to logic 0.
6, 5	ADD1, ADD0	These two address bits are used to either select which analog input channel is to be converted on in the next conversion if the sequencer is not being used, or to select the final channel in a consecutive sequence when the sequencer is being used as described in Table IV. The selected input channel is decoded as shown in Table III.
4,3	MODE1, MODE0	The two Mode pins select the type of analog input on the V_{IN} pins. The AD7934/AD7933 can have either 4 Single Ended inputs, 2 Fully Differential inputs or 2 pseudo differential inputs. See Table III.
2	SEQ0	The SEQ0 bit in the control register is used in conjunction with the SEQ1 bit to control the use of the sequencer function. See Table IV.
1	SEQ1	The SEQ1 bit in the control register is used in conjunction with the SEQ0 bit to control the use of the sequencer function. See Table IV.
0	RANGE	This bit selects the analog input range of the AD7934/AD7933. If it is set to 0 then the analog input range will extend from 0V to V_{REF}. If it is set to 1 then the analog input range will extend from 0V to $2xV_{REF}$. When this range is selected, AV_{DD} must be 4.75 V to 5.25 V.

Table II. Power Mode Selection using the Power Management Bits in the Control Register

PM1	PM2	Mode	Description
1	1	Normal Mode	When operating in normal mode, all circuitry is fully powerered up at all times.
1	0	Full Shutdown	When the AD7934/AD7933 enters this mode, all circuitry is powered down. The information in the Control Register is retained.
0	1	Auto Shutdown	When operating in Auto Shutdown mode, the AD7934/AD7933 will enter Full Shut down mode at the end of each conversion. In this mode, all circuitry is powered down.
0	0	Auto Standby	When the AD7934/AD7933 enter this mode, all circuitry is powered down excluding the internal reference. This mode is similar to Auto Shutdown but allows the part to power up in 1µsec.

Table III. Analog Input Type Selection

Channel Address		MODE0=0, MODE1=0		MODE0=0, MODE1=1		MODE0=1, MODE1=0		MODE0=1, MODE1=1
		4 Single-Ended I/P Channels		4 Fully Differential I/P Channels		4 Pseudo Differential I/P Channels		Not Used
ADD1	ADD0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	
0	0	VIN0	AGND	VIN0	VIN1	VIN0	VIN1	
0	1	VIN1	AGND	VIN1	VIN0	VIN1	VIN0	
1	0	VIN2	AGND	VIN2	VIN3	VIN2	VIN3	
1	1	VIN3	AGND	VIN3	VIN2	VIN3	VIN2	

SEQUENCER OPERATION

The configuration of the SEQ1 and SEQ0 bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table IV outlines the three modes of operation of the Sequencer.

Table IV. Sequence Selection

SEQ1	SEQ0	Sequence Type
0	0	This configuration is selected when the sequence function is not used. The analog input channel selected on each individual conversion is determined by the contents of the channel address bits ADD1 & ADD0 in each prior write operation. This mode of operation reflects the normal operation of a multi-channel ADC, without the Sequencer function being used, where each write to the AD7934/AD7933 selects the next channel for conversion.
0	1	Not Used
1	0	If the SEQ1 and SEQ0 bits are set in this way then the sequence function will not be interrupted upon completion of the WRITE operation. This allows other bits in the Control Register to be altered between conversions while in a sequence without terminating the cycle.
1	1	This configuration is used in conjunction with the Channel Address bits (ADD1 & ADD0) to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the Channel Address bits in the Control Register.

CIRCUIT INFORMATION

The AD7934/AD7933 are fast, 4 channel, 12-&10-bit, single supply, Analog to Digital converters. The parts can be operated from a either a 2.7 V to 3.6 V or a 4.75 V to 5.25 V power supply and feature throughput rates up to 1.5MSPS.

The AD7934/AD7933 provide the user with an on-chip track/hold, an internal accurate reference, an analog to digital converter, and a parallel interface housed in a 28-lead TSSOP package.

The AD7934/AD7933 have four analog input channels which can be configured to be four single ended inputs, two fully differential pairs or two pseudo differential pairs. There is an on-chip channel sequencer which allows the user to select a channel sequence through which the ADC can cycle with each consecutive falling edge of $\overline{CS}$.

The analog input range for the AD7934/AD7933 is 0 to V_{REF} or 0 to 2 x V_{REF} depending on the status of the RANGE bit in the Control register. For the 0 to 2 x V_{REF} range the part must be operated from a 4.75 V to 5.25 V supply.

The AD7934/AD7933 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the Control Register.

CONVERTER OPERATION

The AD7934/AD7933 is a successive approximation ADC based around two capacitive DACs. Figures 2 and 3 show simplified schematics of the ADC in Acquisition and Conversion phase respectively. The ADC comprises of Control Logic, a SAR and two capacitive DACs. Figure 2 shows the operation of the ADC in Differential/Pseudo Differential Mode. Single Ended mode operation is similar but V_{IN-} is internally tied to AGND. In acquisition phase, SW3 is closed and SW1 and SW2 are in position A, the comparator is held in a balanced condition and the sampling capacitor arrays acquire the differential signal on the input.

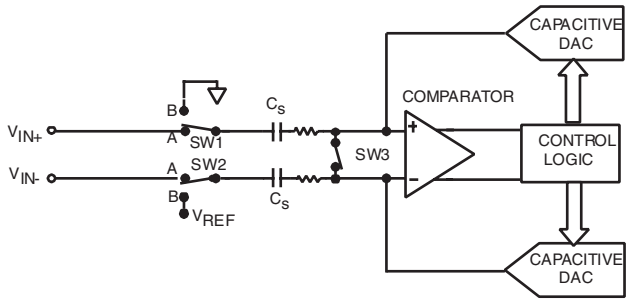


Figure 2. ADC Acquisition Phase

When the ADC starts a conversion (figure 3), SW3 will open and SW1 and SW2 will move to position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The Control Logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC's output code. The output impedances of the sources driving the V_{IN+} and the V_{IN-} pins must be matched otherwise the two inputs will have different settling times, resulting in errors.

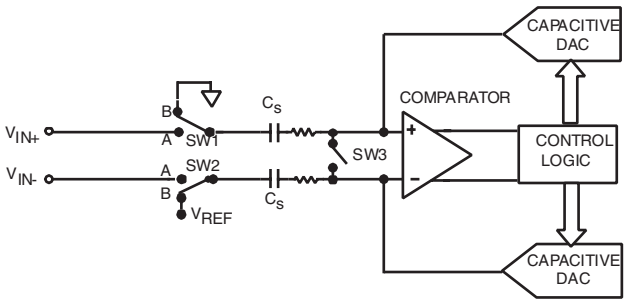


Figure 3. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding for the AD7934/AD7933 is either straight binary or two's complement, depending on the status of the CODING bit in the control register. The designed code transitions occur at successive LSB values (i.e. 1LSB, 2LSBs, etc.) and the LSB size is V_{REF}/4096 for the AD7934 and V_{REF}/1024 for the AD7933. The ideal transfer characteristics of the AD7934/AD7933 for both straight binary and twos complement output coding are shown in Figures 4 and 5 respectively.

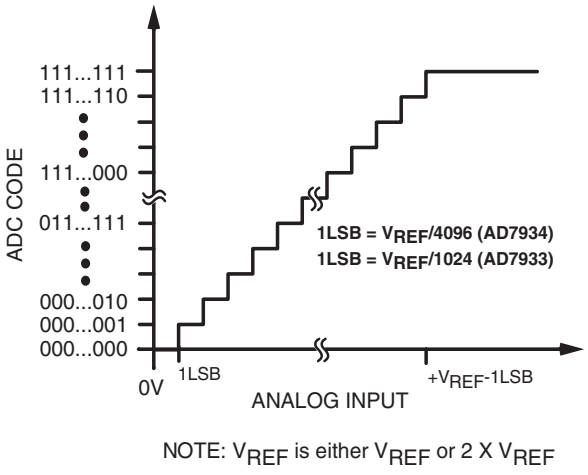


Figure 4. AD7934/AD7933 Ideal Transfer Characteristic with Straight Binary Output Coding

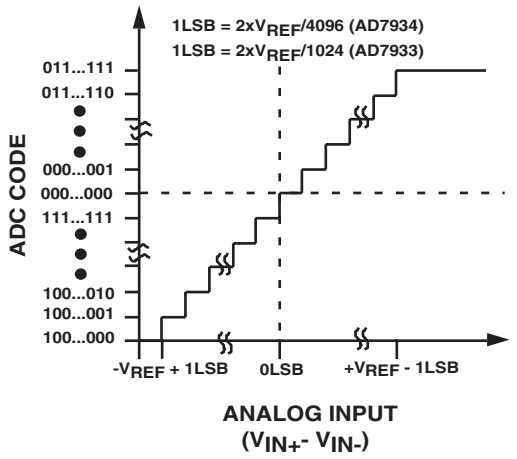


Figure 5. AD7934/AD7933 Ideal Transfer Characteristic with Twos Complement Output Coding

TYPICAL CONNECTION DIAGRAM

Figure 6 shows a typical connection diagram for the AD7934/AD7933. The AGND and DGND pins are connected together at the device for good noise supression. The V_{REFIN}/V_{REFOUT} pin is decoupled to AGND with a 0.1µF capacitor to avoid noise pickup if the internal reference is used. Alternatively, V_{REFIN}/V_{REFOUT} can be connected to an external decoupled reference source. In both cases the analog input range can either be 0V to V_{REF} (Range bit = 1) or 0V to 2 x V_{REF} (Range bit = 0). The analog input configuration can be either 4 Single Ended inputs, 2 Differential Pairs or 2 Pseudo Differential Pairs (see Table III). The V_{DD} pin is connected to either a 3V or 5V supply. The voltage applied to the V_{DRIVE} input controls the voltage of the digital interface and here, it is connected to the same 3V supply of the microprocessor to allow a 3V logic interface (See the digital inputs section).

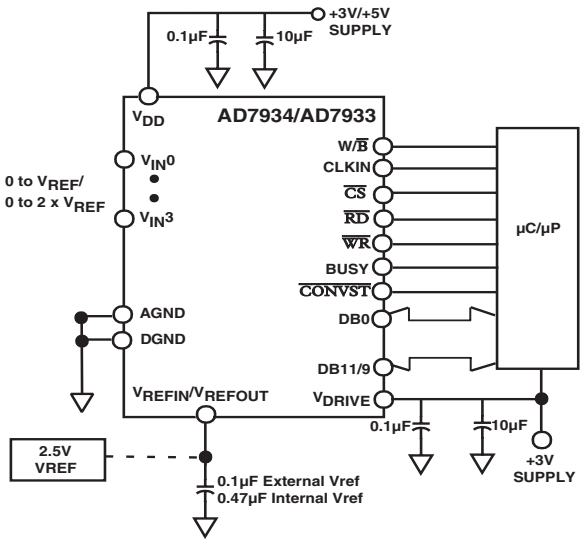


Figure 6. Typical Connection Diagram

ANALOG INPUT STRUCTURE

Figure 7 shows the equivalent circuit of the analog input structure of the AD7934/AD7933 in Differential/Pseudo Differential Mode. In Single Ended mode, V_{IN-} is internally tied to AGND. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting into the substrate. These diodes can conduct up to 10mA without causing irreversible damage to the part.

The capacitors C1, in figure 7 are typically 4pF and can primarily be attributed to pin capacitance. The resistors are lumped components made up of the on-resistance of the switches. The value of these resistors is typically about 100Ω. The capacitors, C2, are the ADC's sampling capacitors and have a capacitance of 16pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal to noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the opamp will be a function of the particular application.

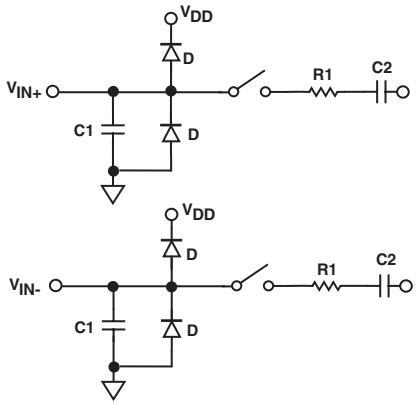


Figure 7. Equivalent Analog Input Circuit. Conversion Phase - Switches Open Track Phase - Switches Closed

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of Total Harmonic Distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 8 shows a graph of the THD versus analog input signal frequency for different source impedances for both V_{DD} = 5 V and 3 V.

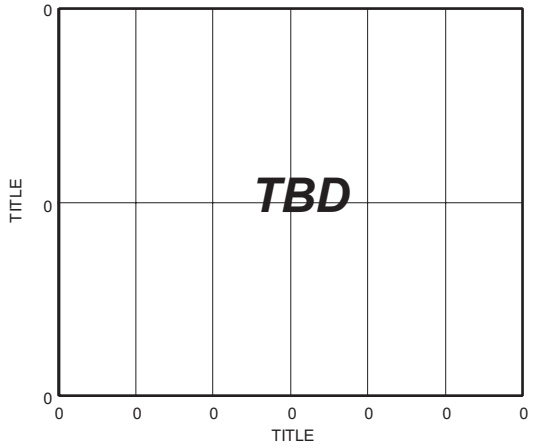


Figure 8.THD vs Analog Input Frequency for Various Source Impedances

Figure 9 shows a graph of THD versus analog input frequency for various supplies, while sampling at 1.5MHz with an SCLK of 20 MHz. In this case the source impedance is 10Ω.

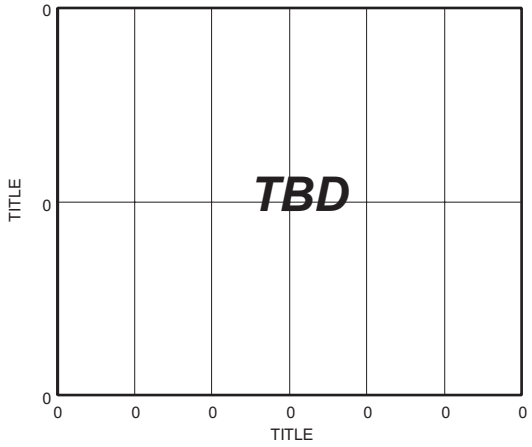


Figure 9.THD vs Analog Input Frequency for various Supply Voltages

THE ANALOG INPUTS

The AD7934/AD7933 has software selectable analog input configurations. The user can choose either 4 Single Ended Inputs, 2 Fully Differential Pairs or 2 Pseudo Differential Pairs. The analog input configuration is chosen by setting the MODE0/MODE1 bits in the internal control register (See Table III).

Single Ended Mode

The AD7934/AD7933 can have 4 single ended analog input channels by setting the MODE0 and MODE1 bits in the control register both to 0. In applications where the signal source has a high impedance, it is recommended to buffer the analog input before applying it to the ADC. The internal reference can be used to externally bias up a bipolar analog input signal. Figure 10 shows a typical connection diagram when operating the ADC in single ended mode.

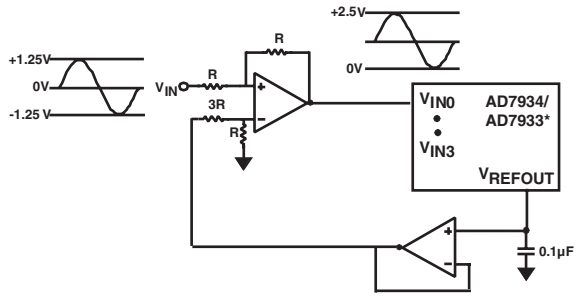


Figure 10. Single Ended Mode Connection Diagram

Differential Mode

The AD7934/AD7933 can have 2 Differential Input Pairs by setting the MODE0 and MODE1 bits in the control register to 0 and 1 respectively.

Differential signals have some benefits over single ended signals including noise immunity based on the device's common mode rejection and improvements in distortion performance. Figure 11 defines the fully differential analog input of the AD7934/AD7933.

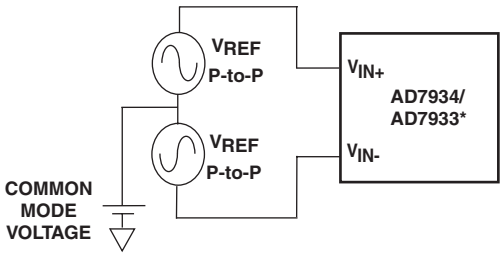


Figure 11. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (i.e. V_{IN+} - V_{IN-}). V_{IN+} and V_{IN-} should be simultaneously driven by two signals each of amplitude V_{REF} that are 180° out of phase. The amplitude of the differential signal is therefore -V_{REF} to +V_{REF} peak-to-peak (i.e. 2 x V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, i.e. (V_{IN+} + V_{IN-})/2 and is therefore the voltage that the two inputs are centered on. This results in the span of each input being CM ± V_{REF}/2. This voltage has to be set up externally and its range varies with V_{REF}. As the value of V_{REF} increases, the common mode range decreases. When driving the inputs with an amplfier, the actual common mode range will be determined by the amplifier's output voltage swing.

Figures 12 and 13 show how the common mode range typically varies with V_{REF} for both a 5 V and a 3 V power supply. The common mode must be in this range to guarantee the functionality of the AD7934/AD7933.

When a conversion takes place, the common mode is rejected resulting in a virtually noise free signal of amplitude $-V_{REF}$ to $+V_{REF}$ corresponding to he digital codes of 0 to 4095.

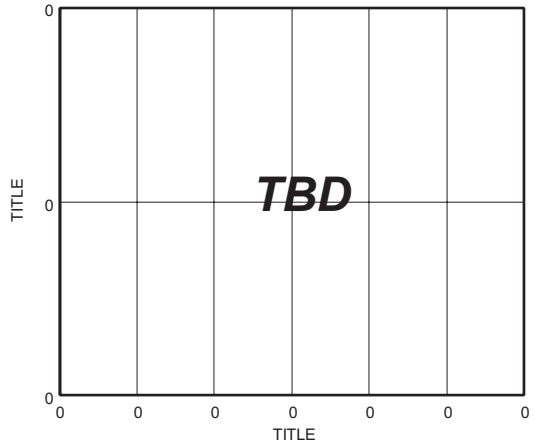


Figure 12. Input Common Mode Range versus V_{REF} (V_{DD} = 5V and V_{REF} (max) = 3.5V)

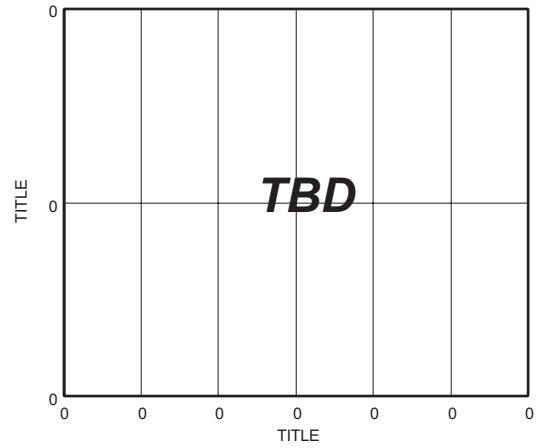


Figure 13. Input Common Mode Range versus V_{REF} (V_{DD}= 3V and V_{REF} (max) = 2.2V)

Driving Differential Inputs

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two equal signals that are 180° out of phase. The common mode must be set up externally and has a range which is determined by V_{REF}, the power supply and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input, provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single ended to differential conversion.

Differential Amplifier

An ideal method of applying differential drive to the AD7934/AD7933 is to use a differential amplifier such as the AD8138. This part can be used as a single ended to differential amplifier or as a differential to differential amplifier. In both cases the analog input needs to be bipolar. It also provides common mode level shifting and buffering of the bipolar input signal. Figure 14 shows how the AD8138 can be used as a single ended to differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADC. The RC low pass filter on each analog input is recommended in ac applications to remove high frequency components of the analog input. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components.

If the analog input source being used has zero impedance then all four resistors (Rg1, Rg2, Rf1, Rf2) should be the same. If the source has a 50 Ω impedance and a 50 Ω termination for example, the value of Rg2 should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain (see figure 14). The outputs of the amplifier are perfectly matched, balanced differential outputs of identical amplitude and are exactly 180° out of phase.

The AD8138 is specified with 3 V, 5 V and ±5 V power supplies but the best results are obtained when it is supplied by ±5 V. A lower cost device that could also be used in this configuration with slight differences in characteristics to the AD8138 but with similar performance and operation is the AD8132.

TBD

Figure 14. Using the AD8138 as a Single Ended to Differential Amplifier

Pseudo Differential Mode

The AD7934/AD7933 can have 2 Pseudo Differential pairs by setting the MODE0 and MODE1 bits in the control register to 1, 0. V_{IN+} is connected to the signal source which must have an amplitude of V_{REF} to make use of the full dynamic range of the part. A DC input in the range -100mV to +100mV is applied to the V_{IN-} pin . The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADCs ground allowing DC common mode voltages to be cancelled. Figure 15 shows a connection diagram for Pseudo Differential Mode.

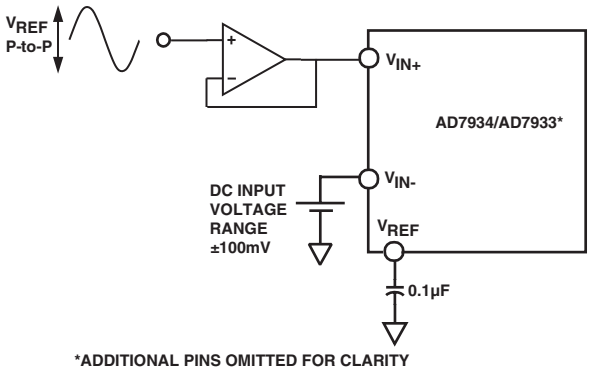


Figure 15. Pseudo Differential Mode Connection Diagram

ANALOG INPUT SELECTION

As illustrated in Table III, the user can set up their analog input configuration by setting the values in the MODE0 and MODE1 bits in the Control Register. Assuming the configuration has been chosen, there are different ways of selecting the analog input to be converted on depending on the state of the SEQ1 and SEQ0 bits in the Control register.

Normal Multichannel Operation (SEQ1=SEQ0= 0)

Any one of four analog input channels or 2 pairs of channels may be selected for conversion in any order by setting the SEQ1 & SEQ0 bits in the Control register both to 0. The channel to be converted on is selected by writing to the address bits ADD1 & ADD0 in the control register to program the multiplexer prior to the conversion. This mode of operation is of a normal multichannel ADC where each data write selects the next channel for conversion. Figure 16 shows a flow chart of this mode of operation. The channel configurations are shown in Table III.

TBD

Figure 16. Normal Multichannel Operation Flow Chart

Using the Sequencer

Consecutive Sequence (SEQ1 =1, SEQ0 = 1)

A sequence of consecutive channels can be converted on beginning with channel 0 and ending with a final channel selected by writing to the ADD1 & ADD0 bits in the Control register. This is done by setting the SEQ1 and SEQ0 bits in the control register both to 1. Once the control register has been written to to set this mode up, the next conversion will be on Channel 0, then Channel 1 and so on until the channel selected via the address bits is reached. The ADC will then return to channel 0. It is not necessary to write to the control register once the sequencer operation has been initiated. The $\overline{WR}$ input must be kept high to ensure that the Control Register is not accidently overwritten, or a sequencer operation interrupted. If the Control Register is written to at any time during the sequence then it must be ensured that the SEQ1 and SEQ0 bits are set to 1, 0. This pattern will continue until such time as the AD7934/AD7933 is written to and the SEQ1 and SEQ0 bits are configured as 0,0 or 0, 1. Figure 17 shows the flow chart of the Consecutive Sequence mode.

TBD

Figure 17. Consecutive Sequence Mode Flow Chart

REFERENCE SECTION

The AD7934/AD7933 can operate with either the on chip reference or an external reference. The internal reference is selected by setting the REF bit in the interal Control register to 0. A block diagram of the internal reference circuitry is shown in Figure 18. The internal reference circuitry includes an on-chip 2.5 V band gap reference, and a reference buffer. When using the internal reference the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.47µF capacitor. This internal reference not only provides the reference for the analog to digital conversion but can also be used externally in the system. It is recommended that the reference output is buffered using an external precision opamp before applying it anywhere in the system.

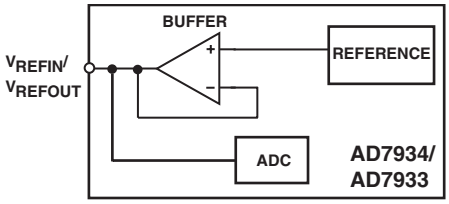


Figure 18. Internal Reference Circuit Block Diagram

Alternatively, an external reference source in the range of 100mV to 3.5V can be applied to the V_{REFIN}/V_{REFOUT} pin of the AD7934/AD7933. An external reference is selected by setting the REF bit in the interal Control register to 1. When using an external reference the V_{REFIN}/V_{REFOUT} pin should be decoupled to AGND with a 0.1µF capacitor. With a 5 V power supply, the specified reference is 2.5 V and maximum reference is 3.5V. With a 3 V power supply, the specified reference is 2.5V and the maximum

reference is 2.6 V. In both cases, the reference is functional from 100mV.
It is important to ensure that, when chosing the reference value, the maximum analog input range (VINmax) is never greater than V_{DD} + 0.3V to comply with the maximum ratings of the device. The following two examples calculate the maximum V_{REF} input that can be used when operating the AD7934/AD7933 at V_{DD} of 5 V and 3 V respectively.

Example 1:

VINmax = V_{DD} + 0.3

VINmax = V_{REF} + V_{REF}/2

If V_{DD} = 5 V

then VINmax = 5.3 V

Therefore 3xV_{REF}/2 = 5.3 V

V_{REF} max = 3.5 V

Therefore, when operating at V_{DD} = 5 V, the value of V_{REF} can range from 100mV to a maximum value of 3.5V. When V_{DD} = 4.75 V, V_{REF} max = 3.17 V.

Example 2:

VINmax = V_{DD} + 0.3

VINmax = V_{REF} + V_{REF}/2

If V_{DD} = 3.6V

then VINmax = 3.9 V

Therefore 3xV_{REF}/2 = 3.6 V

V_{REF} max = 2.6 V

Therefore, when operating at V_{DD} = 3 V, the value of V_{REF} can range from 100mV to a maximum value of 2.4V. When V_{DD} = 2.7 V, V_{REF} max = 2 V.

These examples show that the maximum reference applied to the AD7934/AD7933 is directly dependant on the value applied to V_{DD}.

The performance of the part at different reference values is shown in TBD to TBD. The value of the reference sets the analog input span and the common mode voltage range. Errors in the reference source will result in gain errors in the AD7934/AD7933 transfer function and will add to specified full scale errors on the part. When using an external reference, a capacitor of 0.1µF should be used to decouple the V_{REF} pin to AGND.

Table VI lists examples of suitable voltage references that could be used that are available from Analog Devices and Figure 19 shows a typical connection diagram for an external reference.

Table VI Examples of Suitable Voltage References

Reference	Output Voltage	Initial Accuracy (% max)	Operating Current (µA)
AD589	**1.235**	**1.2-2.8**	**50**
AD1580	**1.225**	**0.08-0.8**	**50**
REF192	**2.5**	**0.08-0.4**	**45**
REF43	**2.5**	**0.06-0.1**	**600**
AD780	**2.5**	**0.04-0.2**	**1000**

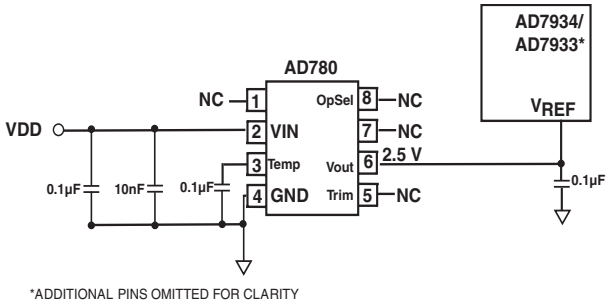


Figure 19. Typical V_{REF} Connection Diagram

Digital Inputs

The digital inputs applied to the AD7934/AD7933 are not limited by the maximum ratings which limit the analog inputs. Instead, the digital inputs applied can go to 7V and are not restricted by the AV_{DD} +0.3V limit as on the analog inputs.

Another advantage of the digital inputs not being restricted by the AV_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If any of these inputs are applied before AV_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to AV_{DD}.

V_{DRIVE} Input

The AD7934/AD7933 has a V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the Parallel Interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7934/AD7933 were operated with an AV_{DD} of 5V, and the V_{DRIVE} pin could be powered from a 3V supply. The AD7934/AD7933 has better dynamic performance with an AV_{DD} of 5V while still being able to interface to 3V processors. Care should be taken to ensure V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V. (See Absolute Maximum Ratings Section).

PARALLEL INTERFACE

The AD7934/AD7933 has a flexible, high speed, parallel interface. This interface is 12-bits (AD7934) or 10-bits (AD7933) wide and is capable of operating in either Word (W/$\overline{B}$ tied high) or Byte (W/$\overline{B}$ tied low) mode. The $\overline{CONVST}$ signal is used to power up the ADC and to initiate conversions.

A falling edge on the $\overline{CONVST}$ signal is used to initiate conversions. Once the $\overline{CONVST}$ signal goes low, the BUSY signal goes high for the duration of the Conversion. At the end of the Conversion, BUSY goes low and can be used to activate an Interrupt Service Routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated in parallel to read the 12- or 10- bits of conversion data. When operating the device Auto Shutdown or Auto Standby mode, where the ADC powers down at the end of each conversion, a rising edge on the $\overline{CONVST}$ signal is used to power up the device.

Reading Data from the AD7934/AD7933

With the W/$\overline{B}$ pin tied logic high, the AD7934/AD7933 interface operates in Word mode. In this case, a single read operation from the device accesses the Conversion data word on pins DB0 to DB11. The DB8/HBEN pin assumes its DB8 function. With the W/$\overline{B}$ pin tied to logic low, the AD7934/AD7933 interface operates in Byte mode. In this case, the DB8/HBEN pin assumes its HBEN function. Conversion data from the AD7934/AD7933 must be accessed in two read operations with 8 bits of data provided on DB0 to DB7 for each of the read operations. The HBEN pin determines whether the read operation accesses the high byte or the low byte of the12- or 10-bit word. For a low byte read, DB0 to DB7 provide the 8 LSBs of the 12-/10-bit word. For a high byte read, DB0 to DB4/2 provide the 4/2 MSBs of the 12-/10-bit word. The remainder of the bits in the high byte provide the Channel ID. Figure 1 shows the read cycle timing diagram for a 12-/10-bit transfer. When operated in Word mode, the HBEN input doesnt exist and only the first read operation is required to access data from the device. When operated in Byte mode, the two read cycles shown in figure 20 are required to access the full data word from the device.

The $\overline{CS}$ and $\overline{RD}$ signals are gated internally and level triggered active low. In either Word mode or Byte mode, $\overline{CS}$ and $\overline{RD}$ may be tied together as the timing specification t_8 and t_9 is 0ns min. The data is placed onto the data bus a time t_{11} after both $\overline{CS}$ and $\overline{RD}$ go low. The $\overline{RD}$ rising edge can be used to latch data out of the device. After a time, t_9, the data lines will become 3 stated.

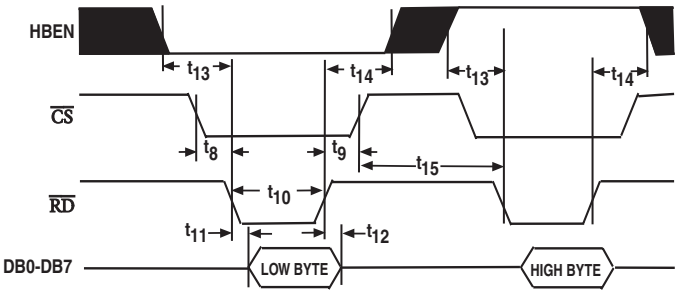


Figure 20. Read Cycle Timing for Byte Mode Operation

Writing Data to the AD7934/AD7933

With W/$\overline{B}$ tied logic high, a single Write operation transfers the full data word on DB0 to DB11/9 to either the Control register or the Shadow register on the AD7934/AD7933. The DB8/HBEN pin assumes its DB8 function. Data to be written to the AD7934/AD7933 should be provided on the DB0 to DB11/9 inputs with DB0 being the LSB of the data word. With W/$\overline{B}$ tied logic low, the AD7934/AD7933 requires two write operations to transfer a full 12-/10-Bit word. DB8/HBEN assumes its HBEN function. Data to be written to the AD7934/AD7933 should be provided on the DB0 to DB7 inputs. HBEN determines whether the byte which is to be written is high byte or low byte data. The low byte of the data word should be written first with DB0 being the LSB of the full data word. For the high byte write, HBEN should be high and the data on the DB0 input should be data bit 8 of the 12-/10-bit word.

Figure 1 shows the write cycle timing diagram of the AD7934/AD7933. When operated in Word mode, the HBEN input does not exist and only the first write operation is required to write data to the device. Data should be provided on DB0 to DB9/DB11. When operated in Byte mode, the two write cycles shown in Figure 21 are required to write the full data word to the AD7934/AD7933. In figure 21, the first write transfers the lower 8 bits of the full data from DB0 to DB7 and the second write transfers the upper 2 or 4 bits of the data word.

The $\overline{CS}$ and $\overline{WR}$ signals are gated internally. $\overline{CS}$ and $\overline{WR}$ may be tied together as the timing specification for t_2 and t_3 is 0ns min. The data is latched into the device on the rising edge of $\overline{WR}$. The data needs to be setup a time t_5 before the $\overline{WR}$ rising edge and held for a time t_6 after the $\overline{WR}$ rising edge.

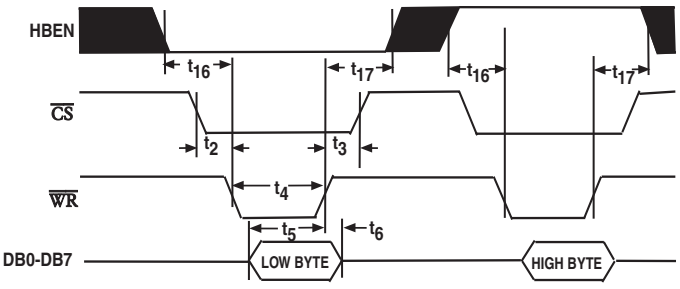


Figure 21. Write Cycle Timing for Byte Mode Operation

MODES OF OPERATION

The AD7934/AD7933 has a number of different power modes of operation. These modes are designed to provide flexible power management options. Different options can be chosen to optimize the power dissipation/throughput rate ratio for differing applications. The mode of operation is selected by the power management bits, PM1 and PM0, in the Control register, as detailed in Table II.

Normal Mode (PM1 = PM0 = 1)
This mode is intended for the fastest throughput rate performance as the user does not have to worry about any power up times as the AD7934/AD7933 remaining fully powered up at all times.

Full Shutdown Mode (PM1 = 1; PM0 = 0)
When this mode is entered, all circuitry on the AD7934/AD7933 is powered down. The part retains the information in the Control Register during the Full Shutdown. The AD7934/AD7933 remains in Full Shutdown mode until the power management bits in the Control Register are changed. If a write to the Control register occurs while the part is in Full Shutdown mode, and the Power Management bits are changed to PM0 = PM1 = 1, i.e. Normal Mode, the part will begin to power up on the $\overline{\text{CONVST}}$ rising edge. To ensure the part is fully powered up before a conversion is initiated, the power up time, TBD, should be allowed before the $\overline{\text{CONVST}}$ falling edge, otherwise, invalid data will be read.

AutoShutdown (PM1 = 0; PM0 = 1)
In this mode of operation, the AD7934/AD7933 automatically enters shutdown at the end of each conversion. In shutdown mode, all internal circuitry on the device is powered. The part retains information in the Control register during shutdown. It remains in shutdown mode until the next rising edge of $\overline{\text{CONVST}}$. On this rising edge, the part will begin to power up and the power up time will depend on whether the user is operating with the internal or an external reference. The user should ensure that at least 1µsec has elapsed before initiating a conversion.

Auto Standby (PM1 = 0; PM0 = 0)
When this mode is entered, all circuitry on the AD7934/AD7933 is powered down except the internal reference. A rising edge on $\overline{\text{CONVST}}$ will power up the device which will take at least 1µsec.

POWER VS. THROUGHPUT RATE

A big advantage of powering the ADC down after a conversion is that the power consumption of the part is significantly reduced at lower throughput rates. When using the different power modes, the AD7934/AD7933 is only powered up for the duration of the conversion. Therefore, the average power consumption is significantly reduced.

MICROPROCESSOR INTERFACING

AD7934/AD7933 To ADSP-2189 Interface
Figure 22 shows a typical interface between the AD7934/AD7933 and the ADSP-2189. The ADSP-2189 can be used in one of two memory modes - Full Memory Mode and Host Mode. The Mode C pin determines in which mode the processor works. The interface, in Figure 22 is set up to have the processor working in Full Memory Mode, which allows full external addressing.

When the AD7934/AD7933 has finished converting, the BUSY line goes low and thus requests an interrupt through the IRQ2 pin. The IRQ2 interrupt has to be set up in the interrupt control register as edge-sensitive. The DMS (Data Memory Select) pin latches in the address of the ADC into the address decoder and therefore starts a read operation.

TBD

Figure 22. Interfacing to the ADSP-2189

APPLICATION HINTS

Grounding and Layout
The printed circuit board that houses the AD7934/AD7933 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place and the connection should be a star ground point established as close to the Ground pins on the AD7934/AD7933 as possible. Avoid running digital lines under the device as this will couple noise onto the die. The analog ground plane should be allowed to run under the AD7934/AD7933 to avoid noise coupling. The power supply lines to the AD7934/AD7933 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

OUTLINE DIMENSIONS

Dimensions shown in inches and mm

28-Lead TSSOP

RU-28