ANALOG DEVICES

Dual High Output Current, High Speed Amplifier

AD8017

FEATURES

High Output Drive Capability
- **20 V p-p Differential Output Voltage, R_L = 50 Ω**
- **10 V p-p Single-Ended Output Voltage While Delivering 200 mA to a 25 Ω Load**

Low Power Operation
- **+5 V to +12 V Voltage Supply @ 7 mA/Amplifier**

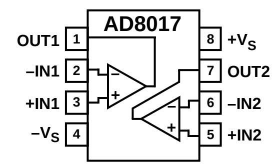
Low Distortion
- **–78 dBc @ 500 kHz SFDR, R_L = 100 Ω, V_O = 2 V p-p**
- **–58 dBc Highest Harmonic @ 1 MHz, I_O = 270 mA (R_L = 10 Ω)**

High Speed
- **160 MHz, –3 dB Bandwidth (G = +2)**
- **1600 V/μs Slew Rate**

APPLICATIONS

xDSL PCI Cards
Consumer DSL Modems
Line Driver
Video Distribution

PIN CONFIGURATION
8-Lead Thermal Coastline SOIC (SO-8)



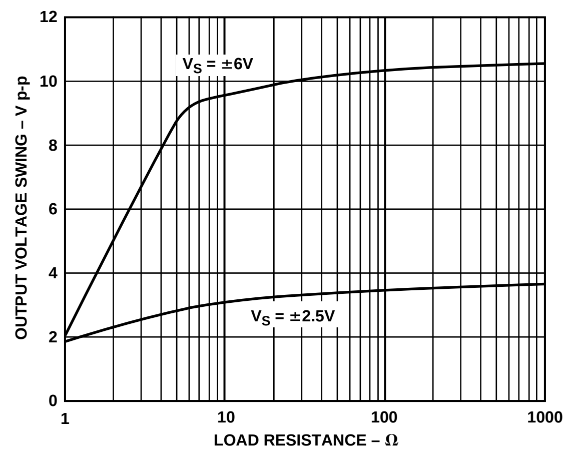


Figure 1. Output Swing vs. Load Resistance

PRODUCT DESCRIPTION

The AD8017 is a low cost, dual high speed amplifier capable of driving low distortion signals to within 1.0 V of the supply rail. It is intended for use in single supply xDSL systems where low distortion and low cost are essential. The amplifiers will be able to drive a minimum of 200 mA of output current per amplifier. The AD8017 will deliver –78 dBc of SFDR at 500 kHz, required for many xDSL applications.

Fabricated in ADI's high speed XFCB process, the high bandwidth and fast slew rate of the AD8017 keep distortion to a minimum, while dissipating a minimum amount of power. The quiescent current of the AD8017 is 7 mA/amplifier.

Low distortion, high output voltage drive, and high output current drive make the AD8017 ideal for use in low cost Customer Premise End (CPE) equipment for ADSL, SDSL, VDSL and proprietary xDSL systems.

The AD8017 drive capability comes in a very compact form. Utilizing ADI's proprietary Thermal Coastline SOIC package, the AD8017's total (static and dynamic) power on +12 V supplies is easily dissipated without external heatsink, other than to place the AD8017 on a 4-layer PCB.

The AD8017 will operate over the commercial temperature range 0°C to +85°C.

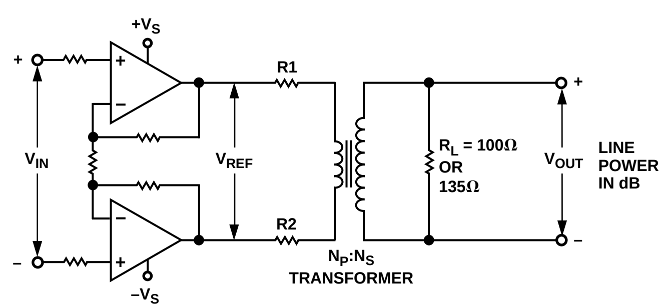


Figure 2. Differential Drive Circuit for xDSL Applications

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD8017–SPECIFICATIONS (@ +25°C, V_S = ±6 V, R_L = 100 Ω, R_F = R_G = 619 Ω, unless otherwise noted)

Parameter	Conditions	AD8017 Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +2, V_{OUT} < 0.4 V p-p	100	160		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p		70		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		105		MHz
Slew Rate	Noninverting, V_{OUT} = 2 V p-p, G = +2		1600		V/µs
Rise and Fall Time	Noninverting, V_{OUT} = 2 V p-p		2.6		ns
Settling Time	0.1%, V_{OUT} = 4 V Step		35		ns
Overload Recovery	V_{IN} = 5 V p-p		74		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
2nd Harmonic	500 kHz, R_L = 100 Ω/25 Ω		–78/–71		dBc
	1 MHz, R_L = 100 Ω/25 Ω		–76/–69		dBc
3rd Harmonic	500 kHz, R_L = 100 Ω/25 Ω		–105/–91		dBc
	1 MHz, R_L = 100 Ω/25 Ω		–81/–72		dBc
IP3	500 kHz, R_L = 100 Ω/25 Ω		40/35		dBm
IMD	500 kHz, R_L = 100 Ω/25 Ω		–76/–66		dBc
MTPR	26 kHz to 1.1 MHz		–66		dBc
Input Noise Voltage	f = 10 kHz		1.9		nV/√Hz
Input Noise Current	f = 10 kHz (+ Inputs)		23		pA√Hz
	f = 10 kHz (– Inputs)		21		pA√Hz
Crosstalk	f = 5 MHz, G = +2		–66		dB
DC PERFORMANCE					
Input Offset Voltage			1.8	3.0	mV
	T_{MIN}–T_{MAX}			4.0	mV
Open Loop Transimpedance	V_{OUT} = 2 V p-p	185	700		kΩ
	T_{MIN}–T_{MAX}	150			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		50		kΩ
Input Capacitance	+Input		2.4		pF
Input Bias Current (+)			16	±45	µA
	T_{MIN}–T_{MAX}			±65	µA
Input Bias Current (–)			1.0	±25	µA
	T_{MIN}–T_{MAX}			±30	µA
CMRR	V_{CM} = ±2.5 V	59	63		dB
Input CM Voltage Range			±5.1		V
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
Output Voltage Swing	R_L = 25 Ω	±4.6	±5.0		V
Output Current[1]	Highest Harmonic < –58 dBc, f = 1 MHz, R_L = 10 Ω	200	270		mA
	T_{MIN}–T_{MAX}, Highest Harmonic < –52 dBc	100			mA
Short-Circuit Current			1500		mA
POWER SUPPLY					
Supply Current/Amp			7.0	7.7	mA
	T_{MIN}–T_{MAX}			7.8	mA
Operating Range	Dual Supply	±2.2		±6.0	V
Power Supply Rejection Ratio		58	61		dB
Operating Temperature Range		0		+85	°C

NOTES

[1]Output current is defined here as the highest current load delivered by the output of each amplifier into a specified resistive load (R_L = 10 Ω), while maintaining an acceptable distortion level (i.e., less than –60 dBc highest harmonic) at a given frequency (f = 1 MHz).

Specifications subject to change without notice.

SPECIFICATIONS (@ +25°C, V_S = ±2.5 V, R_L = 100 Ω, R_F = R_G = 619 Ω, unless otherwise noted)

Parameter	Conditions	AD8017 Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +2, V_{OUT} < 0.4 V p-p	75	120		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p		40		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		100		MHz
Slew Rate	Noninverting, V_{OUT} = 2 V p-p, G = +2		800		V/µs
Rise and Fall Time	Noninverting, V_{OUT} = 2 V p-p		2.0		ns
Settling Time	0.1%, V_{OUT} = 2 V Step		35		ns
Overload Recovery	V_{IN} = 2.5 V p-p		74		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p				
2nd Harmonic	500 kHz, R_L = 100 Ω/25 Ω		–75/–68		dBc
	1 MHz, R_L = 100 Ω/25 Ω		–73/–66		dBc
3rd Harmonic	500 kHz, R_L = 100 Ω/25 Ω		–91/–88		dBc
	1 MHz, R_L = 100 Ω/25 Ω		–79/–74		dBc
IP3	500 kHz, R_L = 100 Ω/25 Ω		40/36		dBm
IMD	500 kHz, R_L = 100 Ω/25 Ω		–78/–64		dBc
MTPR	26 kHz to 1.1 MHz		–66		dBc
Input Noise Voltage	f = 10 kHz		1.8		nV/√Hz
Input Noise Current	f = 10 kHz (+ Inputs)		23		pA√Hz
	f = 10 kHz (– Inputs)		21		pA√Hz
Crosstalk	f = 5 MHz, G = +2		–66		dB
DC PERFORMANCE					
Input Offset Voltage			0.8	2.0	mV
	T_{MIN}–T_{MAX}			2.6	mV
Open Loop Transimpedance	V_{OUT} = 2 V p-p	40	166		kΩ
	T_{MIN}–T_{MAX}	46			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		50		kΩ
Input Capacitance	+Input		2.4		pF
Input Bias Current (+)			16	±40	µA
	T_{MIN}–T_{MAX}			±60	µA
Input Bias Current (–)			2	±25	µA
	T_{MIN}–T_{MAX}			±30	µA
CMRR	V_{CM} = ±1.0 (±1.0)	57	60		dB
Input CM Voltage Range			±1.6		V
OUTPUT CHARACTERISTICS					
Output Resistance			0.2		Ω
Output Voltage Swing	R_L = 25 Ω	±1.55	±1.65		V
Output Current[1]	Highest Harmonic < –55 dBc, f = 1 MHz, R_L = 10 Ω	100	120		mA
	T_{MIN}–T_{MAX} Highest Harmonic < 50 dBc	60			mA
Short-Circuit Current			1300		mA
POWER SUPPLY					
Supply Current/Amp			6.2	7	mA
	T_{MIN}–T_{MAX}			7.3	mA
Operating Range	Dual Supply	±2.2		±6.0	V
Power Supply Rejection Ratio		59	62		dB
Operating Temperature Range		0		+85	°C

NOTES

[1]Output current is defined here as the highest current load delivered by the output of each amplifier into a specified resistive load (R_L = 10 Ω), while maintaining an acceptable distortion level (i.e., less than –60 dBc highest harmonic) at a given frequency (f = 1 MHz).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . . 1.3 W
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±2.5 V
Output Short Circuit Duration
. . . . Observe Power Derating Curves
Storage Temperature Range . . . . –65°C to +125°C
Operating Temperature Range . . . . 0°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device on a two-layer board with 2500 mm^2 of 2 oz. copper at +25°C 8-lead SOIC package: θ_{JA} = 95.0°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8017AR	0°C to +85°C	8-Lead SOIC	SO-8

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

The output stage of the AD8017 is designed for maximum load current capability. As a result, shorting the output to common can cause the AD8017 to source or sink 500 mA. To ensure proper operation, it is necessary to observe the maximum power derating curves. Direct connection of the output to either power supply rail can destroy the device.

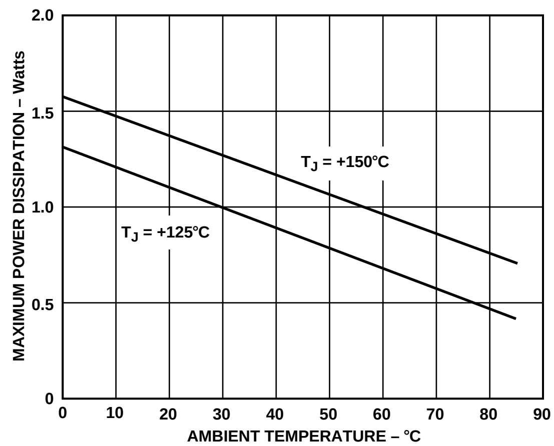


Figure 3. Plot of Maximum Power Dissipation vs. Temperature for AD8017

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8017 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

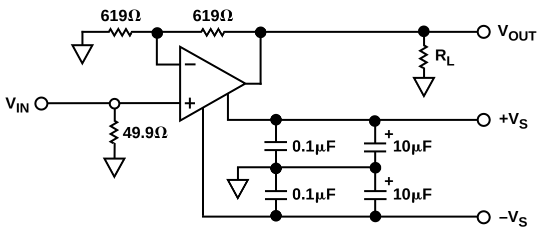


Figure 4. Test Circuit: Gain = +2

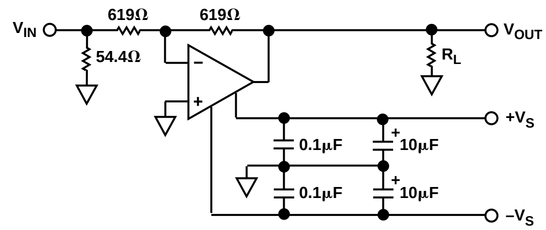


Figure 7. Test Circuit: Gain = –1

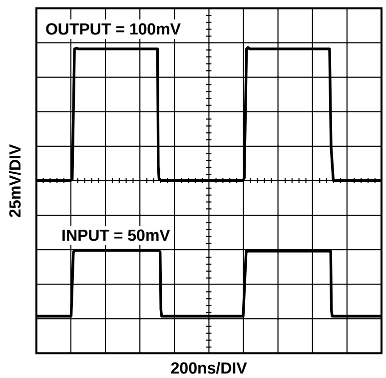


Figure 5. 100 mV Step Response; G = +2, V_S = ±2.5 V or ±6 V, R_L = 100 Ω

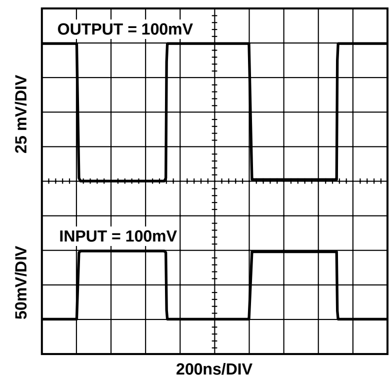


Figure 8. 100 mV Step Response; G = –1, V_S = ±2.5 V or ±6 V, R_L = 100 Ω

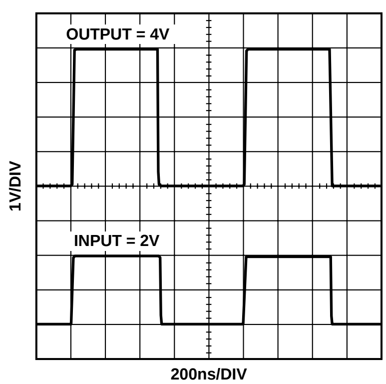


Figure 6. 4 V Step Response; G = +2, V_S = ±6 V, R_L = 100 Ω

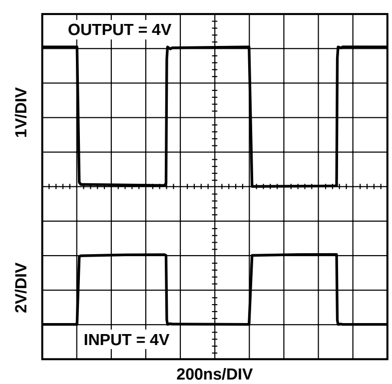


Figure 9. 4 V Step Response; G = –1, V_S = ±6 V, R_L = 100 Ω

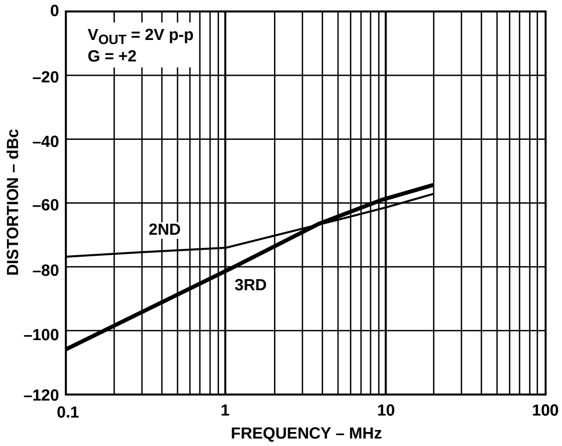


Figure 10. Distortion vs. Frequency; V_S = ±6 V, R_L = 100 Ω

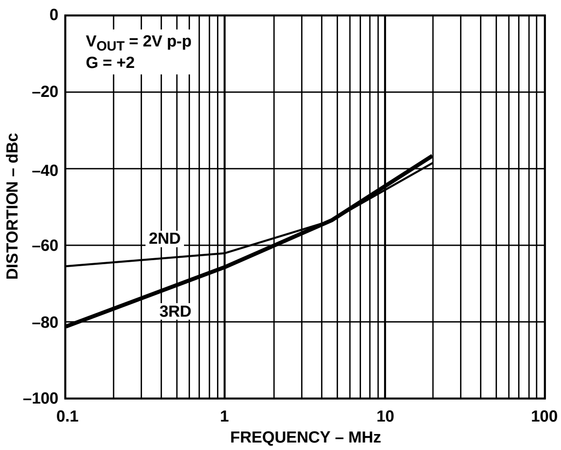


Figure 11. Distortion vs. Frequency; V_S = ±6 V, R_L = 25 Ω

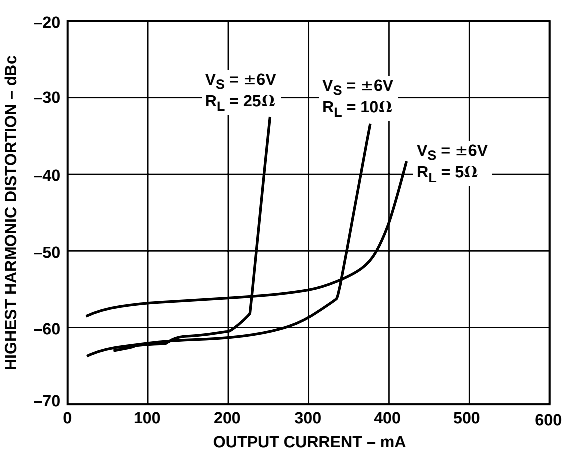


Figure 12. Distortion vs. Output Current; V_S = ±6 V, f = 1 MHz, G = +2

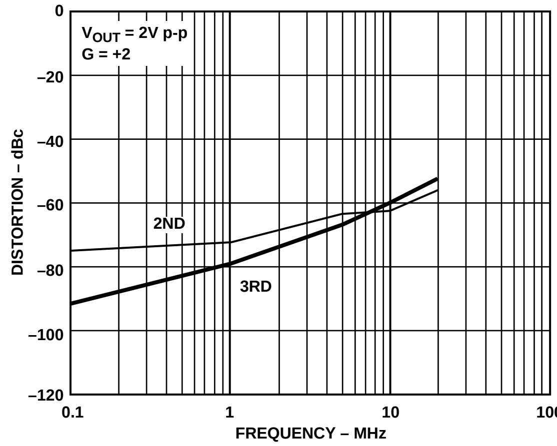


Figure 13. Distortion vs. Frequency; V_S = ±2.5 V, R_L = 100 Ω

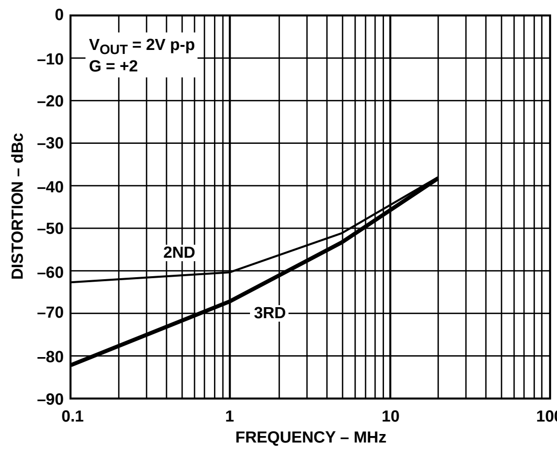


Figure 14. Distortion vs. Frequency; V_S = ±2.5 V, R_L = 25 Ω

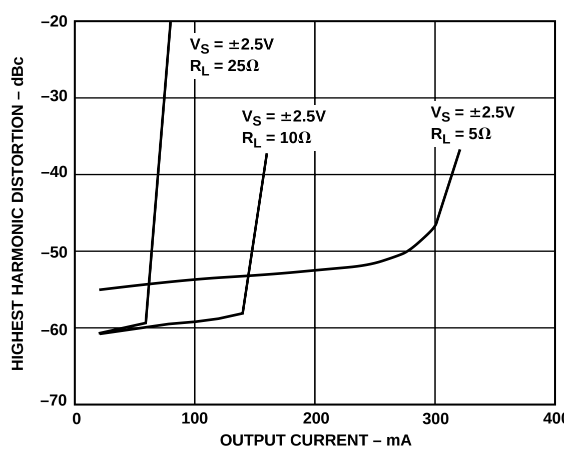


Figure 15. Distortion vs. Output Current; V_S = ±2.5 V, f = 1 MHz, G = +2

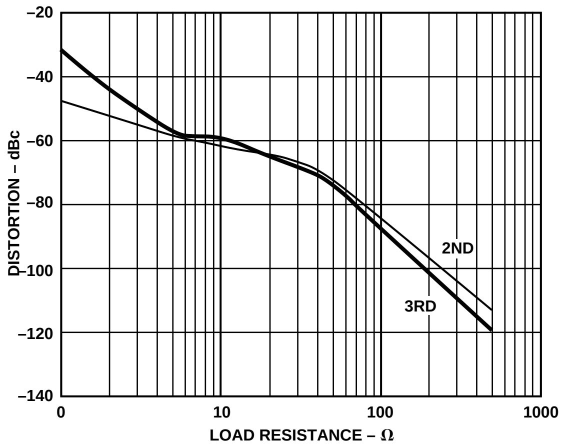


Figure 16. Distortion vs. R_L, $V_S = \pm 6$ V, G = +2, V_{OUT} = 2 V p-p, f = 1 MHz

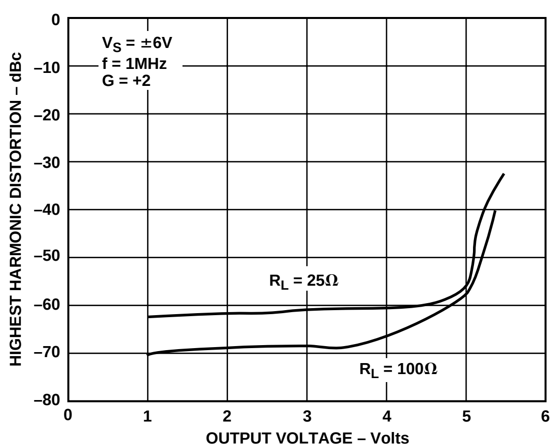


Figure 17. Distortion vs. Output Voltage, $V_S = \pm 6$ V, G = +2, f = 1 MHz

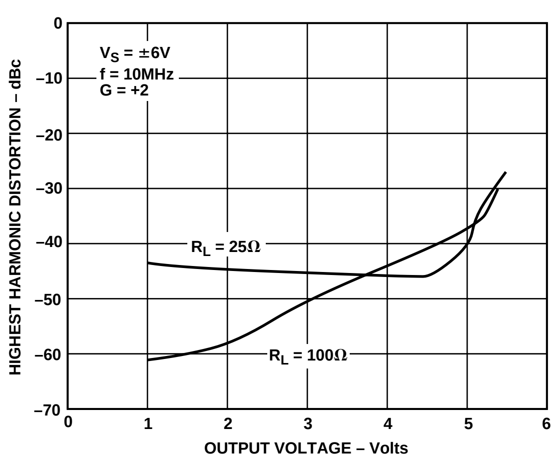


Figure 18. Distortion vs. Output Voltage, $V_S = \pm 6$ V, G = +2, f = 10 MHz

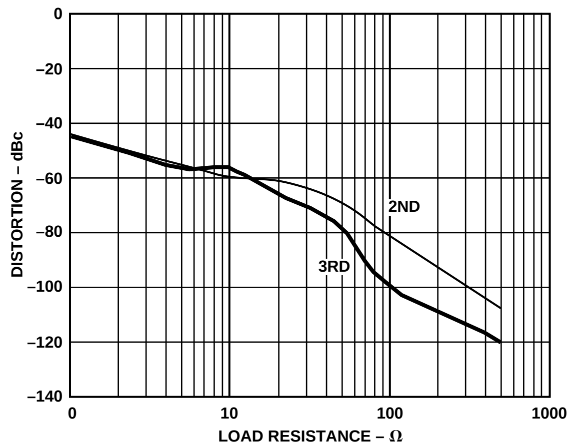


Figure 19. Distortion vs. R_L, $V_S = \pm 2.5$ V, G = +2, V_{OUT} = 2 V p-p, f = 1 MHz

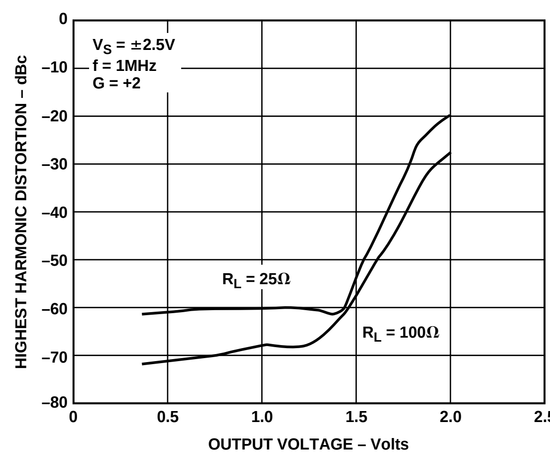


Figure 20. Distortion vs. Output Voltage, $V_S = \pm 2.5$ V, G = +2, f = 1 MHz

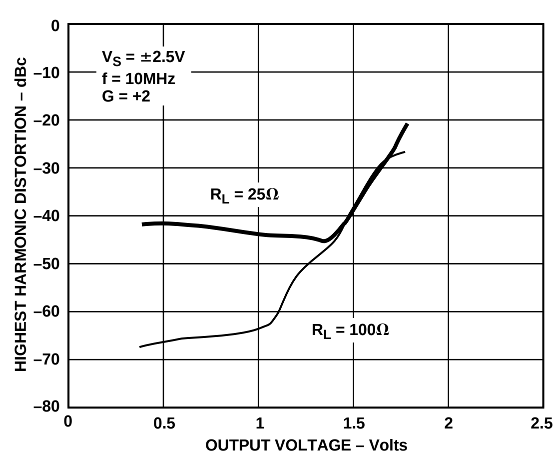


Figure 21. Distortion vs. Output Voltage, $V_S = \pm 2.5$ V, G = +2, f = 10 MHz

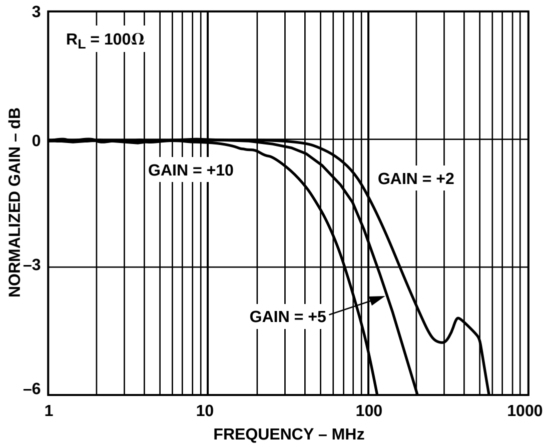


Figure 22. Frequency Response; $V_S = \pm 6$ V

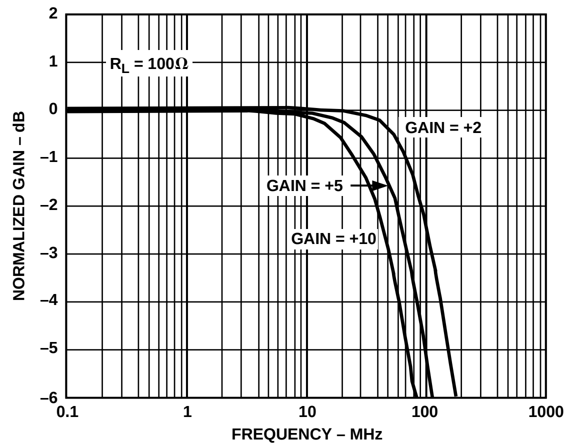


Figure 25. Frequency Response; $V_S = \pm 2.5$ V

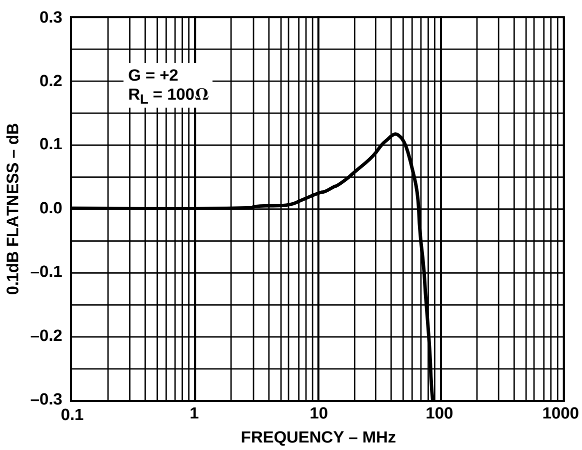


Figure 23. Gain Flatness; $V_S = \pm 6$ V

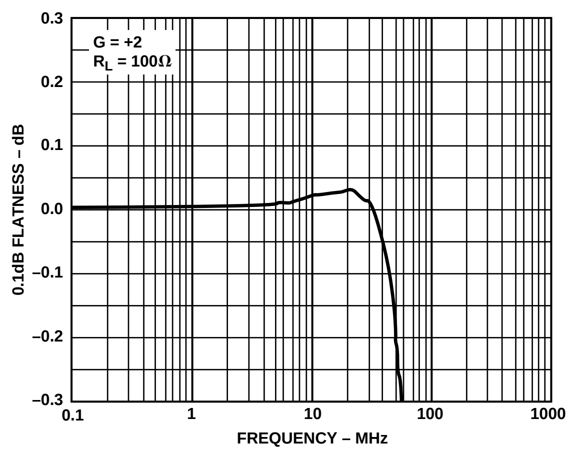


Figure 26. Gain Flatness; $V_S = \pm 2.5$ V

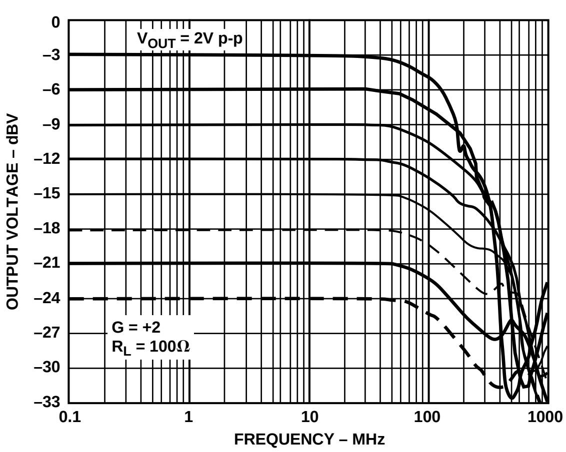


Figure 24. Output Voltage vs. Frequency; $V_S = \pm 6$ V

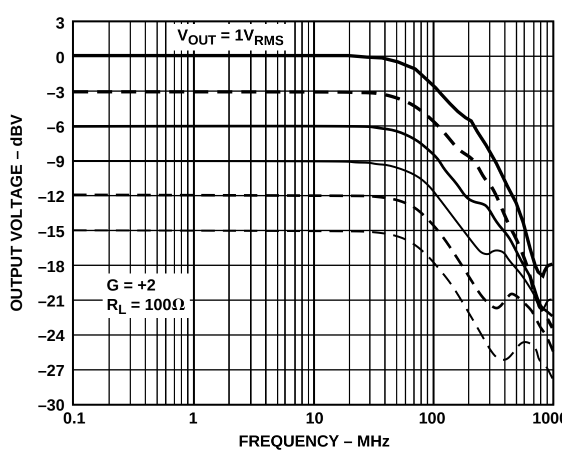


Figure 27. Output Voltage vs. Frequency; $V_S = \pm 2.5$ V

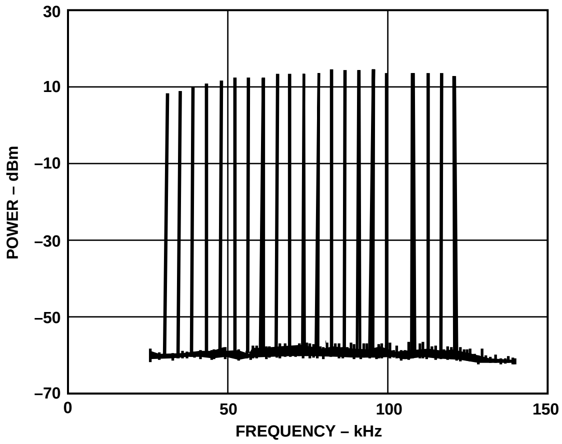


Figure 28. Multitone Power Ratio: $V_S = \pm6$ V, 27 dBm Output Power into 25 Ω

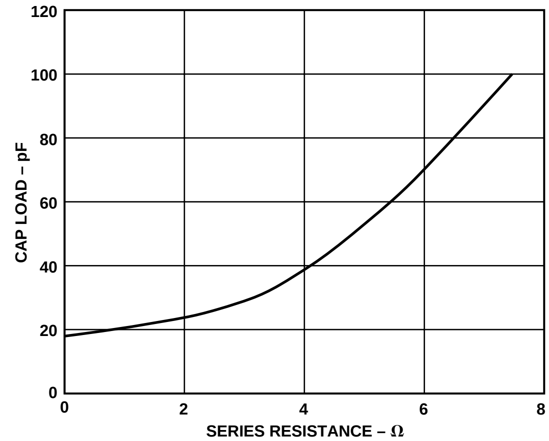


Figure 31. R_S and C_L vs. 30% Overshoot

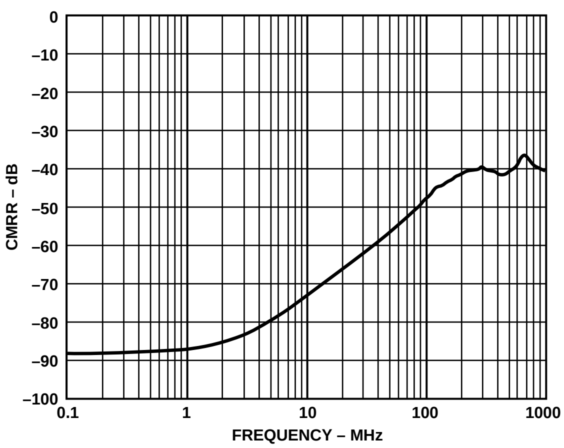


Figure 29. CMRR vs. Frequency; $V_S = \pm6$ V or $V_S = \pm2.5$ V

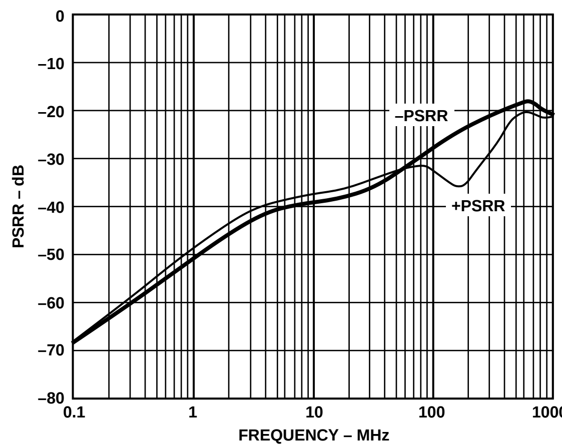


Figure 32. PSRR vs. Frequency; $V_S = \pm6$ V or $V_S = \pm2.5$ V

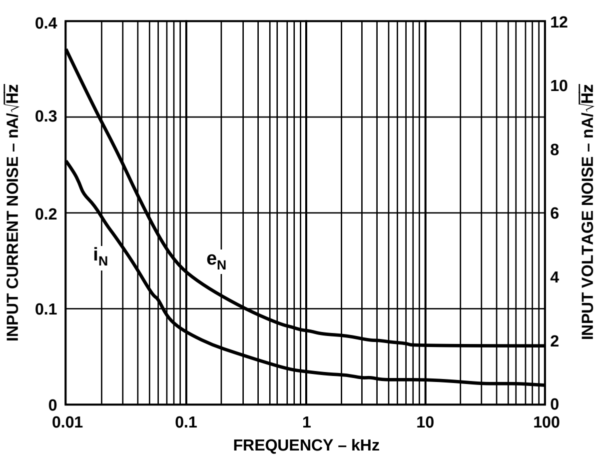


Figure 30. Noise vs. Frequency

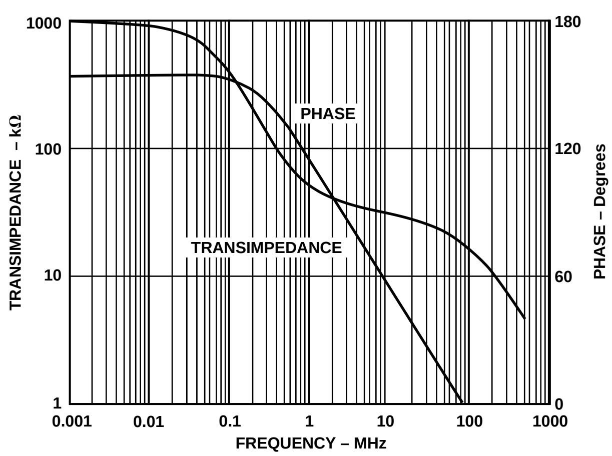


Figure 33. Open-Loop Transimpedance and Phase vs. Frequency

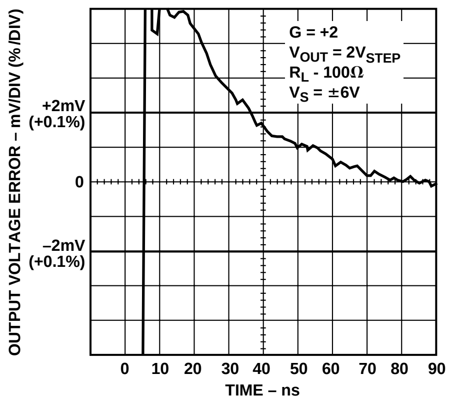


Figure 34. Settling Time; $V_S = \pm 6.0$ V

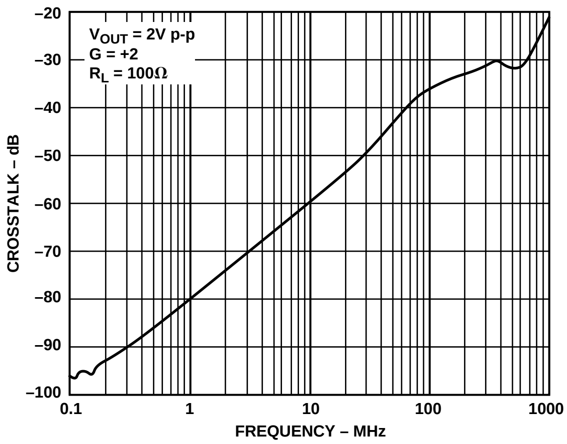


Figure 35. Output Crosstalk vs. Frequency

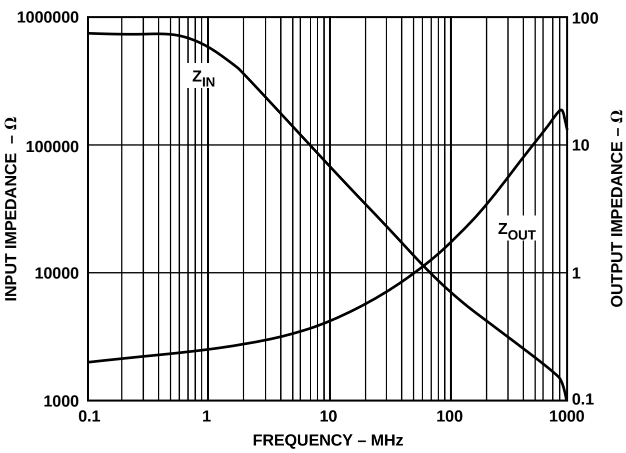


Figure 36. Input and Output Impedance vs. Frequency

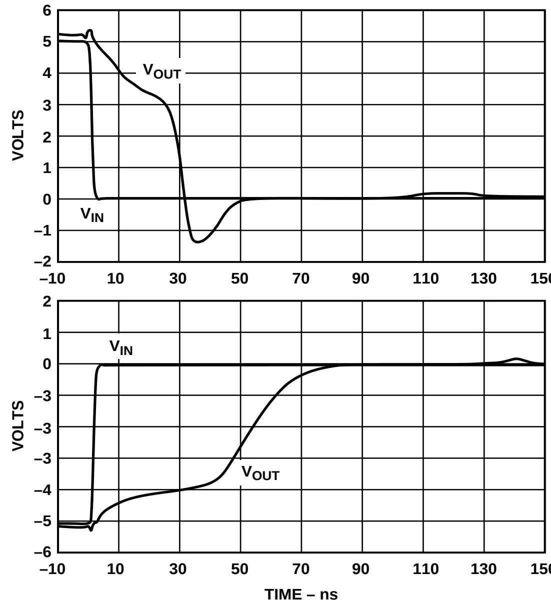


Figure 37. Overload Recovery; $V_S = \pm 6$ V, G = +2, R_L = 100 Ω, V_{IN} = 5 V p-p, T = 1 µs

THEORY OF OPERATION

The AD8017 is a dual high speed CF amplifier that attains new levels of bandwidth (BW), power, distortion and signal swing, under heavy current loads. Its wide dynamic performance (including noise) is the result of both a new complementary high speed bipolar process and a new and unique architectural design. The AD8017 basically uses a two gain stage complementary design approach versus the traditional "single stage" complementary mirror structure sometimes referred to as the Nelson amplifier. Though twin stages have been tried before, they typically consumed high power since they were of a folded cascode design much like the AD9617.

This design allows for the standing or quiescent current to add to the high signal or slew current-induced stages. In the time domain, the large signal output rise/fall time and slew rate is typically controlled by the small signal BW of the amplifier and the input signal step amplitude respectively, not the dc quiescent current of the gain stages (with the exception of input level shift diodes Q1/Q2). Using two stages as opposed to one, also allows for a higher overall gain bandwidth product (GBWP) for the same power, thus providing lower signal distortion and the ability to drive heavier external loads. In addition, the second gain stage also isolates (divides down) A3's input reflected load drive and the nonlinearities created resulting in relatively lower distortion and higher open-loop gain. See Figure 38.

Overall, when "high" external load drive and low ac distortion is a requirement, a twin gain stage integrating amplifier like the AD8017 will provide excellent results for low power over the traditional single stage complementary devices. In addition, being a CF amplifier, closed-loop BW variations versus external gain variations (varying R_G) will be much lower compared to a VF op amp, where the BW varies inversely with gain. Another key attribute of this amplifier is its ability to run on a single 5 V supply due in part to its wide common-mode input and output voltage range capability. For 5 V supply operation, the device obviously consumes less than half the quiescent power (vs. 12 V supply) with little degradation in its ac and dc performance characteristics. See specification pages for comparisons.

DC GAIN CHARACTER

Gain stages A1/$\overline{A1}$ and A2/$\overline{A2}$ combined provide negative feedforward transresistance gain. See Figure 38. Stage A3 is a unity gain buffer which provides external load isolation to A2. Each stage uses a symmetrical complementary design. (A3 is also complementary, though not explicitly shown). This is done to reduce both second order signal distortion and overall quiescent power as discussed above. In the quasi dc-to-low frequency region, the closed loop gain relationship can be approximated as:

$G = 1+R_F/R_G$ for Noninverting Operation
$G = -R_F/R_G$ for Inverting Operation

These basic relationships above are common to all traditional operational amplifiers.

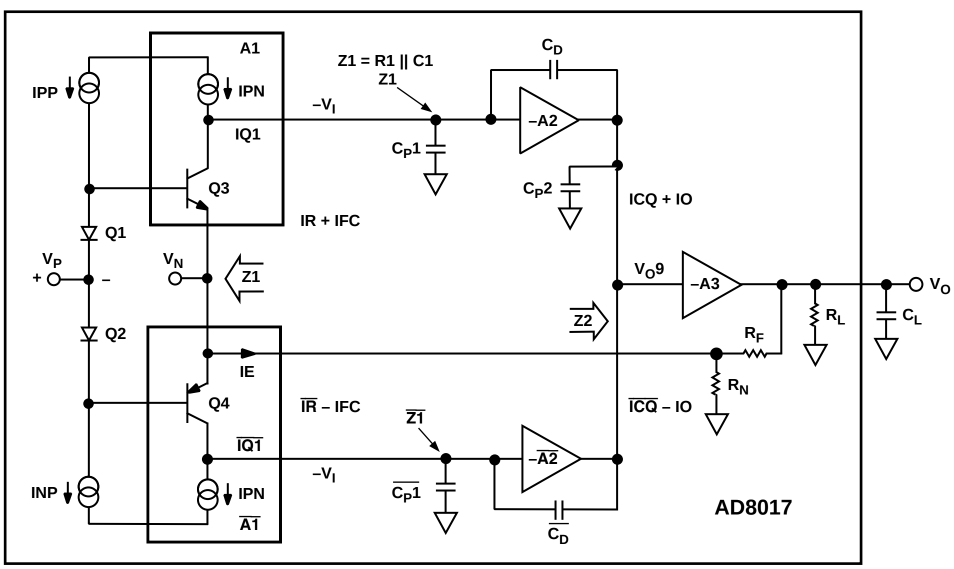


Figure 38. Simplified Block Diagram

APPLICATIONS

Output Power Characteristics as Applied to ADSL Signals

The AD8017 was designed to provide both relatively high current and voltage output capability. Figures 17 and 20 quantify the ac load current versus distortion of the device at loads of 100 Ω and 25 Ω at 1 MHz. Using approximately –50 dBc as the worst case distortion limit, the AD8017 exhibits acceptable linearity to within approximately 1.4 V of either supply rail (12 V or ±6 V) while simultaneously providing 200 mA of load current. These levels are achieved at only 7 mA of quiescent current for each amplifier.

ADSL applications require signal line powers of 13 dBm that can randomly peak to an instantaneous power (or V × I product) of 28.5 dBm. This equates to peak-to-rms voltage ratio of 5.3-to-1. Using a 1:1 transformer in the ADSL circuit illustrated below and 100 Ω as the line resistance, a peak voltage of 8.4 V at a peak current of 84 mA will be required from the line driver output (see Table I). For 12-volt single supply operation, as commonly used in PCs, the AD8017 meets this demanding signal requirement, as discussed above. See detailed application below. A higher turns ratio transformer can be used to reduce the primary output voltage swing of the amplifier (for devices that do not have the voltage swing, but do have the current drive capability). However, this requires more than an equivalent increase in current due to the added I × R losses from the transformer for the same receiver power. Generally this will result in added distortion. Table I below shows the ADSL ac current and voltages required for both a 1:1 and 1:2 transformer turns ratio.

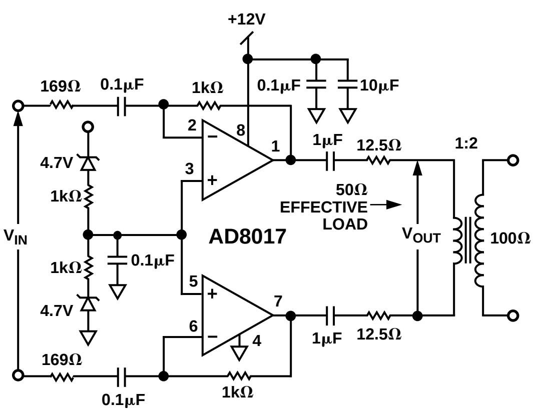


Figure 39. Single +12 V Supply ADSL Remote Terminal Transmitter

Single +12 V Supply ADSL Remote Terminal (RT) Transmitter

For consumer use, it is desirable to create an ADSL modem that can be a plug-in accessory for a PC. In such an application, the circuit should dissipate a minimum of power, yet still meet the ADSL specification.

The circuit in Figure 39 shows a single +12 V supply circuit that uses the AD8017 as a remote terminal transmitter. This supply voltage is readily available on the PCI connector of PCs. The circuit configures each half of the AD8017 as an inverter with a gain of about six. Both of the amplifier circuits are ac coupled at both the inputs and the outputs. This makes the dc levels of the circuit independent of the other dc levels of the signal chain.

The inputs will generally be driven by the output of an active filter, which has a low output impedance. Thus there will be a minimum of loading of the source caused by the 169 Ω input impedance in the pass band. The output will require a 1:2 step-up transformer to drive a 100 Ω line. The reflected impedance back to the primary will be 25 Ω. With 25 Ω of series termination added (12.5 Ω in each output), the effective load that the differential amplifier outputs will drive is 50 Ω.

The input and output ac coupling provides two high pass circuits. The inputs are formed by the 0.1 μF capacitor and the 169 Ω resistor, which provides a break frequency of about 9.4 kHz. The two 1 μF capacitors in the output along with the 50 Ω effective load provides a 6.4 kHz break frequency in the output side. Both of these circuits want to reject the Plain Old Telephone System (POTS) band (dc to 4 kHz) while passing the ADSL upstream band, which starts at about 20 kHz.

The positive inputs must be biased at mid supply, which is nominally +6 V. This will maintain the maximum dynamic range of the output in each direction, regardless of the tolerance of the supply. The inverting configuration was chosen as this requires a steady dc current from this supply, as opposed to the signal-dependent current that would be required in a noninverting configuration. Several options were studied for creating this supply.

A voltage regulator could be used, but there are several disadvantages. The first is that this will not track the middle of the supplies as it will always have an output that is a fixed voltage from ground. This also requires an additional active component that will impact the cost of the total solution.

A two-resistor divider could also be used. There is a tradeoff required here in the selection of the value of the resistors. As the resistors become smaller, the amount of power that they will dissipate will increase. For two 1 kΩ resistors, the power dissipation in this circuit would be 72 mW. Thus, in order to keep this power to a minimum, it is desirable to make the resistors as large as possible.

Table I. DSL Drive Amplifier Requirements for Various Combinations of Line Power, Line Impedance and Turn Ratios

Line Power	Insertion Loss	Line Load	Turns Ratio	Crest Factor	Reflected Impedance	R1 = R2	Per Amp Voltage	Peak Per Amplifier Voltage Output	Peak Current Output
13 dBm	1 dB	100 Ω	1:1	5.3	100 Ω	50 Ω	1.585 V rms	8.4 V peak	84 mA
13 dBm	1 dB	100 Ω	1:2	5.3	25 Ω	12.5 Ω	0.792 V rms	4.2 V peak	168 mA

The practical maximum value that these resistors can have is determined by the offset voltage that is created by the input bias current that flows through them. The maximum input bias current into the + inputs is 45 µA. This will create an offset voltage of 45 mV per 1 kΩ of bias resistor. Fortunately, the ac coupling of the stages provides only unity gain for this dc offset voltage, which is another advantage of this configuration. Any dc offset in the output will limit the amount of dynamic signal swing that will be available between the rails.

The circuit shown uses two 4.7 V Zener diodes that provide a voltage drop which serves to limit the power dissipation in the bias circuit. This allows the use of smaller value resistors in the bias circuit. Thus, for this circuit the current will be (12 V – (2 × 4.7 V))/2 kΩ = 1.3 mA. Thus, this circuit will dissipate only 15.6 mW, yet only induce a maximum of 40 mV of offset at the output. This circuit will also track the midpoint of the supplies over their specified tolerance range.

The distortion of the circuit was measured with a 50 Ω load. The frequency used was 500 kHz, which is beyond the maximum required for the upstream signal. For ADSL over POTS, a maximum frequency of 135 kHz is required. For ADSL over ISDN, the maximum frequency is 276 kHz. The amplitude was 20 V p-p (10 V p-p for each amplifier), which is the maximum crest signal that will be required. The second harmonic was better than –80 dBc, while the third harmonic was –64 dBc. This represents a worst case of the absolute maximum signal that will be required for only a very small statistical basis and at a frequency that is higher than the maximum required. For a statistical majority of the time, the signal will be at a lower amplitude and frequency, where the distortion performance will be better.

When the circuit was run while providing the upstream drive signal in an ADSL system, the supply current to the part was measured at 25 mA. Thus, the total power to the drive circuit was 300 mW. This power winds up in three places: the drive amplifier, down the line and in the termination and interface circuitry.

The ADSL specification calls for 13 dBm or 20 mW into the line. The line termination will consume an equal amount of power, as it is the same resistance value. About a 1 dB loss can be expected in the losses in the interface circuitry, which translates into about 10 mW of power. Thus, the total power dissipated in the AD8017 when used as a driver in this application is about 250 mW.

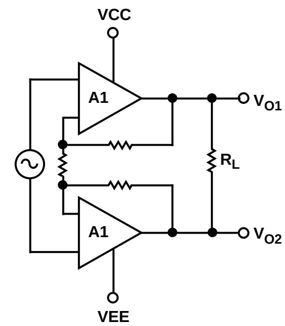


Figure 40. Differential Driver Simplified Circuit Schematic

It is important to consider the total power dissipation of the AD8017 in order to properly size the heatsinking area for your application. The dc power dissipation for $V_{IN} = 0$ is simply, $I_Q \cdot (V_{CC} + V_{EE})$, or $2 \times I_Q \times V_S$. For the AD8017, this number is 0.17 W. In this purely differential circuit we can use symmetry to simplify the computation for a dc input signal,

$$P_D = 2 \times I_Q \times V_S + 4 \times \left(V_S - V_O\right) \times \frac{V_O}{R_L}$$

This formula is slightly pessimistic due to the fact that some of the quiescent supply current commutates during sourcing or sinking current into the load. For a sine wave source, integration over a half cycle yields:

$$P_D = 2 \times I_Q \times V_S + 2 \times \left(\frac{4 V_O V_S}{\pi R_L} - \frac{V_O^2}{R_L} \right) \text{(Refer to Figure 41)}$$

The situation is more complicated with a complex modulated signal. In the case of a DMT signal, taking the equivalent sine wave power overestimates the power dissipation by > 15%. For example:

P_{OUT} = 16 dBm = 40 mW
V_{OUT} @ 50 Ω = 1.41 $V\,rms$ or V_O = 1.0 V

at each amplifier output, which yields a P_D of 0.436 W. By actual measurement, P_D for a DMT signal of 16 dBm requires 0.38 W of power to be dissipated by the AD8017.

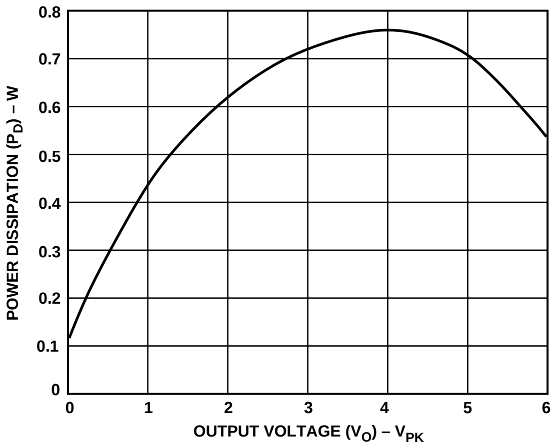


Figure 41. Power Dissipation (P_D) vs. Output Voltage (V_O), R_L = 50 Ω

Thermal Considerations

The AD8017 in a "Thermal Coastline" SO-8 package relies on the device pins to assist in removing heat from the die at a faster rate than that of conventional packages. The effect is to provide a lower θ_{JC} for the device. To make the most effective use of this, special details should be worked into the copper traces of the printed circuit board.

There will be a tradeoff, however, between designing a board that will maximally remove heat, and one that will provide the desired ac performance. This is the result of the additional parasitic capacitance on some of the pins that would be caused by the addition of extra heatsinking copper traces.

The first technique for maximum heatsinking is to use a heavy layer of copper. 2 oz. copper will provide better heatsinking than 1 oz. copper. Additional internal circuit layers can also be used to more effectively remove heat, and to provide better power and ground distribution.

There are no "ground" pins per se on the AD8017 (when run on a dual supply), but the power supplies (Pins 4 and 8) are at ac ground. Thus, these pins can be safely tied to a maximum area of copper foil without affecting the ac performance of the part. On the surface side of the board, the copper area that connects to Pins 4 and 8 should be enlarged and spread out to the maximum extent possible. As a practical matter, there will be diminishing returns from adding copper more than a few centimeters from the pins.

When the power supplies are run on the board on internal power planes, then these should also be made as large as practical, and multiple vias (~0.012 in. or 0.3 mm) should be provided from the component layer near the power supply pins of the AD8017 to the inner layers. These vias should not have any of the traditional "thermal relief" spokes to the planes, because the function of these is to impede heat flow for ease of soldering. This is counter to the effect desired for heatsinking.

On the side of the board opposite the component, additional heatsinking can be provided by adding copper area near the vias to further lower the thermal resistance. Additional vias can be provided throughout to better conduct heat from the inner layers to the outer layers.

The remainder of the device pins are active signal pins and must be treated a bit more carefully. Pins 2 and 6 are the summing junctions of the op amps and will be the most adversely affected by stray capacitance. For this reason, the copper area of these pins should be minimized. In addition, the copper nearby on the component layer should be kept more than 3 mm–5 mm away from these pins, where possible. The inner and opposite side circuit layers directly below the summing junctions should also be void of copper.

The positive inputs and outputs can withstand somewhat more capacitance than the summing junctions without adversely affecting ac performance. However, these pins should be treated carefully, and the amount of heatsinking and excess capacitance should be analyzed and adjusted depending on the application. If maximum ac performance is desired and the power dissipation is not extreme, then the copper area connected to these pins should be minimized. If the ac performance is not very critical and maximum power must be dissipated, then the copper area connected to these pins can be increased. As in many other areas of analog design, the designer must use some judgment based on the consideration of the above, in order to produce a satisfactory design.

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8017 requires careful attention to board layout and component selection.

Table II shows recommended component values for the AD8017 and Figures 42–44 show recommended layouts for the 8-lead SOIC package for a positive gain. Proper RF design techniques and low parasitic component selections are mandatory.

Table II. Typical Bandwidth vs. Gain Setting Resistors (V_S = 6 V, R_L = 100 Ω)

Gain	R_F (Ω)	R_G (Ω)	R_T (Ω)	Small Signal –3 dB BW (MHz)
–1	619	619	54.5	110
+1	619		49.9	320
+2	619	619	49.9	160
+10	619	68.8	49.9	40

R_T chosen for 50 Ω characteristic input impedance.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figures 4 and 7). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional (4.7 µF– 10 µF) tantalum electrolytic capacitor should be connected in parallel.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance greater than 1.5 pF at the inverting input will significantly affect high speed performance when operating at low noninverting gain.

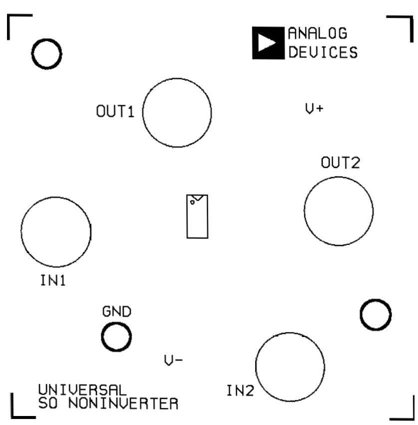


Figure 42. Universal SOIC Noninverter Top Silkscreen

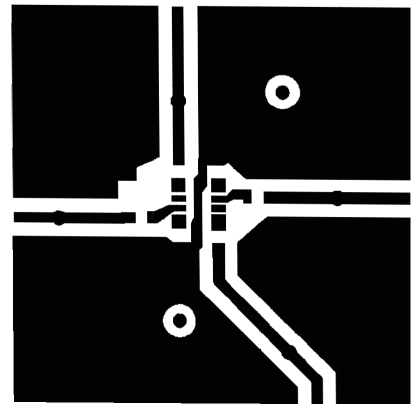


Figure 43. Universal SOIC Noninverter Top

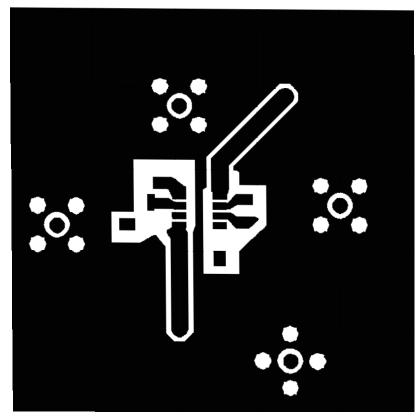
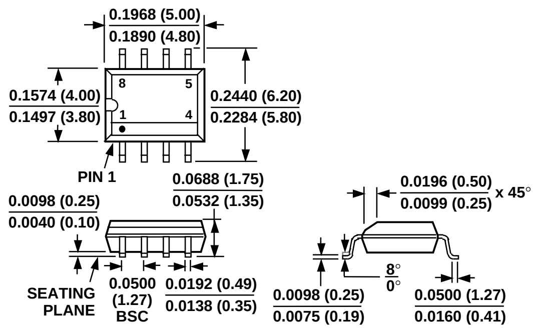


Figure 44. Universal SOIC Noninverter Bottom

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
(SO-8)



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