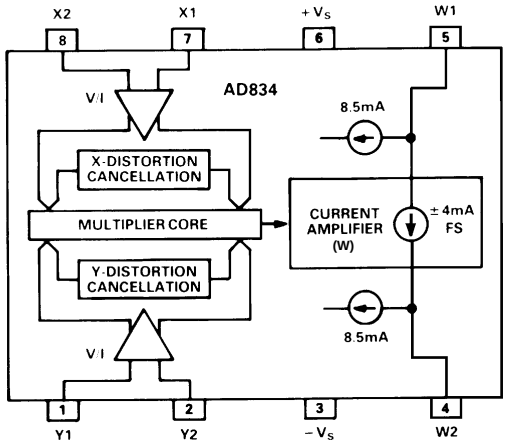
500 MHz Four-Quadrant Multiplier

AD834

FEATURES
DC to >500 MHz Operation
Differential ±1 V Full-Scale Inputs
Differential ±4 mA Full-Scale Output Current
Low Distortion (≤0.05% for 0 dBm Input)
Supply Voltages from ±4 V to ±9 V
Low Power (280 mW typical at V_S = ±5 V)

APPLICATIONS
High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L = 50 Ω) in excess of 500 MHz from either of the differential voltage inputs. In multiplier modes, the typical total full-scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X = Y = ±1 V, the differential output is ±4 mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0°C to +70°C and is available in an 8-pin DIP package and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of –40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of –55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

Two application notes featuring the AD834 (AN-212 and AN-216) can now be obtained by calling 1-800-ANALOG-D. For additional applications circuits consult the AD811 data sheet.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500 MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than –60 dB on either input) at high frequencies and low signal feedthrough (typically –65 dB up to 20 MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5 MHz and 0.8° at 50 MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500 ps, typically settling to within 1% in under 5 ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

REV. B

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AD834—SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5 V, unless otherwise noted; dBm assumes 50 Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4\,mA$			$W = \frac{XY}{(1V)^2} \times 4\,mA$		
Total Error[1] (Figure 6)	–1 V ≤ X, Y < +1 V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{MIN} to T_{MAX}					±1.5	**±3**	% FS
vs. Supplies[2]	±4 V to ±6 V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X = ±1 V, Y = Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X = Nulled, Y = ±1 V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X = 0 dBm, Y = Nulled							
	f = 10 MHz		–65			–65		dB
	f = 100 MHz		–50			–50		dB
AC Feedthrough, Y[5]	X = Nulled, Y = 0 dBm							
	f = 10 MHz		–70			–70		dB
	f = 100 MHz		–50			–50		dB
INPUTS (X1, X2, Y1, Y2)								
Full-Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{MIN} to T_{MAX}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4 V to ±6 V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common-Mode Rejection	f ≤ 100 kHz; 1 V p-p		70			70		dB
Nonlinearity, X	Y = 1 V; X = ±1 V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X = 1 V; Y = ±1 V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X = 0 dBm, Y = 1 V							
	f = 10 MHz		–60			–60		dB
	f = 100 MHz		–44			–44		dB
Distortion, Y	X = 1 V, Y = 0 dBm							
	f = 10 MHz		–65			–65		dB
	f = 100 MHz		–50			–50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X = 0, Y = 0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{MIN} to T_{MAX}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f = 10 Hz to 1 MHz Outputs into 50 Ω Load		16			16		nV/√Hz
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{MIN} to T_{MAX}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0°C to +70°C)			AD834J, JR-REEL					
Military (–55°C to +125°C)						AD834S		
Industrial (–40°C to +85°C)						AD834A		
PACKAGE OPTIONS								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTES

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f ≤ 10 kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full-scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ($+V_S$ to $-V_S$) . . . . . 18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $+V_S$
Operating Temperature Range
AD834J . . . . . 0°C to +70°C
AD834A . . . . . –40°C to +85°C
AD834S/883B . . . . . –55°C to +125°C
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Storage Temperature Range (R, N) . . . . . –65°C to +125°C
Lead Temperature (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 500 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
8-Pin Cerdip Package (Q)	30°C/W	110°C/W
8-Pin Plastic SOIC (R)	45°C/W	165°C/W
8-Pin Plastic Mini-DIP (N)	50°C/W	99°C/W

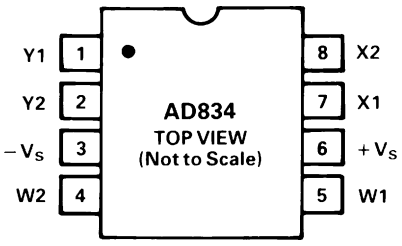
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD834JN	0°C to +70°C	N-8
AD834JR	0°C to +70°C	R-8
AD834JR-REEL	0°C to +70°C	R-8
AD834AQ	–40°C to +85°C	Q-8
AD834SQ/883B	–55°C to +125°C	Q-8
AD834S Chips		Chips

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC) Package.

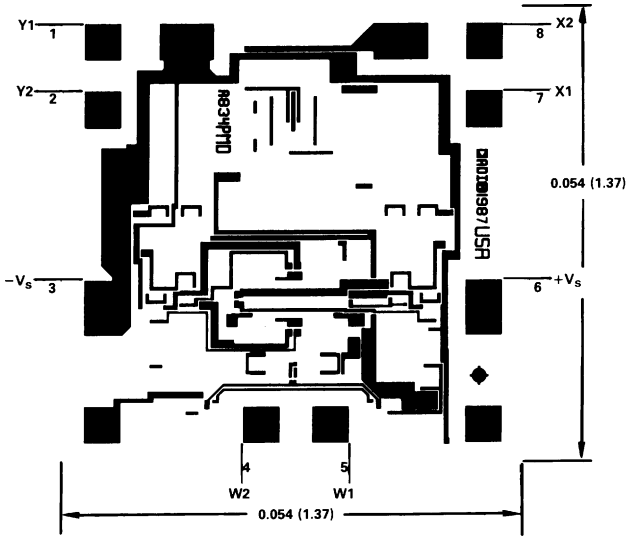
CONNECTION DIAGRAM

Small Outline (R) Package
Plastic DIP (N) Package
Cerdip (Q) Package



METALIZATION PHOTOGRAPH
CHIP DIMENSIONS AND BONDING DIAGRAM

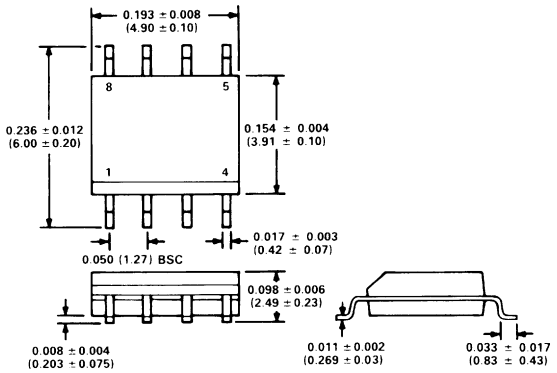
Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



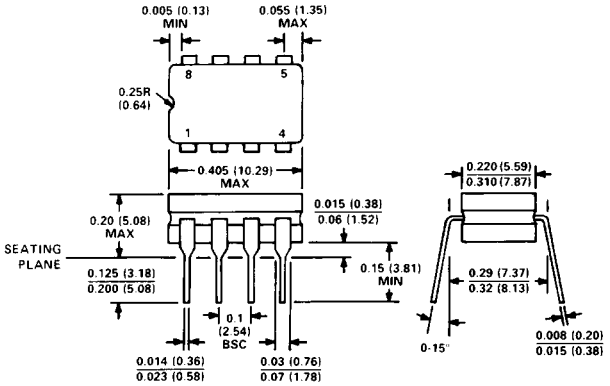
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Small Outline (R) Package



Cerdip (Q) Package



AD834–Typical Characteristics

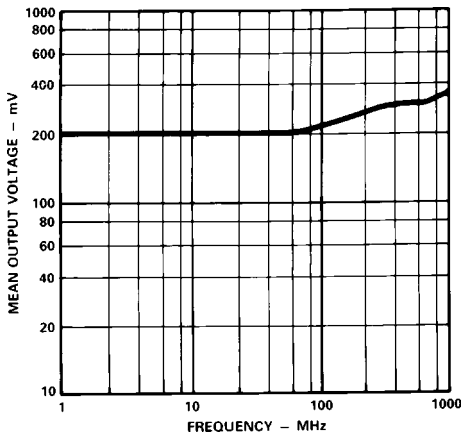


Figure 1. Mean-Square Output vs. Frequency

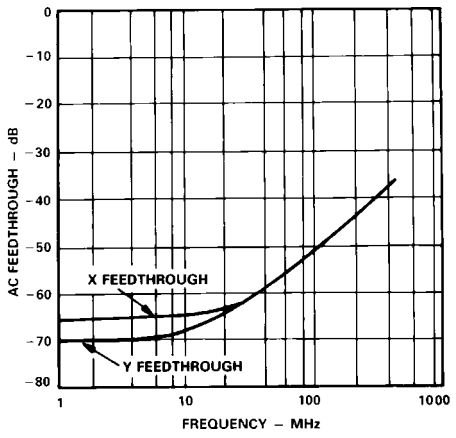


Figure 2. AC Feedthrough vs. Frequency

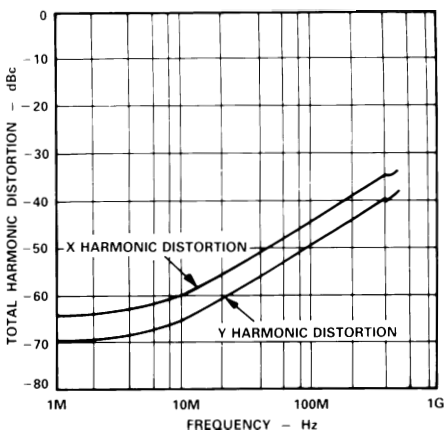


Figure 3. Total Harmonic Distortion vs. Frequency

Figure 1. Figure 1 is a plot of the mean-square output versus frequency for the test circuit of Figure 5. Note that the rising response is due to package resonances.

Figure 2. For frequencies above 1 MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out.

Figure 3. THD data represented in Figure 3 is dominated by the second harmonic, and is generated with 0 dBm input on the ac input and +1 V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude will affect THD performance.

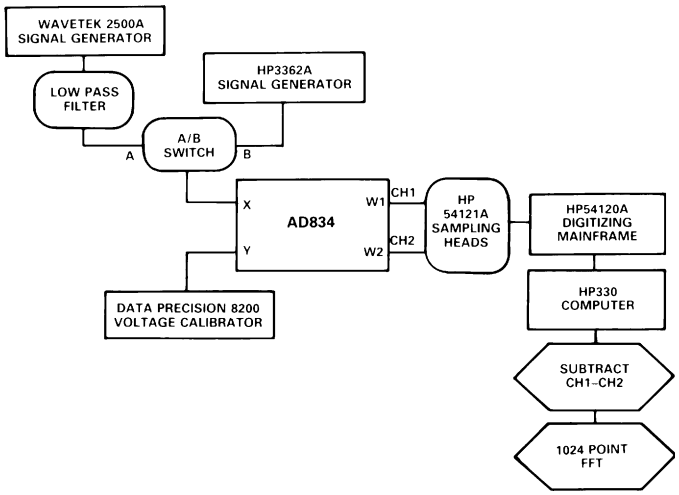


Figure 4. Test Configuration for Measuring AC Feedthrough and Total Harmonic Distortion

Figure 5. The squarer configuration shown in Figure 5 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing capacitors C3/C5 and C4/C6 across load resistors R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

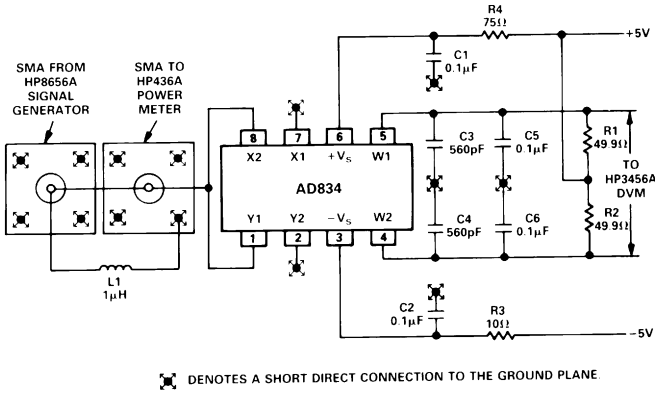


Figure 5. Bandwidth Test Circuit

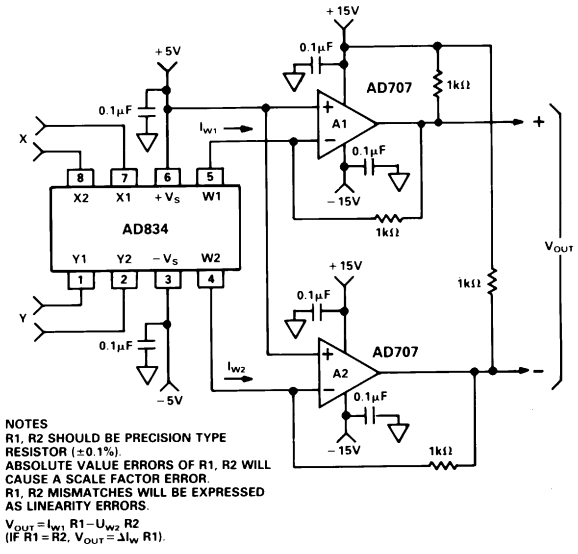


Figure 6. Low Frequency Test Circuit

BASIC OPERATION

Figure 7 is a functional equivalent of the AD834. There are three differential signal interfaces: the voltage inputs X = X1–X2 and Y = Y1–Y2, and the current output, W (see Figure 7) which flows in the direction shown when X and Y are positive. The outputs W1 and W2 each have a standing current of typically 8.5 mA.

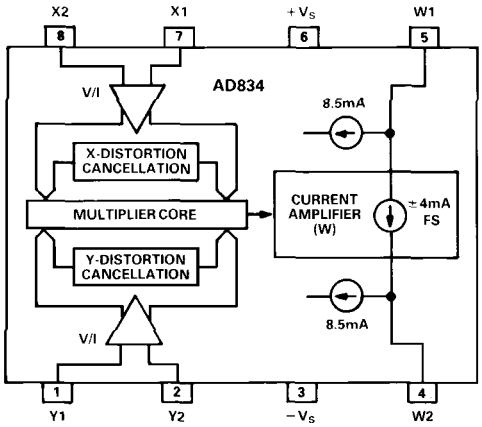


Figure 7. AD834 Functional Block Diagram

The input voltages are first converted to differential currents which drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285 Ω. This low value results in low input related noise and drift. However, the low full-scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits which operate by Kelvin sensing the voltages generated in the core—an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage which provides a current gain of nominally × 1.6, trimmed during manufacture to set up the full-scale output current of ±4 mA. **This output appears at a pair of open collectors which must be supplied with a voltage slightly above the voltage on Pin 6.** As shown in Figure 8, this can be arranged by inserting a resistor in series with the supply to this pin and taking the load resistors to the full supply. With R3 = 60 Ω, the voltage drop across it is about 600 mV. Using two 50 Ω load resistors, the full-scale differential output voltage is ±400 mV.

The full bandwidth potential of the AD834 can only be realized when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1 GHz, and the actual upper frequency in a typical application will usually be determined by the care with which the layout is effected. Note that R4 (in series with the $-V_S$ supply) carries about 30 mA and thus introduces a voltage drop of about 150 mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

Figure 8 shows the use of optional termination resistors at the inputs. Note that although the resistive component of the input

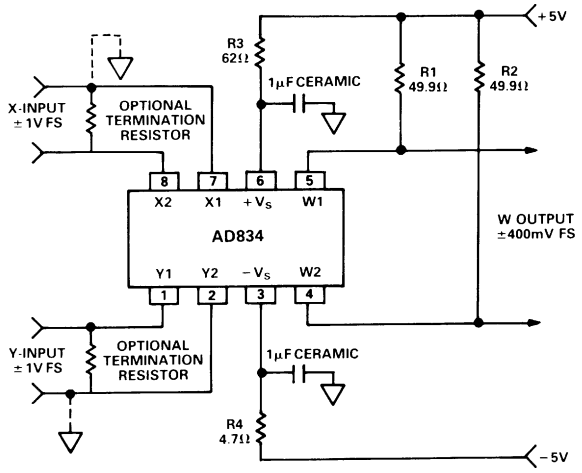


Figure 8. Basic Connections for Wideband Operation

impedance is quite high (about 25 kΩ), the input bias current of typically 45 μA can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50 Ω (net source of 25 Ω) the offset would be 25 Ω × 45 μA = 1.125 mV. This can be almost fully cancelled by including (in this example) another 25 Ω resistor in series with the "unused" input (in Figure 8, either X1 or Y2). In order to minimize crosstalk the input pins closest to the output (X1 and Y2) should be grounded; the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

TRANSFER FUNCTION

The output current W is the linear product of input voltages X and Y divided by $(1\ V)^2$ and multiplied by the "scaling current" of 4 mA:

$$W = \frac{XY}{(1V)^2} 4\,mA$$

Provided that it is understood that the inputs are specified in *volts*, a simplified expression can be used:

$$W = (XY)\,4\,mA$$

Alternatively, the full transfer function can be written:

$$W = \frac{XY}{1V} \times \frac{1}{250\,\Omega}$$

When both inputs are driven to their clipping level of about 1.3 V, the peak output current is roughly doubled, to ±8 mA, but distortion levels will then be very high.

TRANSFORMER COUPLING

In many high frequency applications where baseband operation is not required at either inputs or output, transformer coupling can be used. Figure 9 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

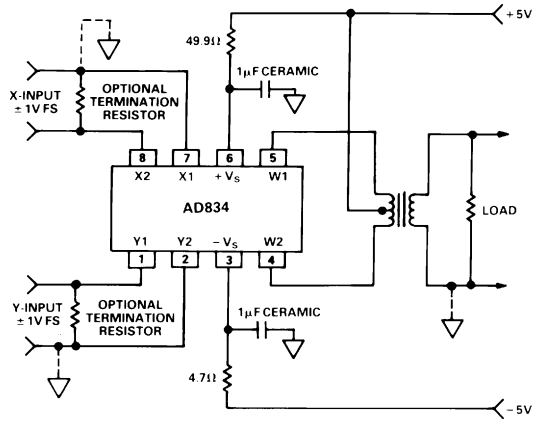


Figure 9. Transformer—Coupled Output

A particularly effective type of transformer is the balun[1] which is a short length of transmission line wound on to a toroidal ferrite core. Figure 10 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (hence the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line (although this will usually not be critical for short line lengths). The collector load resistors R_C may also be chosen to reverse terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

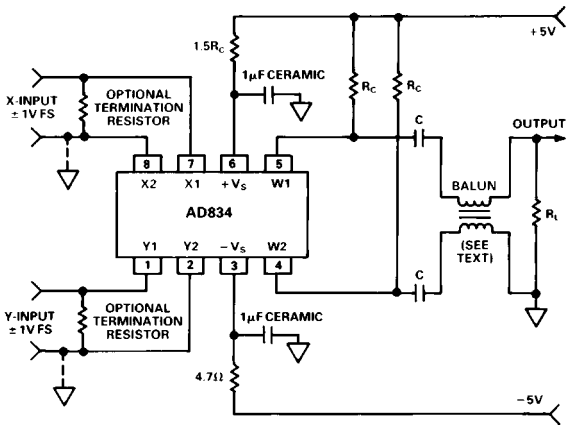


Figure 10. Using a Balun at the Output

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the *series* inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

[1]For a good treatment of baluns, see "Transmission Line Transformers" by Jerry Sevick; American Radio Relay League publication.

WIDEBAND MULTIPLIER CONNECTIONS

Where operation down to dc and a ground based output are necessary, the configuration shown in Figure 11 can be used. The element values were chosen in this example to result in a full-scale output of ±1 V at the load, so the overall multiplier transfer function is

$$W = (X1–X2)\,(Y1–Y2)$$

where it is understood that the *inputs and output are in volts.* The polarity of the output can be reversed simply by reversing either the X or Y input.

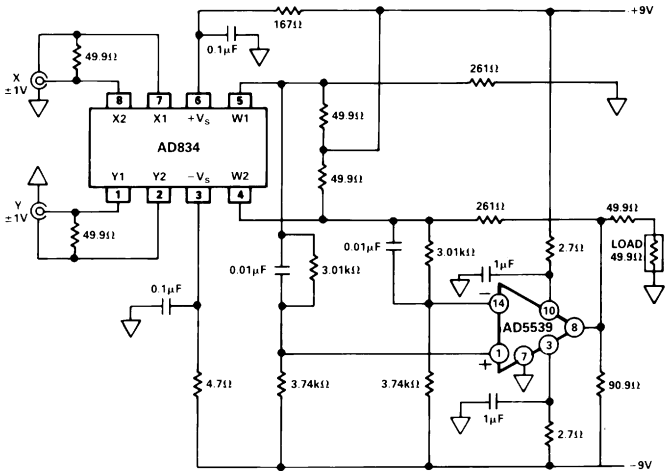


Figure 11. Sideband DC-Coupled Multiplier

The op amp should be chosen to support the desired output bandwidth. The AD5539 is shown here, providing an overall system bandwidth of 100 MHz. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset may be nulled by including a 100 Ω trim pot between each of the lower pair of resistors (3.74 kΩ) and the negative supply.

The pulse response for this circuit shown in Figure 12; the X input was a pulse of 0 V to +1 V and the Y input was +1 V dc. The transition times at the output are about 4 ns.

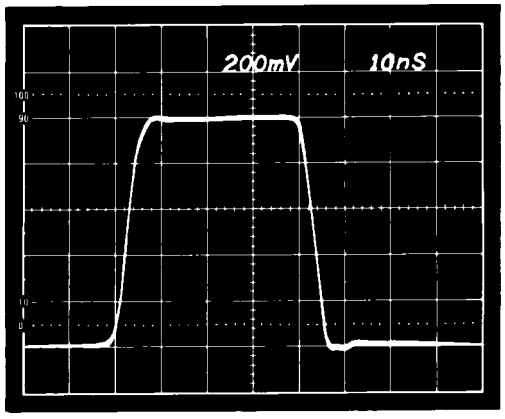


Figure 12. Pulse Response for the Circuit of Figure 11

POWER MEASUREMENT (MEAN SQUARE AND RMS)

The AD834 is well suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the V × I product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low-pass filter to extract the long term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, since the following active circuitry is required to process only low frequency signals.

(Refer to Figure 5 test configuration.) Using the device as a squarer the wideband output in response to a sinusoidal stimulus is a raised cosine:

$$\sin^2 \omega t = (1 + \cos 2\omega t)/2$$

Recall here that the full-scale output current (when full-scale input voltages of 1 V are applied to both X and Y) is 4 mA. In a 50 Ω system, a sinusoid power of +10 dBm has a peak value of 1 V. Thus, at this drive level the peak output voltage across the differential 50 Ω load in the absence of the filter capacitors would be 400 mV (that is, 4 mA × 50 Ω × 2), whereas the average value of the raised cosine is only 200 mV. The averaging configuration is useful in evaluating the bandwidth of the AD834, since a dc voltage is easier to measure than a wideband, differential output. In fact, the squaring mode is an even more critical test than the direct measurement of the bandwidth of either channel taken independently (with a dc input on the nonsignal channel), because the phase relationship between the two channels also affects the average output. For example, a time delay difference of only 250 ps between the X and Y channels would result in zero output when the input frequency is 1 GHz, at which frequency the phase angle is 90 degrees and the intrinsic product is now between a sine and cosine function, which has zero average value.

The physical construction of the circuitry around the IC is critical to realizing the bandwidth potential of the device. The input is supplied from an HP8656A signal generator (100 kHz to 990 MHz) via an SMA connector and terminated by an HP436A power meter using an HP8482A sensor head connected via a second SMA connector. Since neither the generator nor the sensor provide a dc path to ground, a lossy 1 μH inductor L1, formed by a 22-gauge wire passing through a ferrite bead (Fair-Rite type 2743001112) is included. This provides adequate impedance down to about 30 MHz. The IC socket is mounted on a ground plane, with a clear area in the rectangle formed by the pins. This is important, since significant transformer action can arise if the pins pass through individual holes in the board; this has been seen to cause an oscillation at 1.3 GHz in improperly constructed test jigs. The filter capacitors must be connected directly to the same point on the ground plane via the shortest possible leads. Parallel combinations of large and small capacitors are used to minimize the impedance over the full frequency range. (Refer to Figure 1 for mean-square response for the AD834 in cerdip package, using the configuration of Figure 5.)

To provide a square-root response and thus generate the rms value at the output, a second AD834, also connected as a squarer, can be used, as shown in Figure 13. Note that an attenuator is inserted both in the signal input and in the feedback path to the second AD834. This increases the maximum input capability to +15 dBm and improves the response flatness by damping some of the resonances. The overall gain is unity; that is, the output voltage is exactly equal to the rms value of the input signal. The offset potentiometer at the AD834 outputs extends the dynamic range, and is adjusted for a dc output of 125.7 mV when a 1 MHz sinusoidal input at –5 dBm is applied.

Additional filtering is provided; the time constants were chosen to allow operation down to frequencies as low as 1 kHz and to provide a critically damped envelope response, which settles typically within 10 ms for a full-scale input (and proportionally slower for smaller inputs). The 5 μF and 0.1 μF capacitors may be scaled down to reduce response time if accurate rms operation at low frequencies is not required. The output op amp must be specified to accept a common-mode input near its supply. Note that the output polarity may be inverted by replacing the NPN transistor with a PNP type.

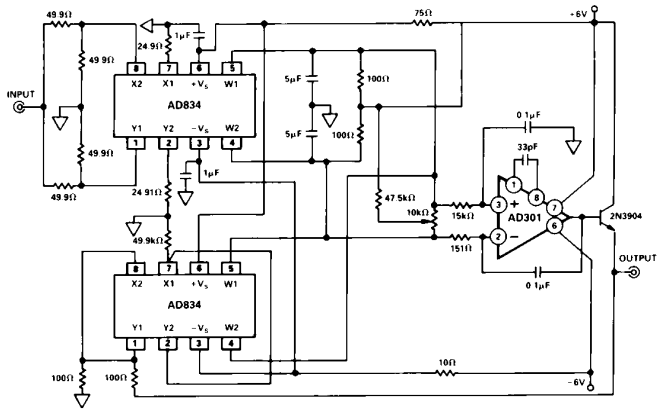


Figure 13. Connections for Wideband RMS Measurement

FREQUENCY DOUBLER

Figure 14 shows another squaring application. In this case, the output filter has been removed and the wideband differential output is converted to a single sided signal using a "balun," which consists of a length of 50 Ω coax cable fed through a ferrite core (Fair-Rite type 2677006301). No attempt is made to reverse terminate the output. Higher load power could be achieved by replacing the 50 Ω load resistors by ferrite bead inductors. The same precautions should be observed with regard to PC board layout as recommended above. The output spectrum shown in Figure 15 is for an input power of +10 dBm at a frequency of 200 MHz. The second harmonic component at 400 MHz has an output power of –15 dBm. Some feedthrough of the fundamental occurs: it is 15 dBs below the main output. It is believed that improvements in the design of the balun would reduce this feedthrough. A spurious output at 600 MHz is also present, but it is 30 dBs below the main output. At an input frequency of 100 MHz, the measured power level at 200 MHz is –16 dBm, while the fundamental feedthrough is reduced to 25 dBs below the main output; at an output of 600 MHz the power is –11 dBm and the third harmonic at 900 MHz is 32 dBs below the main output.

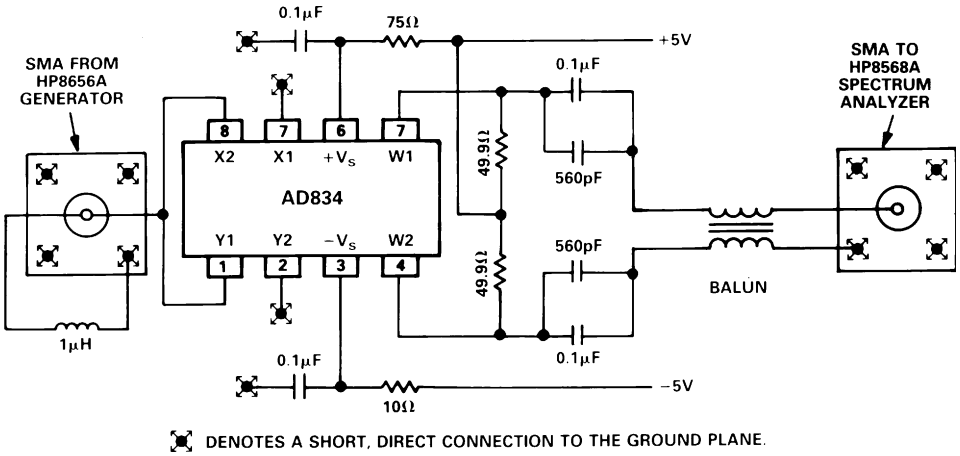


Figure 14. Frequency Doubler Connections

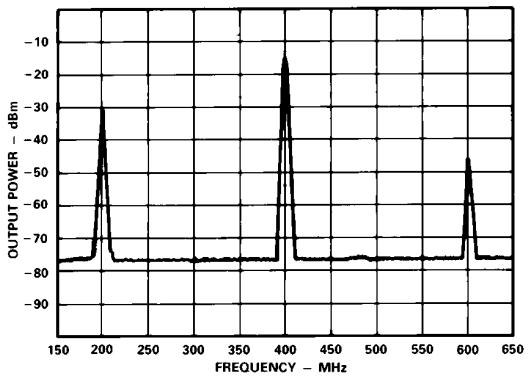


Figure 15. Output Spectrum for Configuration of Figure 14

WIDEBAND THREE SIGNAL MULTIPLIER/DIVIDER

Two AD834s and a wideband op amp can be connected to make a versatile multiplier/divider having the transfer function

$$W = \frac{(X1 - X2)(Y1 - Y2)}{(U1 - U2)} + Z$$

with a denominator range of about 100:1. The denominator input U = U1–U2 must be positive and in the range 100 mV to 10 V; X, Y and Z inputs may have either polarity. Figure 16 shows a general configuration which may be simplified to suit a particular application. This circuit accepts full-scale input voltages of 10 V, and delivers a full-scale output voltage of 10 V. The optional offset trim at the output of the AD834 improves the accuracy for small denominator values. It is adjusted by nulling the output voltage when the X and Y inputs are zero and U = +100 mV.

The AD840 is internally compensated to be stable without the use of any additional HF compensation. As the input U is reduced, the bandwidth falls because the feedback around the op amp is proportional to the input U.

This circuit may be modified in several ways. For example, if the differential input feature is not needed, the unused input

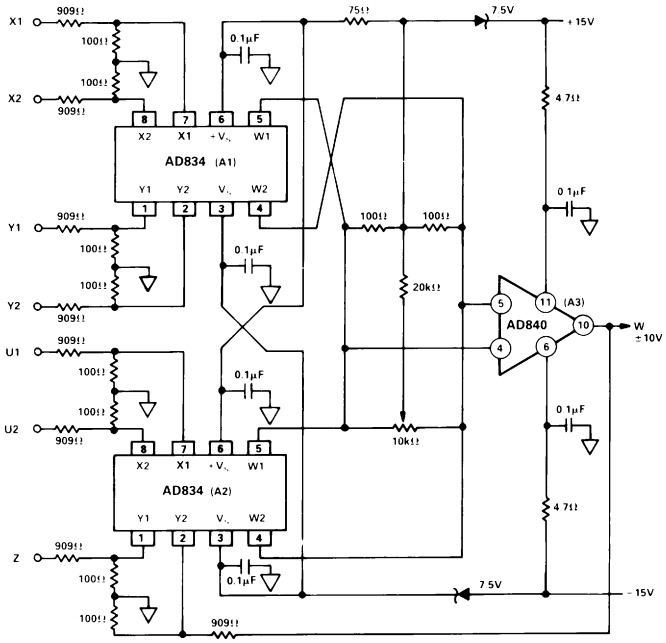


Figure 16. Wideband Three Signal Multiplier/Divider

can be connected to ground through a single resistor, equal to the parallel sum of the resistors in the attenuator section. The full-scale input levels on X, Y and U can be adapted to any full-scale voltage down to ±1 V by altering the attenuator ratios. Note, however, that precautions must be taken if the attenuator ratio from the output of A3 back to the second AD834 (A2) is lowered. First, the HF compensation limit of the AD840 may be exceeded if the negative feedback factor is too high. Second, if the attenuated output at the AD834 exceeds its clipping level of ±1.3 V, feedback control will be lost and the output will suddenly jump to the supply rails. However, with these limitations understood, it will be possible to adapt the circuit to smaller full-scale inputs and/or outputs, and for use with lower supply voltages.

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