12–Bit, 20/40/65 MSPS 3 V A/D Converter

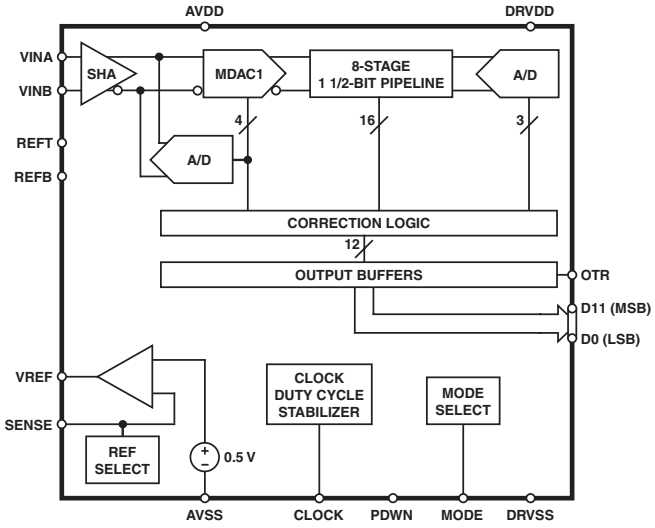
Preliminary Technical Data 1/19/01 AD9235

FEATURES

SNR = 70.4dBc (to Nyquist)
SFDR = 92dBc @ 2.4MHz Analog Input
84dBc @ 32.5MHz Analog Input
DNL = ± 0.4lsb
Low Power: 330 mW at 65 MSPS (to Nyquist)
Differential Input with 500 MHz Bandwidth
On–Chip Reference and SHA
Flexible Analog Input: 1 Vp-p to 2 Vp-p Range
Single 3 V Supply Operation (2.7 V to 3.6 V)
Offset Binary or Two's Complement data format
Clock Duty Cycle Stabilizer

APPLICATIONS

Ultrasound Equipment
IF Sampling in Communications Receivers
IS-95, CDMA-one, IMT-2000
Battery Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes



PRODUCT DESCRIPTION

The AD9235 is a monolithic, single 3 V supply, 12-bit, 65MSPS Analog to Digital Converter with a high performance sample-and-hold amplifier and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 65MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows for a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available analog to digital converters, the AD9235 is suitable for applications in communications, imaging and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A Duty Cycle Stabilizer compensates for wide variations in the Clock duty cycle while maintaining excellent performance. The digital output data is presented in straight binary or two's complement formats. An out-of-range signal indicates an overflow condition, which can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-pin surface mount plastic package and is specified over the industrial temperature range (-40°C to +85°C).

PRODUCT HIGHLIGHTS

1. The AD9235 operates from a single 3 V power supply, and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 330 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 500MHz, and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214, a 10-bit, 65/80/105 MSPS A/D Converter.
5. The Clock Duty Cycle Stabilizer maintains performance over a wide range of Clock pulsewidths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

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DC SPECIFICATIONS (AVDD = +3 V, DRVDD = +2.5, 2V p-p Input, 1.0V external reference, T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Temp	Test Level	AD9235BRU-20			AD9235BRU-40			AD9235BRU-65			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	V		±0.01			±0.01			±0.01		% FSR
	25°C	I			TBD			TBD			TBD	% FSR
Gain Error	Full	V		±0.03			±0.03			±0.03		% FSR
	25°C	I			TBD			TBD			TBD	% FSR
Differential Nonlinearity (DNL)[2]	Full	VI	TBD	±0.4	TBD	TBD	±0.4	TBD	TBD	±0.4	TBD	LSB
Integral Nonlinearity (INL)[2]	Full	VI	TBD	±1.0	TBD	TBD	±1.0	TBD	TBD	±1.0	TBD	LSB
TEMPERATURE DRIFT												
Zero Error	Full	V		± 2			± 2			± 2		ppm/°C
Gain Error[1]	Full	V		TBD			TBD			TBD		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage (1 V Mode)	Full	V	TBD	1.0	TBD	TBD	1.0	TBD	TBD	1.0	TBD	V
Load Regulation @ 1 mA	Full	V		0.8			0.8			0.8		mV
	25°C	I			TBD			TBD			TBD	mV
Output Voltage (0.5 V Mode)	Full	V		0.5			0.5			0.5		V
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	Full	V		0.54			0.54			0.54		LSB rms
VREF = 1.0 V	Full	V		0.27			0.27			0.27		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5 V	Full	V		1			1			1		V p-p
Input Span, VREF = 1.0 V	Full	V		2			2			2		V p-p
Input Capacitance	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		5			5			5		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	V	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	V	2.5	3.0	3.6	2.5	3.0	3.6	2.5	3.0	3.6	V
Supply Currents												
IAVDD[2]	Full	V		32			58			104		mA
	25°C	I		31	TBD		56	TBD		101	TBD	mA
IDRVDD[2]	Full	V		2			4			5		mA
	25°C	I		2	TBD		4	TBD		5	TBD	mA
PSRR	Full	V		± 0.025			± 0.025			± 0.025		% FSR
	25°C	I		± 0.0015	TBD		± 0.0015	TBD		± 0.0015	TBD	% FSR
POWER CONSUMPTION												
DC Input[3]	Full	V		96			173			312		mW
	25°C	I		93	TBD		168	TBD		303	TBD	mW
Sine Wave Input[2]	Full	V		102			185			327		mW
	25°C	I		101	TBD		180	TBD			TBD	mW
Stand-By Power	Full	V		2.0			2.0			2.0		mW
	25°C	I		1.2	TBD		1.2	TBD		1.2	TBD	mW

NOTES

1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0V external reference).
2. Measured at Maximum Clock Rate, F_{IN} = 2.4 MHz with approximately 5 pF loading on each output bit.
3. Measured with DC input at Maximum Clock Rate.

DIGITAL SPECIFICATIONS (AVDD = +3 V, DRVDD = +2.5 V, 2V p-p Input, 1.0V external reference, T_{MIN} to T_{MAX}, unless otherwise noted)

			AD9235BRU-20			AD9235BRU-40			AD9235BRU-65			
Parameter	**Temp**	**Test Level**	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	**Units**
LOGIC INPUTS												
High-Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low-Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High-Level Input Current	Full	IV	-10		10	-10		10	-10		10	µA
Low-Level Input Current	Full	IV	-10		10	-10		10	-10		10	µA
Input Capacitance	Full	IV		5			5			5		pF
LOGIC OUTPUTS												
DRVDD = 3.3 V												
High-Level Output Voltage (I_{OH} = 50 µA)	Full	IV	3.29			3.29			3.29			V
High-Level Output Voltage (I_{OH} = 0.5 mA)	Full	IV	3.25			3.25			3.25			V
Low-Level Output Voltage (I_{OL} = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (I_{OL} = 50 µA)	Full	IV			0.05			0.05			0.05	V
DRVDD = 2.5 V												
High-Level Output Voltage (I_{OH} = 50 µA)	Full	IV	2.49			2.49			2.49			V
High-Level Output Voltage (I_{OH} = 0.5 mA)	Full	IV	2.45			2.45			2.45			V
Low-Level Output Voltage (I_{OL} = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (I_{OL} = 50 µA)	Full	IV			0.05			0.05			0.05	V

SWITCHING SPECIFICATIONS (AVDD = +3 V, DRVDD = +2.5 V, 2V p-p Input, 1.0V external reference, T_{MIN} to T_{MAX}, unless otherwise noted)

			AD9235BRU-20			AD9235BRU-40			AD9235BRU-65			
Parameter	**Temp**	**Test Level**	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	**Units**
SWITCHING PERFORMANCE												
Max Conversion Rate	Full	VI	20			40			65			MSPS
Min Conversion Rate	Full	V			5			5			5	MSPS
CLOCK Period	Full	V	50.0			25.0			15.4			ns
CLOCK Pulsewidth High	Full	V	15.0			8.8			6.2			ns
CLOCK Pulsewidth Low	Full	V	15.0			8.8			6.2			ns
Valid Data Delay[2]	Full	V		3.5			3.5			3.5		ns
Pipeline Delay(Latency)	Full	V		7			7			7		Cycles
Wake-Up Time[3]	Full	V		3			3			3		ms

NOTES:

1. Output Voltage Levels measured with 5pF load on each output.
2. Valid Data Delay is measured from CLOCK 50% transition to DATA 50% transition, with 5pF load.
3. Wake-Up Time is dependant on value of decoupling capacitors, typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

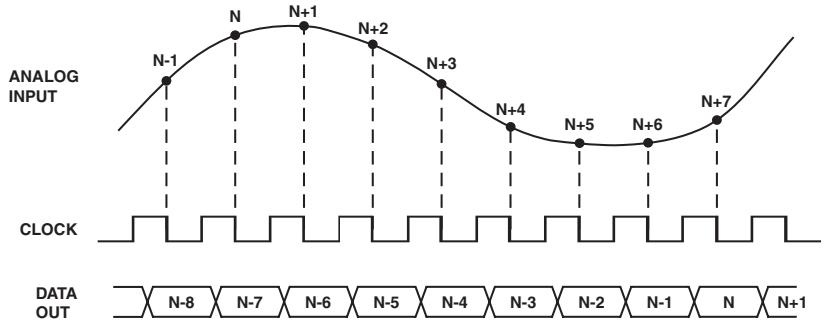


Figure 1. Timing Diagram

AC SPECIFICATIONS (AVDD = +3 V, DRVDD = +2.5 V, 2V p-p Input, 1.0V external reference, T_{MIN} to T_{MAX}, DCS off, unless otherwise noted)

			AD9235BRU-20			AD9235BRU-40			AD9235BRU-65			
Parameter	**Temp**	**Test Level**	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	**Units**
SIGNAL-TO-NOISE RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		70.8			70.6			70.5		dBc
f_{INPUT} = 9.7 MHz	Full	VI	TBD	TBD			TBD			TBD		dBc
	25°C	I	TBD	70.6			70.5			70.3		dBc
f_{INPUT} = 19.6 MHz	Full	VI		TBD		TBD	TBD			TBD		dBc
	25°C	I		70.6		TBD	70.4			70.2		dBc
f_{INPUT} = 32.5 MHz	Full	VI		TBD			TBD		TBD	TBD		dBc
	25°C	I		70.5			70.4		TBD	70.4		dBc
f_{INPUT} = 100 MHz	25°C	V		68.6			68.4			68.3		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		70.6			70.7			70.4		dBc
f_{INPUT} = 9.7 MHz	Full	VI	TBD	TBD			TBD			TBD		dBc
	25°C	I	TBD	70.6			70.5			70.3		dBc
f_{INPUT} = 19.6 MHz	Full	VI		TBD		TBD	TBD			TBD		dBc
	25°C	I		70.4		TBD	70.3			70.0		dBc
f_{INPUT} = 32.5 MHz	Full	VI		TBD			TBD		TBD	TBD		dBc
	25°C	I		70.3			70.2		TBD	69.8		dBc
f_{INPUT} = 100 MHz	25°C	V		68.6			68.3			67.8		dBc
TOTAL HARMONIC DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		-90.0			-88.0			-88.0		dBc
f_{INPUT} = 9.7 MHz	Full	VI		TBD	TBD		TBD			TBD		dBc
	25°C	I		-89.0	TBD		-88.0			-86.0		dBc
f_{INPUT} = 19.6 MHz	Full	VI		TBD			TBD	TBD		TBD		dBc
	25°C	I		-86.0			-86.0	TBD		-86.0		dBc
f_{INPUT} = 32.5 MHz	Full	VI		TBD			TBD			TBD	TBD	dBc
	25°C	I		-85.0			-86.0			-82.0	TBD	dBc
f_{INPUT} = 100 MHz	25°C	V		-82.0			-83.0			-78.0		dBc
WORST HARMONIC (2^{nd} or 3^{rd})												
f_{INPUT} = 9.7 MHz	Full	VI		TBD	TBD							dBc
f_{INPUT} = 19.6 MHz	Full	VI					TBD	TBD				dBc
f_{INPUT} = 32.5 MHz	Full	VI								TBD	TBD	dBc
SPURIOUS FREE DYNAMIC RANGE												
f_{INPUT} = 2.4 MHz	25°C	V		94.0			94.0			92.0		dBc
f_{INPUT} = 9.7 MHz	Full	VI	TBD	TBD			TBD			TBD		dBc
	25°C	I	TBD	93.0			94.0			91.0		dBc
f_{INPUT} = 19.6 MHz	Full	VI		TBD		TBD	TBD			TBD		dBc
	25°C	I		88.0		TBD	90.0			90.0		dBc
f_{INPUT} = 32.5 MHz	Full	VI		TBD			TBD		TBD	TBD		dBc
	25°C	I		87.0			88.0		TBD	84.0		dBc
f_{INPUT} = 100 MHz	25°C	V		84.0			85.0			80.0		dBc

ABSOLUTE MAXIMUM RATINGS[1]

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AVSS	-0.3	+3.9	V
DRVDD	DRVSS	-0.3	+3.9	V
AVSS	DRVSS	-0.3	+0.3	V
AVDD	DRVDD	-3.9	+3.9	V
Digital Outputs	DRVSS	-0.3V	DRVDD +0.3	V
CLOCK, MODE	AVSS	-0.3V	AVDD +0.3	V
VINA, VINB	AVSS	-0.3V	AVDD +0.3	V
VREF	AVSS	-0.3V	AVDD +0.3	V
SENSE	AVSS	-0.3V	AVDD +0.3	V
REFB, REFT	AVSS	-0.3V	AVDD +0.3	V
PDWN	AVSS	-0.3V	AVDD +0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		-45	85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		–65	150	°C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Typical thermal impedances (28-terminal TSSOP); θ_{JA} = 97.9°C/W; θ_{JC} = 14 °C/W. These measurements were taken on a 2-layer board in still air, in accordance with EIA/JESD51-3.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

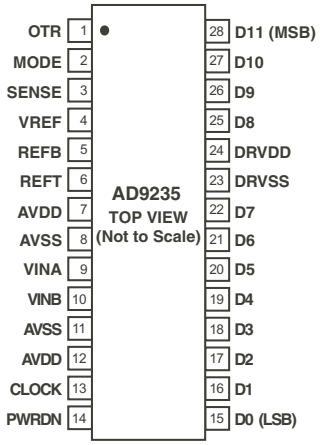
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9235BRU-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU–28
AD9235BRU-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU–28
AD9235BRU-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU–28
AD9235/PCB		Evaluation Board	

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	OTR	Out of Range indicator.
2	MODE	Data format and clock duty cycle stabilizer mode selection.
3	SENSE	Reference mode selection.
4	VREF	Voltage Reference Input/Output.
5	REFB	Differential Reference (Negative).
6	REFT	Differential Reference (Positive).
7, 12	AVDD	Analog Power Supply.
8, 11	AGND	Analog ground.
9	VINA	Analog Input Pin (+).
10	VINB	Analog Input Pin (-).
13	CLOCK	Clock Input Pin.
14	PDWN	Power-Down function selection.
23	DRGND	Digital output ground.
24	DRVDD	Digital Output Driver Supply.
15-22, 25-28	D0 (LSB) – D11 (MSB)	Data Output Bits.

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at TMIN or TMAX.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as noise on the input to the ADC.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to obtain a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

CLOCK PULSEWIDTH AND DUTY CYCLE

Pulsewidth high is the minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance: pulse width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specs define an acceptable clock duty cycle.

MINIMUM CONVERSION RATE

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

MAXIMUM CONVERSION RATE

The clock rate at which parametric testing is performed.

OUTPUT PROPAGATION DELAY

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

TWO TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

EQUIVALENT CIRCUITS

TBD

Figure 2. Equivalent Analog Input Circuit

TBD

Figure 3. Equivalent Reference Input Circuit

TBD

Figure 4. Equivalent Clock Input Circuit

TBD

Figure 5. Equivalent Digital Output Circuit

TBD

Figure 6. Equivalent Reference Output Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

(AVDD = +3 V, DRVDD = +2.5 V, 2V p-p Input, 1.0V external reference, T_A = 25°C, unless otherwise noted)

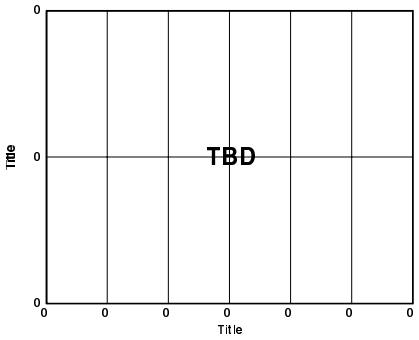


Figure 7. Spectrum: FS = 100 MSPS, f_{INPUT} = 10 MHz

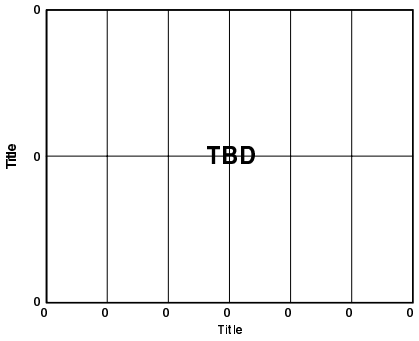


Figure 8. Two tone Intermodulation Distortion

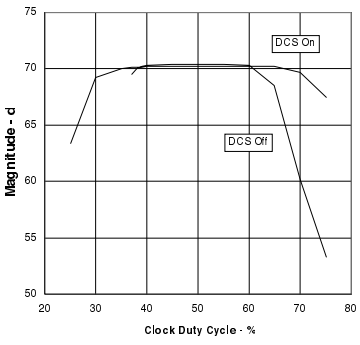


Figure 9. SNR vs. Clock Duty Cycle

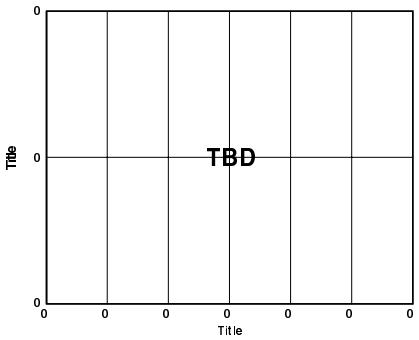


Figure 10. Spectrum: FS = 100 MSPS, f_{INPUT} = 40 MHz

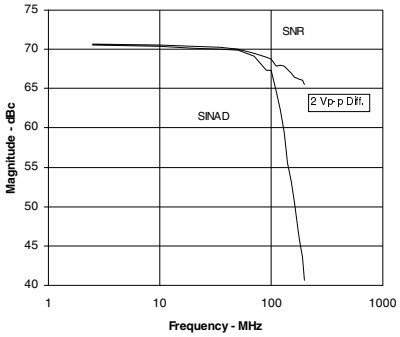


Figure 11. SINAD/SNR vs. f_{INPUT}

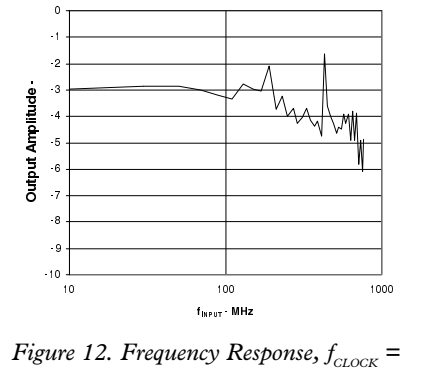


Figure 12. Frequency Response, f_{CLOCK} = 65 MSPS

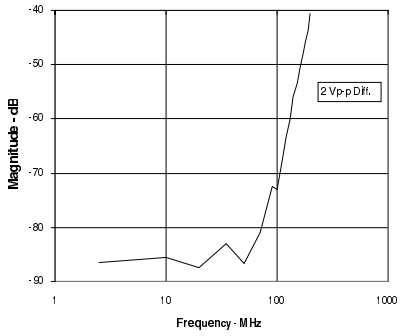


Figure 13. Harmonic Distortion vs. f_{INPUT}

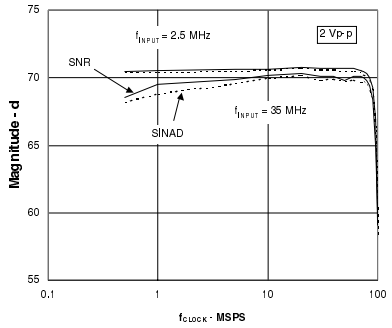


Figure 14. SINAD/SNR vs. Clock Rate

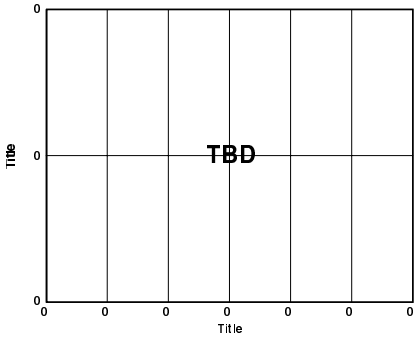


Figure 15. Analog Power Dissipation vs. Clock Rate

TYPICAL PERFORMANCE CHARACTERISTICS

(AVDD = +3 V, DRVDD = +2.5 V, 2V p-p Input, 1.0V external reference, T_A = 25°C, unless otherwise noted)

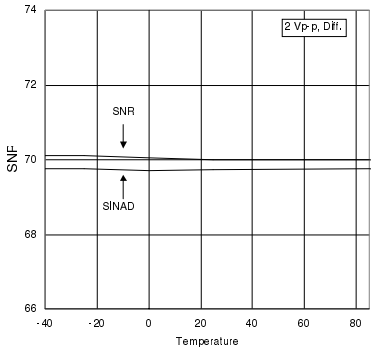


Figure 16. SINAD/SNR vs. Temperature

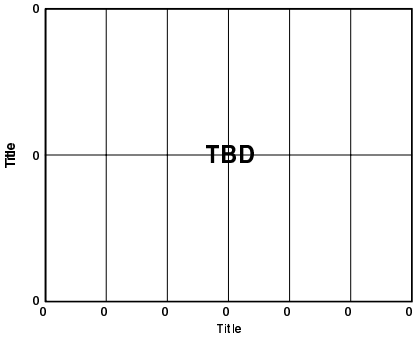


Figure 17. ADC Gain vs. Temperature (with External 2 V Reference)

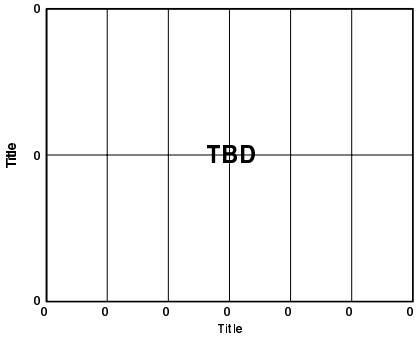


Figure 18. TBD

APPLYING THE AD9235

THEORY OF OPERATION

The AD9235 architecture consists of a front-end Sample and Hold Amplifier (SHA) followed by a pipelined switched capacitor A/D converter. The pipelined A/D converter is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The input stage contains a differential SHA that can be configured as AC or DC coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction and passes the data to the output buffers. The output buffers are powered from a separate supply allowing adjustment of the output voltage swing. During power-down the output buffers go into a high impedance state.

OPERATIONAL MODES

The AD9235 contains a multi-level mode selection pin that establishes the output data format and enables or disables the Clock Duty Cycle Stabilizer (DCS). The input threshold values and corresponding mode selections are outlined in Table I.

Table I. Mode Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Two's Complement	Disabled
2/3 AVDD	Two's Complement	Enabled
1/3 AVDD	Binary	Enabled
AVSS (default)	Binary	Disabled

The MODE pin is internally pulled down to AVSS (Binary Data Format, DCS Disabled) if left floating.

ANALOG INPUT

The analog input to the AD9235 is a differential SHA. It may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The maximum and minimum input voltage values are determined by AVDD and VREF as follows:

$$V_{MIN} = VREF/2, \text{ and}$$

$$V_{MAX} = (AVDD + VREF)/2.$$

For best dynamic performance, impedances at VINA and VINB should match.

Alternatively, the input may be driven into VINA or VINB from a single-ended source. The input span will be twice the programmed reference voltage. One input will accept the signal, while the opposite input will be set to mid-scale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VINA while a 1 V reference is applied to VINB. The AD9235 will then accept a signal varying between 2 V and 0 V.

CLOCK INPUT AND CONSIDERATIONS

Typical high-speed A/D converters use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9235 contains a Clock Duty Cycle Stabilizer that retimes the non-sampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of Clock input duty cycles without affecting the performance of the AD9235.

High-speed, high-resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$\text{SNR degradation} = 20 \log10 [1/2 \pi f_{INPUT} t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and A/D aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

The Clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9235. Power supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing or other methods), it should be retimed by the original clock at the last step.

DIGITAL OUTPUTS

The AD9235 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

As detailed above, the data format can be selected for either offset binary or two's complement. During power down, the outputs transition to a high impedance state. It takes approximately one millisecond after disabling power down to restore full operation.

TIMING

The AD9235 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 1 for a detailed timing diagram.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9235; these transients can detract from the converter's dynamic performance.

The lowest typical conversion rate of the AD9235 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9235. The input range can be adjusted by varying the reference voltage applied to the AD9235, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

INTERNAL REFERENCE CONNECTION

A comparator within the AD9235 detects the potential at the VREF pin. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 19), setting VREF to 1 V.

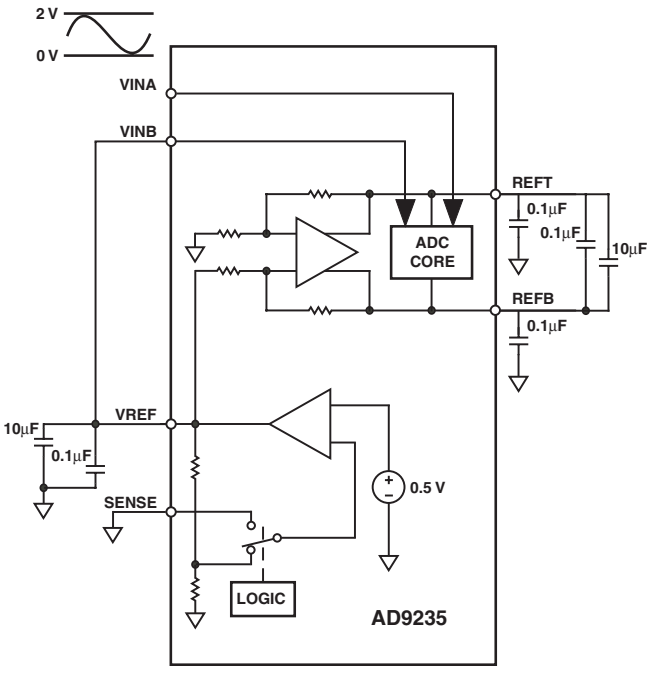


Figure 19. Internal Reference Operation, 2 V Span, Single-Ended Input

If SENSE is tied to VREF, the switch is connected to SENSE and the reference voltage will be 0.5 V (Figure 20). In all reference configurations, REFT and REFB drive the ADC conversion core and establish its maximum and minimum span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

If resistors are placed between VREF, SENSE and ground (as shown in Figure 21), the switch is again set to the SENSE position and the reference amplitude depends on the external programming resistors. Therefore, in this mode the reference must be limited to a maximum of 1V.

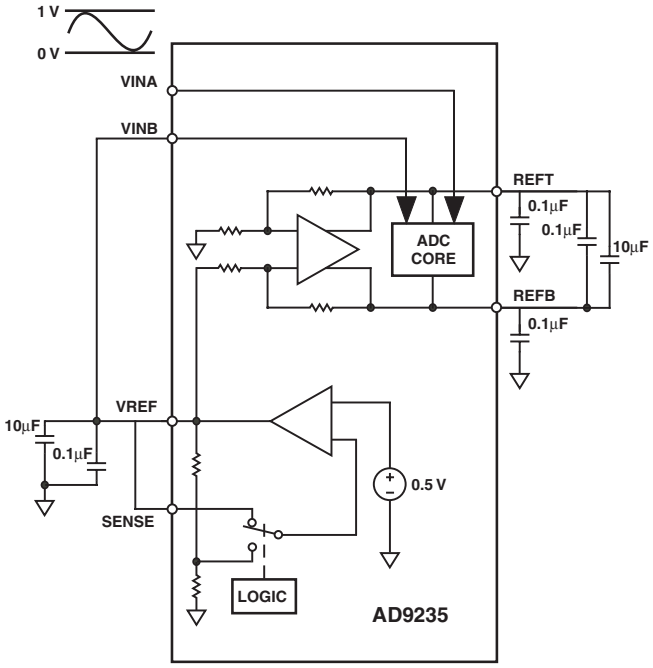


Figure 20. Internal Reference Operation, 1 V Span, Single-Ended Input

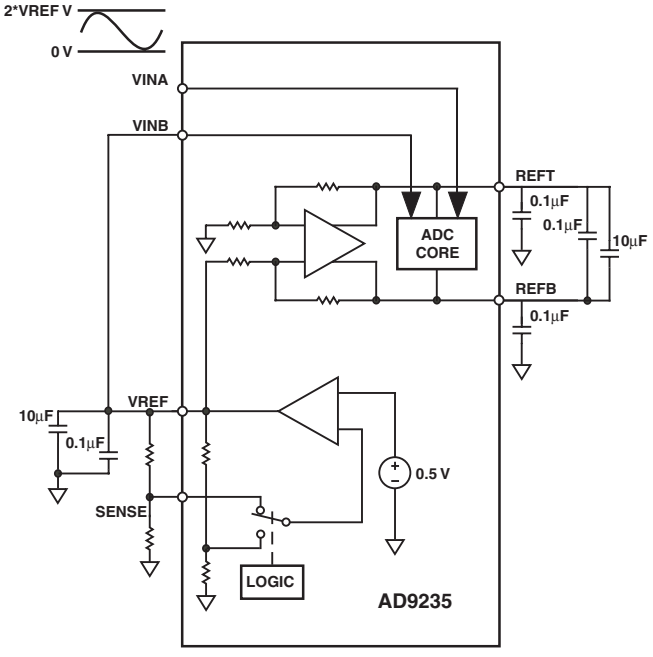


Figure 21. Internal Reference Operation, Programmable Span, Single-Ended Input

EXTERNAL REFERENCE OPERATION

The use of an external reference may be necessary for several reasons. A reference with a tighter voltage tolerance will enhance the accuracy of the ADC. A lower drift reference may be selected, which will improve gain and offset drift performance. When several ADC's track one another, a single

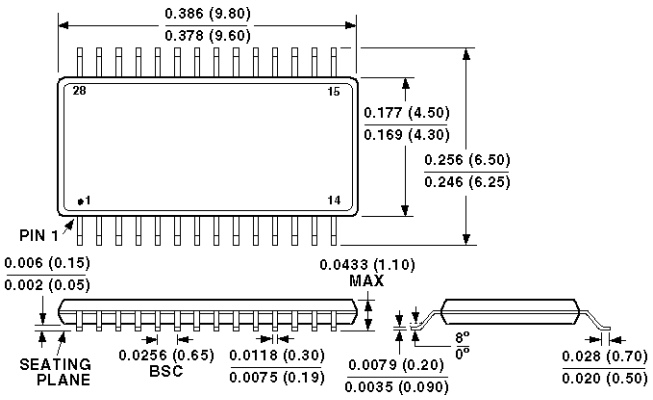
reference (internal or external) will be necessary. The AD9235 will draw less power when an external reference is used.

When the SENSE pin is tied to AVDD, the internal reference will be disabled, allowing the use of an external reference. An internal reference buffer will load the external reference with an equivalent 10 kΩ load. The internal buffer will generate positive and negative full-scale references for the ADC core. The input span will always be twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1V.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

28-Terminal Plastic Thin Shrink Small Outline Package (RU-28)



ERRATA

Date	Revision	Modification
6/15/99	R0.1	Created
2/28/00	R0.2	Created speed grade options.
3/10/00	PrA	Added pinout and pin descriptions. Updated AC specifications
7/20/00	PrB	Updated format, specifications.
9/11/00	PrC	Updated to conform to Output Bit naming convention.
1/2/01	PrD	Updated Mode Table, removed watermarks.
1/19/01	PrE	Corrected Errors, Updated format