a

14-Bit, 40/65 MSPS Monolithic A/D Converter

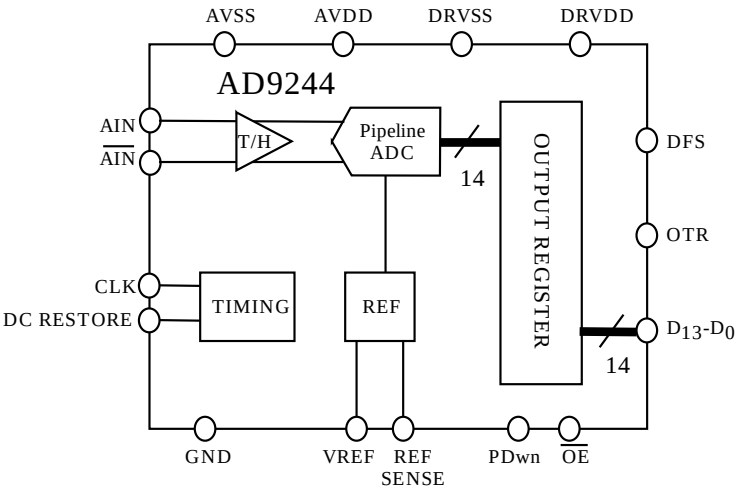
Preliminary Technical Data 2-05-01 AD9244

FEATURES
14-Bit, 65MSPS ADC
Low Power:
- 650mW at 65MSPS with Fin up to Nyquist
- 400mW at 20MSPS with Fin up to Nyquist

On-Chip Reference and Track/Hold
200MHz Analog Input Bandwidth
SNR = 75dB up to Nyquist
SFDR = 85dB up to Nyquist
Differential Non Linearity Error = ±0.5LSB
Guaranteed No Missing Codes Over Full Temp range
2V p-p Full Scale Analog Input Range
Single +5.0V Analog Supply, 3/5V Driver Supply
Out-of-Range Indicator
Straight Binary or Two's Complement Output Data
48-Lead LQFP Package

APPLICATIONS
Communications Subsystems (Microcell, Picocell)
Medical and High End Imaging Equipment
Ultrasound Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9244 is a monolithic, single 5V supply, 14-bit, 65MSPS Analog to Digital Converter with an on-chip, high performance sample and hold amplifier and voltage reference. The AD9244 uses a multi-stage differential pipelined architecture with output error correction logic to provide 14-bit accuracy at 65MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9244 has an on-board, programmable reference. An external reference can also be chosen to suit the DC accuracy and temperature drift requirements of the application.

A single ended clock input is used to control all internal conversion cycles. The digital output data can be presented in straight binary or in two's complement format. An out of range (OTR) signal indicates an overflow condition, which can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9244 is available in a 48 pin surface mount plastic package (48 LQFP) and is specified for operation over the industrial temperature range (-40°C to +85°C).

PRODUCT HIGHLIGHTS

Low Power—The AD9244 at 600 mW consumes a fraction of the power of presently available in existing, high speed monolithic solutions.

On-Board Sample-and-Hold (SHA)—The versatile SHA input can be configured for either single-ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9244's input range.

Single Supply—The AD9244 uses a single +5 V power supply simplifying system power supply design. It also features a separate digital output driver supply line to accommodate 3 V and 5 V logic families.

IF Sampling—The AD9244 delivers outstanding performance at input frequencies beyond the first Nyquist zone. Sampling at 65MSPS, with an input frequency of 100MHz, the AD9244 delivers 68dB SNR and SFDR of 82dB.

Rev Pr0 2/5/01

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD9244–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = +5 V, DRVDD = +3 V, f_{SAMPLE} = 65 MSPS, INPUT RANGE of 2V p-p, Differential inputs, EXTERNAL REFERENCE, T_{MIN} to T_{MAX} unless otherwise noted)

		Test	AD9244BST-65			AD9244BST-40			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION				14			14		bits
DCACCURACY									
Differential Nonlinearity (DNL)	+25°C	I		±0.5			±0.5		LSB
	Full	VI							LSB
Integral Nonlinearity (INL)	+25°C	I		±1.0			±1.0		LSB
	Full	VI							LSB
No Missing Codes	Full	VI		guaranteed			guaranteed		
Gain Error[1]	+25°C	I		±tbd			±tbd		%FS
	Full	VI							%FS
Gain Tempco2	Full	VI		tbd			tbd		ppm/°C
ANALOG INPUT									
Input Voltage Range (differential)	Full	V		2			2		V p-p
Common Mode Voltage	Full	V	0.5		2	0.5		2	V
Input Offset Voltage	Full	V		tbd			tbd		mV
	+25°C	I							mV
Reference Voltage	Full			1.0			1.0		V
Input Resistance	Full	VI		5			5		kΩ
	+25°C	I							kΩ
Input Capacitance	Full	VI		7			7		pf
	+25°C	I							pf
Input Bias Current	Full	VI		5			5		µa
	+25°C	I							µa
Analog Bandwidth (full power)	+25°C	V		200			200		MHz
POWER SUPPLY									
Power Dissipation[2,3]	Full	VI		650			400		mW
Power Supply Rejection Ratio (PSRR)	+25°C	I		tbd			tbd		mV/V

NOTES
[1]Gain Error and temperature Error Coefficient are based on the ADC only (with a fixed 1.0V external reference).
[2]Digital supply current based on DRVDD = 3.0V output drive with <10pf loading under dynamic test conditions.
[3]Power dissipation is measured with a sine wave analog input of 10.3MHz

AD9244–SPECIFICATIONS

DYNAMIC SPECIFICATIONS (AVDD = +5 V, DRVDD = +3 V, f_{SAMPLE} = 65 MSPS, INPUT RANGE of 2V p-p, Differential inputs, EXTERNAL REFERENCE, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Temp	Test Level	AD9244BST-65 Min	AD9244BST-65 Typ	AD9244BST-65 Max	AD9244BST-40 Min	AD9244BST-40 Typ	AD9244BST-40 Max	Units
SWITCHING PERFORMANCE									
Max Conversion rate	Full	VI	65			40			MHz
Min Conversion Rate	Full	VI			500			500	kHz
Encode Pulse Width High (t_{EH})[1]	+25°C	IV			12			14	ns
Encode Pulse Width Low (t_{EL})[1]	+25°C	IV	3		12	3		12	ns
Aperature Delay (t_A)	+25°C	IV	3			3			ns
Aperature Uncertainty (Jitter)	+25°C	V		1			1		ps rms
Output Valid Time (t_V)[2]	+25°C	V		1			1		ns
Output Propagation Delay (t_{PD})[2]	+25°C	V		1			1		ns
DYNAMIC PERFORMANCE[3]									
Transient Response	+25°C	V		tbd			tbd		ns
Overvoltage Recovery Time	+25°C	V		tbd			tbd		ns
Signal to Noise Ratio (SNR) (without harmonics)									
f_{IN} = 2.5MHz	+25°C	I		75			74		dB
f_{IN} = 10.3MHz	+25°C	I		74			74		dB
Signal to Noise Ratio (SNR) (with harmonics)									
f_{IN} = 2.5MHz	+25°C	I		74			73		dB
f_{IN} = 10.3MHz	+25°C	I		73			73		dB
Effective Number of Bits (ENOBS)									
f_{IN} = 2.5MHz	+25°C	I		12.0			11.8		bits
f_{IN} = 10.3MHz	+25°C	I		11.8			11.8		bits
Spurious Free Dynamic Range (SFDR)									
f_{IN} = 2.5MHz	+25°C	I		85			85		dB
f_{IN} = 10.3MHz	+25°C	I		80			80		dB
2nd Harmonic Distortion									
f_{IN} = 2.5MHz	+25°C	I		tbd			tbd		dBc
f_{IN} = 10.3MHz	+25°C	I		tbd			tbd		dBc
3rd Harmonic Distortion									
f_{IN} = 2.5MHz	+25°C	I		tbd			tbd		dBc
f_{IN} = 10.3MHz	+25°C	I		tbd			tbd		dBc
Two-Tone Intermod Distortion									
f_{IN} = 2.5MHz	+25°C	V		tbd			tbd		dBc
f_{IN} = 10.3MHz	+25°C	V		tbd			tbd		dBc

NOTES
[1]Duty cycle restore circuit enabled. (50-50 duty cycle)
[2]t_{VD} and t_{PD} are measured from the 1.5V level of the ENCODE input to the 10%/90% levels of the digital output swing. The digital output load during test is not to exceed an AC load of 10pf or a DC current of ±40µa.
[3]SNR/Harmonics based on an analog input voltage of -0.5dBFS referenced to a 2.0V p-p full scale input range.

AD9244–SPECIFICATIONS

DIGITAL SPECIFICATIONS (AVDD = +5 V, DRVDD = +3 V, f_{SAMPLE} = 65 MSPS, INPUT RANGE of 2V p-p, Differential inputs, EXTERNAL REFERENCE, T_{MIN} to T_{MAX} unless otherwise noted)

		Test	AD9244BST-65			AD9244BST-40			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	+1.8			+1.8			V
Logic "0" Voltage	Full	VI			+0.3			+0.3	V
Logic "1" Current	Full	VI			±10			±10	µa
Logic "0" Current	Full	VI			±10			±10	µa
Input Capacitance	+25°C	V		5			5		pf
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	2.85			2.85			V
Logic "0" Voltage	Full	VI			0.05			0.05	V

DEFINITIONS OF SPECIFICATION

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

The variation in aperture delay for successive samples which is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

NYQUIST SAMPLING

When the frequency components of the analog input are below the Nyquist frequency (Fclock/2), this is often referred to as Nyquist sampling.

IF SAMPLING

Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Higher sampled frequencies will be aliased down into the 1st Nyquist zone (DC-Fclock/2) on the output of the ADC. Care must be taken that the bandwidth of the sampled signal does not overlap Nyquist zones and alias onto itself. Nyquist sampling performance is limited by the bandwidth of the input SHA and clock jitter (jitter adds more noise at higher input frequencies).

ABSOLUTE MAXIMUM RATINGS*

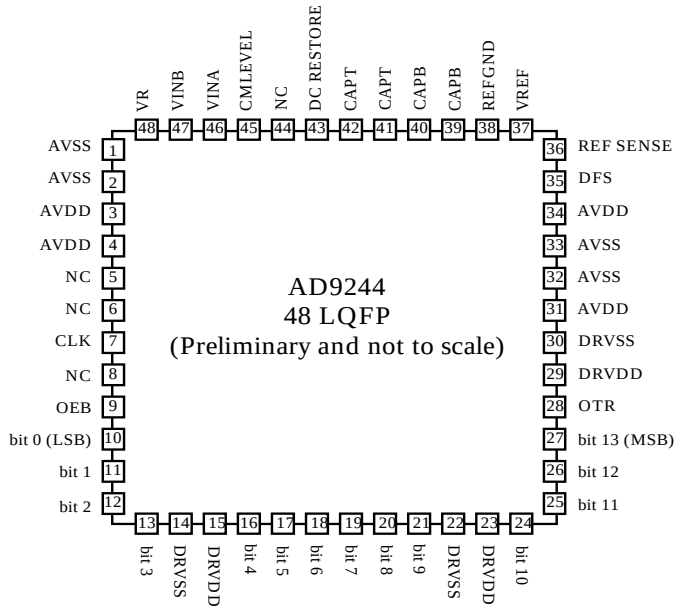
Pin Name	Min	Max	Units
AVDD	–0.3	+6.0	V
DRVDD	–0.3	+6.0	V
AVSS	–0.3	+6.0	V
AVDD	–0.3	+6.0	V
REFCOM	AVSS–0.3	AVSS + 0.3	V
CLK, MODE	AVSS–0.3	AVDD + 0.3	V
VINA, VINB	AVSS–0.3	AVSS + 0.3	V
VREF	AVSS–0.3	AVSS + 0.3	V
SENSE	AVSS–0.3	AVSS + 0.3	V
CAPB, CAPT	AVSS–0.3	AVSS + 0.3	V
Digital Output Current		20	ma
Storage Temperature	–65	+150	°C
Operating Temperature		+175	°C
Case Temperature		+175	°C
Storage Temperature	–65	+150	°C
Lead Temperature (10 sec)		+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested
II 100% production tested at 25°C and sample tested at specified temperatures
III Sample tested only
IV Parameter is guaranteed by design and characterization testing
V Parameter is a typical value only
VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.



PIN FUNCTION DESCRIPTIONS

Pin Nunber	Name	Descriptions
1,2,32,33	AVSS	Analog Ground
3,4,31,34	AVDD	Digital Supply Voltage
5,6,8,44	NC	Do not connect
7	CLK	Clock Input
9	OEB	Digital Output Enable
10	bit 0 (LSB)	Least Significant Bit, digital output
11-13,16-21		
24-26	bit 1 - bit13	digital outputs
27	bit 14 (LSB)	Most Significant Bit, digital output
14,22,30	DRVSS	Digital Ground
15,23,29	DRVDD	Digital Supply Voltage
28	OTR	Out of range indicator
35	DFS	Output Format Control, connect to; DRVDD for straight binary DRVSS for 2's complement
36	REFSENSE	Internal reference control
37	VREF	Internal Reference
38	REFGND	Reference ground
39-42	CAPT,CAPB	Internal ADC reference
43	DC RESTORE	50% Duty Cycle Restorer, (Connect to AVSS or AVDD to activate 50% restore, decouple to ground for external control of both clock edges.)
45	CMLLEVEL	Common mode reference (0.5AVSS)
46,47	VINA,VINB	Differential analog inputs
48	VR	Internal Bias Decoupling

ORDERING GUIDE

MODEL	TEMPERATURE RANGE	PACKAGE OPTION
AD9244BST-65,-40	-40°C to +85°C	ST-48
AD9244-EVAL	+25°C	Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9226 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

INTRODUCTION

The AD9244 is a high performance, single-supply 14-bit ADC. In addition to high dynamic range Nyquist sampling, it is designed for excellent IF under-sampling performance with an input analog bandwidth of 200MHz. The analog input range of the AD9244 is highly flexible, allowing for both single-ended or differential inputs of varying amplitudes that can be ac or dc coupled.

The AD9244 utilizes an eight-stage pipeline architecture with a wideband, calibrated, input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The MDAC amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The performance of the AD9244 is greatly enhanced by the use of active calibration on each die. This yields supurb dynamic performance.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes eight clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers of the AD9244 can be configured to interface with +5 V or +3.3 V logic families. The clock must be driven to 5V logic levels.

Connecting the DC RESTORE pin to either AVSS or AVDD implements the internal clock stabilization function in the Ad9244. In this mode, the AD9244 generates its own internal falling edge to create an internal 50% duty cycle clock, independent of the externally applied duty cycle. See the pin function descriptions on page 6 for details.

If the DC RESTORE pin is connected to ground through a 10kΩ resistor or left floating (and decoupled), the AD9244 will use both edges of the external clock in its internal timing circuitry (see Figure 1 and specification page for exact timing requirements).

Control of straight binary or two's complement output format is accomplished with the DFS pin. See the pin function descriptions on page 6 for details.

The ADC samples the analog input on the rising edge of the clock. While clock is low, the input SHA is in sample mode. When the clock transitions to a high logic level, the SHA goes into the hold mode. System disturbances just prior to or immediately after the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 2 is a simplified model of the AD9244 analog input. It highlights the relationship between the analog inputs, VINA, VINB, and the reference voltage, VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the A/D core. The minimum input voltage to the A/D core is automatically defined to be –VREF.

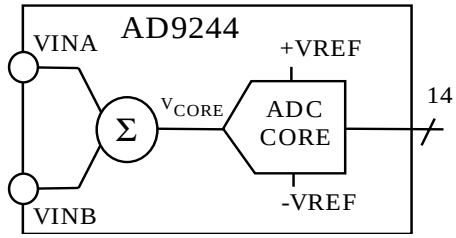


Figure 2. Equivalent Analog Input of AD9244

The addition of a differential input structure allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the A/D core is the difference of the voltages applied at the VINA and VINB input pins. Therefore, the equation

$$V_{CORE} = VINA - VINB \quad (1)$$

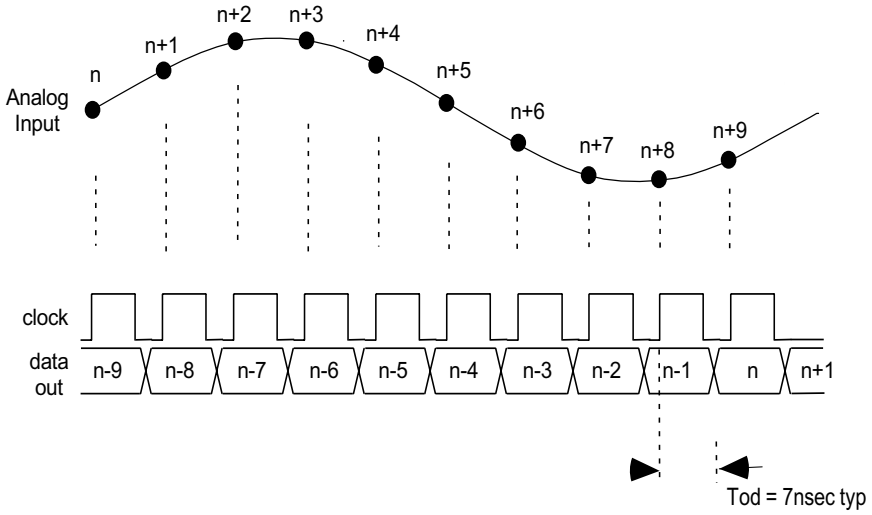


Figure 1. Input Timing for AD9244

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

$$-VREF - V_{CORE} - VREF \quad (2)$$

where *VREF* is the voltage at the *VREF* pin.

While an infinite combination of VINA and VINB inputs exist that satisfy Equation 2, an additional limitation is placed on the inputs by the power supply voltages of the AD9244. The power supplies bound the valid operating range for VINA and VINB. The condition,

$$\begin{aligned} AVSS - 0.3\,V < VINA < AVDD + 0.3\,V \\ AVSS - 0.3\,V < VINB < AVDD + 0.3\,V \end{aligned} \quad (3)$$

where *AVSS* is nominally 0 V and *AVDD* is nominally +5 V, defines this requirement. The range of valid inputs for VINA and VINB is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationship between VINA, VINB, VREF and the analog input range of the AD9244, see below in Tables I and II.

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V) VINA[1]	VINB[1]	Comments
Single-Ended	DC or AC	1.0	0.5 to 1.5	1.0	Best for stepped input response applications, requires ±5 V op amp.
		2.0	1 to 3	2.0	Optimum noise performance, excellent SNR performance, often requires low distortion op amp with VCC > +5 V due to its headroom issues.
Differential (via Transformer) or Amplifier	AC/DC	1.0	2 to 3	3 to 2	Optimum full-scale THD and SFDR performance well beyond the A/Ds Nyquist frequency. Preferred mode for undersampling applications.
		2.0	1.5 to 3.5	3.5 to 1.5	Optimum noise performance.

NOTE
[1]VINA and VINB can be interchanged if signal inversion is required.

Table II. Reference Configuration Summary

Reference Operating Mode	Input Span (VINA–VINB) (Vp-p)	Required VREF (V)	Connect	To
INTERNAL	1	1	SENSE	VREF
INTERNAL	2	2	SENSE	AVSS
INTERNAL	$1 \le SPAN \le 2$ (SPAN = VREF)	$1 \le VREF \le 2.0$ AND VREF = (1 + R1/R2)	R1 R2	VREF AND SENSE SENSE AND REFCOM
EXTERNAL (NONDYNAMIC)	$1 \le SPAN \le 2$ (Span = EXT REF)	$1 \le VREF \le 2.0$	SENSE VREF	AVDD EXT. REF.

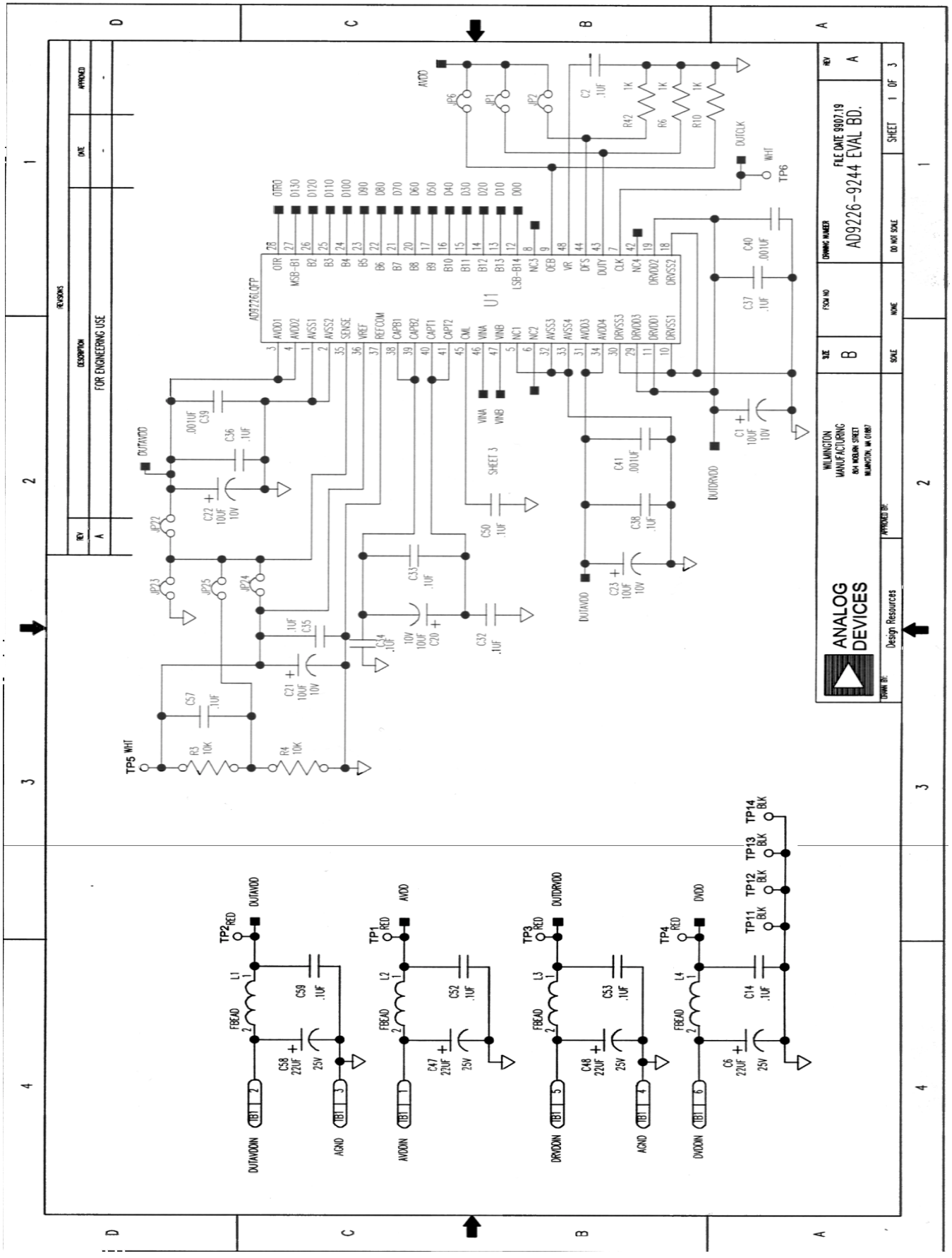


Figure 3. AD9244 Eval Board, Supply, Reference, Analog Inputs and Digital Outputs

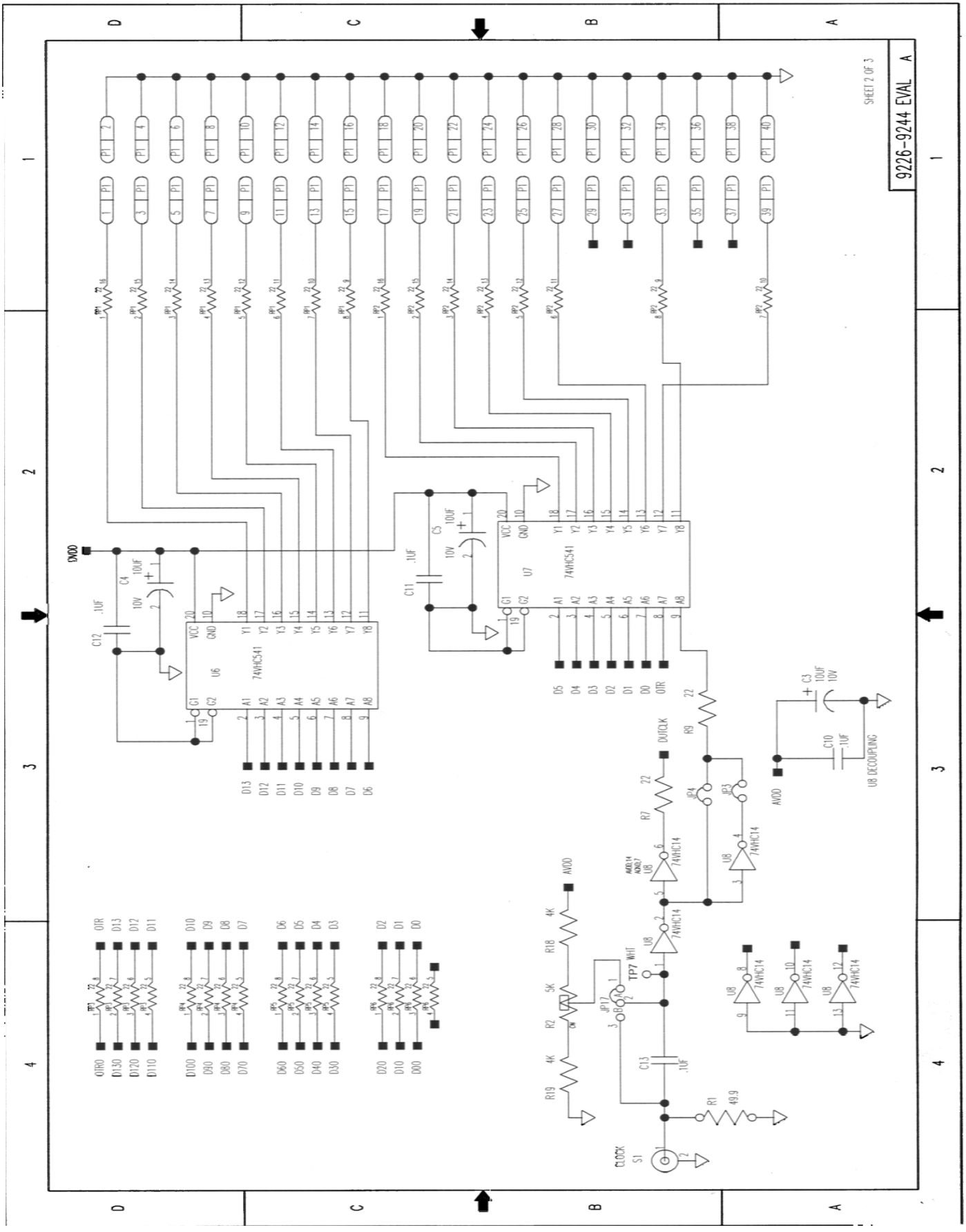


Figure 4. AD9244 Eval Board, Clock Buffer Inputs, Digital Buffer Outputs

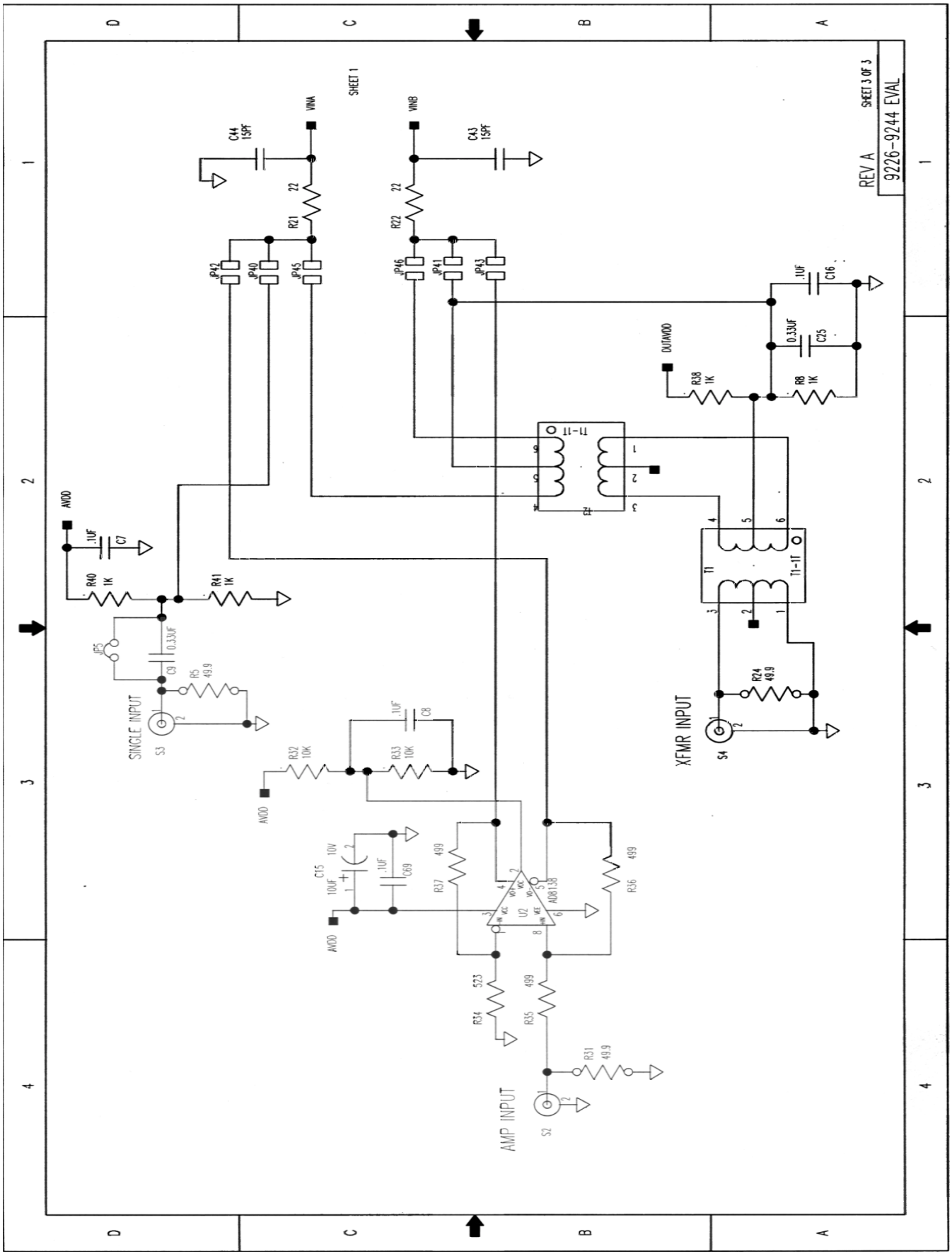


Figure 5. AD9244 Eval Board, Analog Input Circuitry

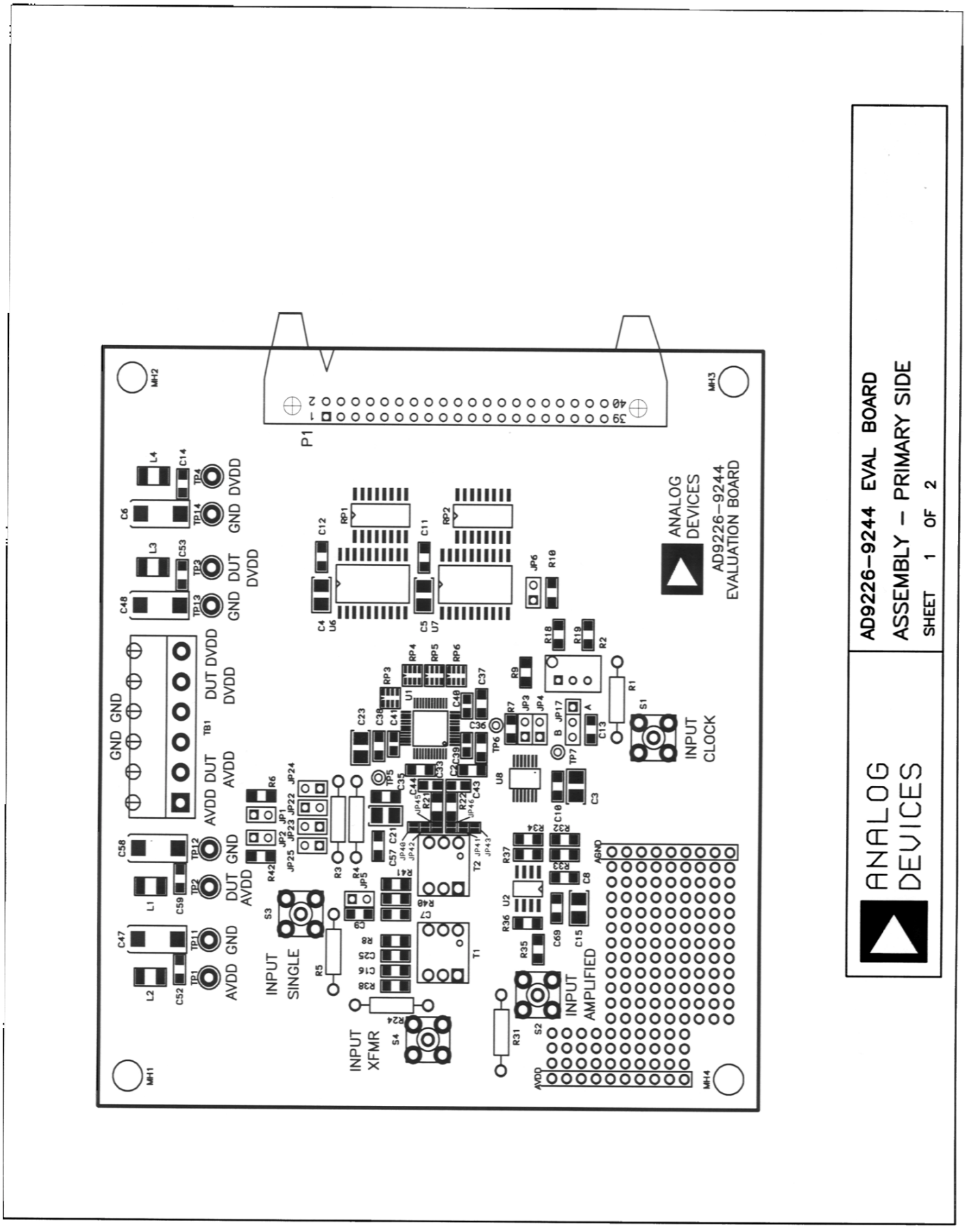


Figure 6. AD9244 Eval Board, Assembly - Primary Side

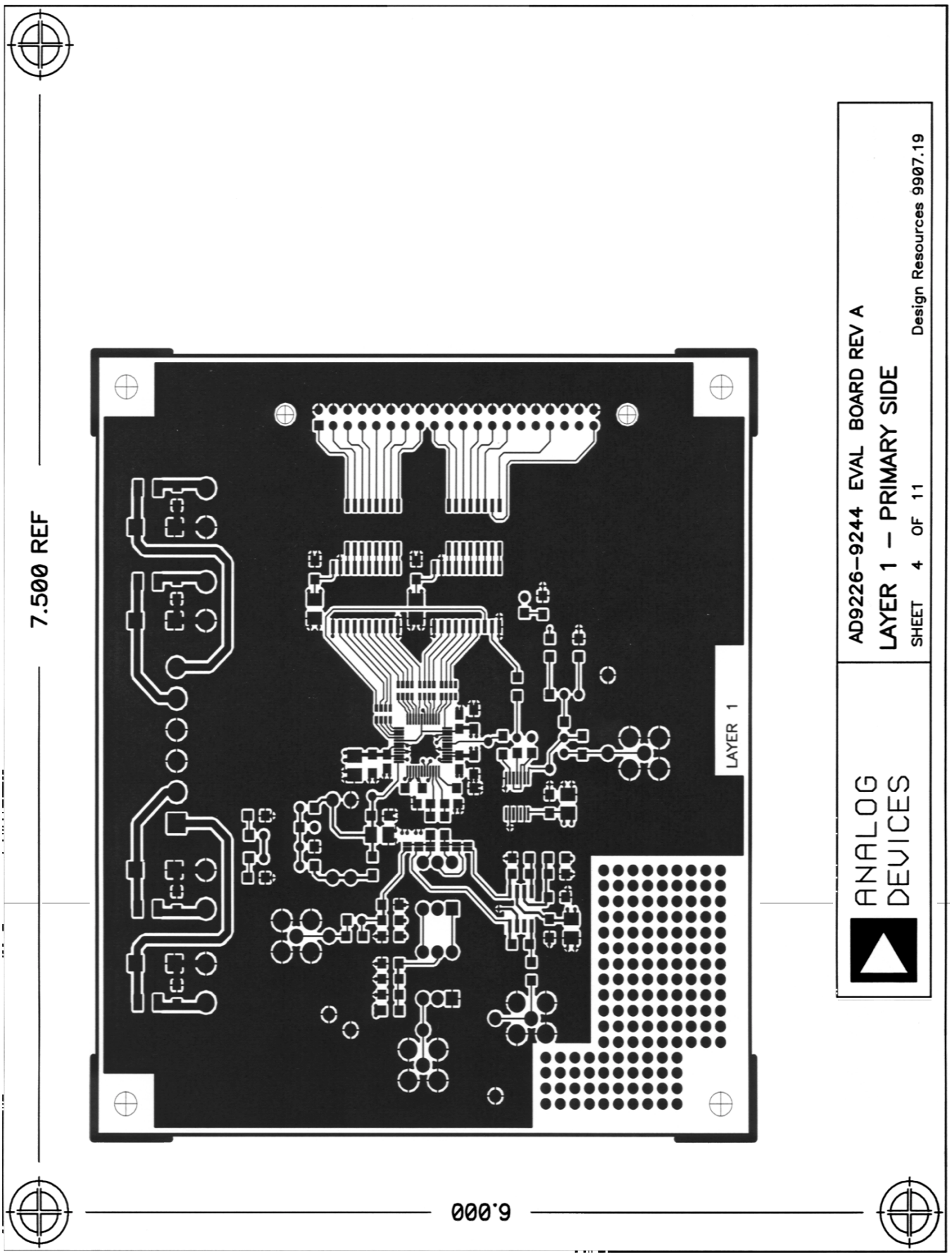


Figure 7. AD9244 Eval Board, Layer 1 - Primary Side

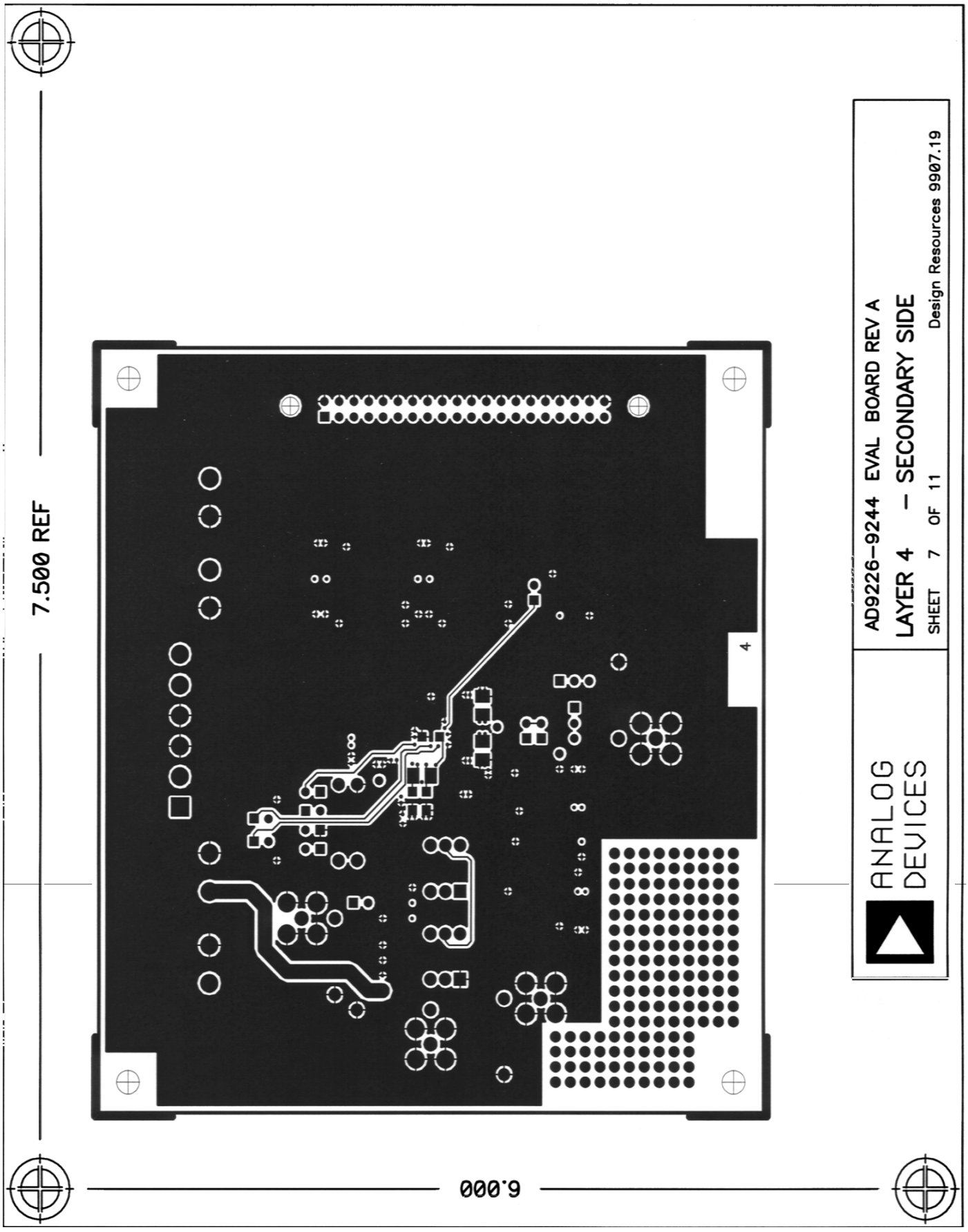


Figure 8. AD9244 Eval Board, Layer 4 - Secondary Side

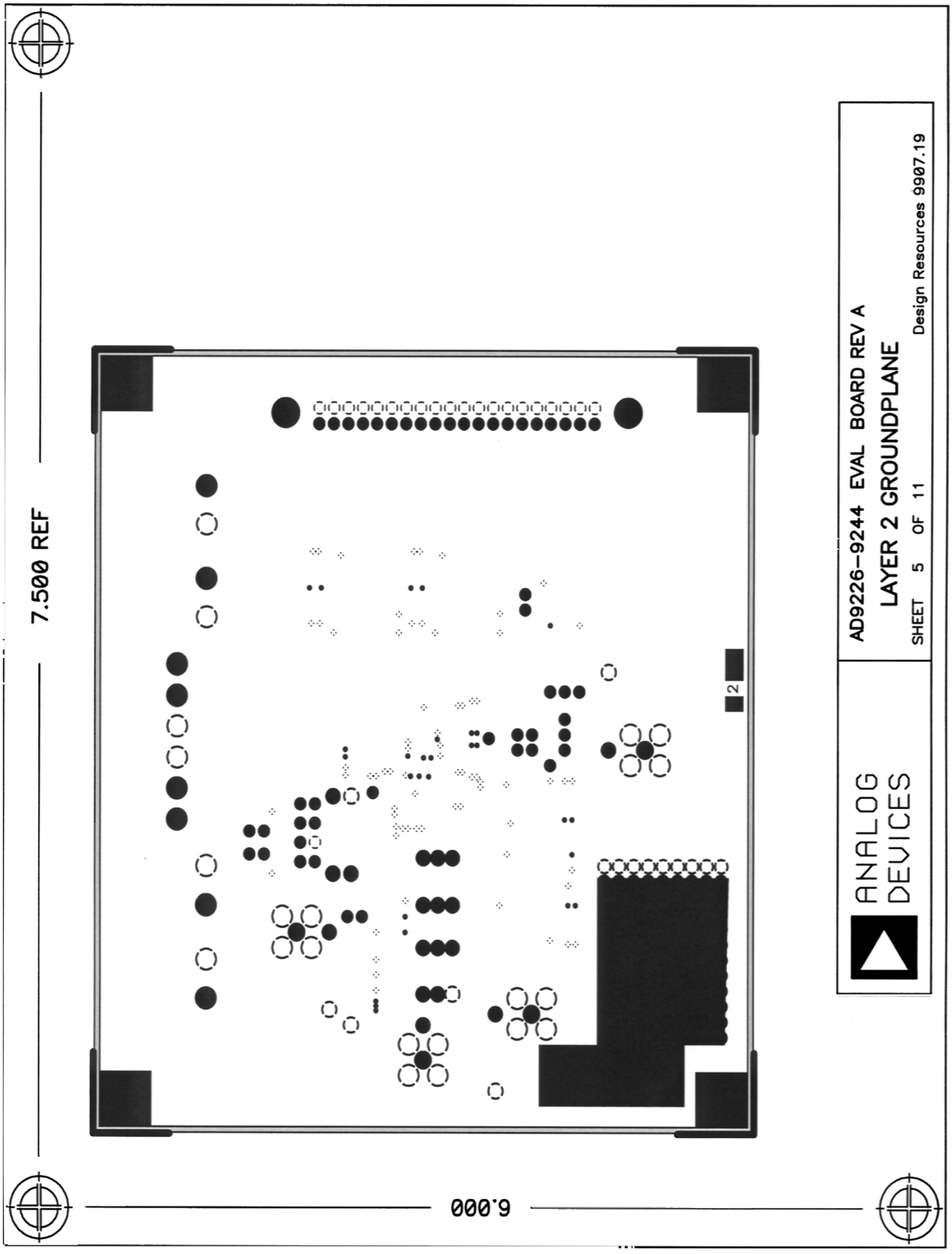


Figure 9. AD9244 Eval Board, Layer 2 - Ground Plane

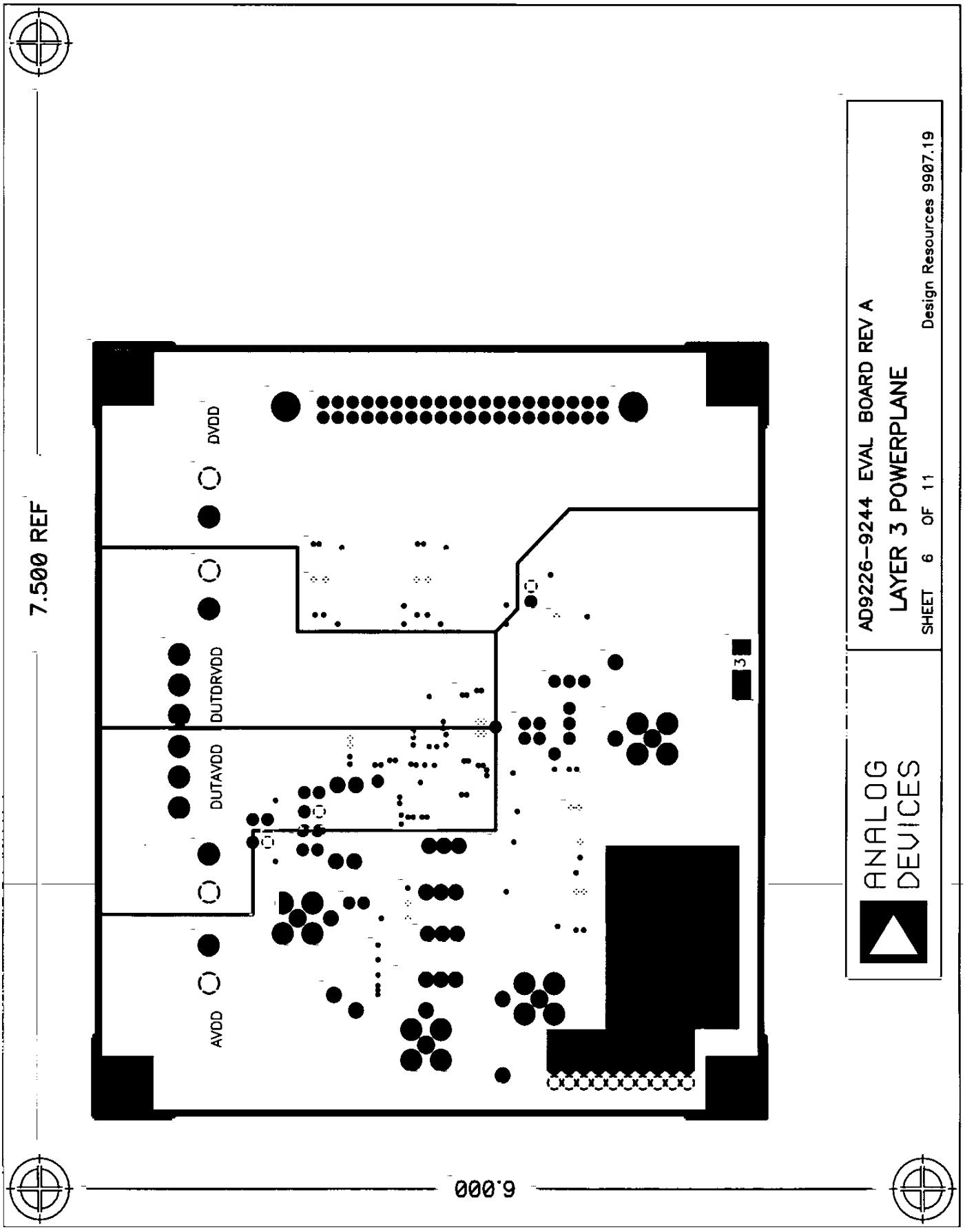


Figure 10. AD9244 Eval Board, Layer 3 - Power Plane

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48 pin LQFP package (ST-48)