10-Bit, 210 MSPS A/D Converter

AD9410

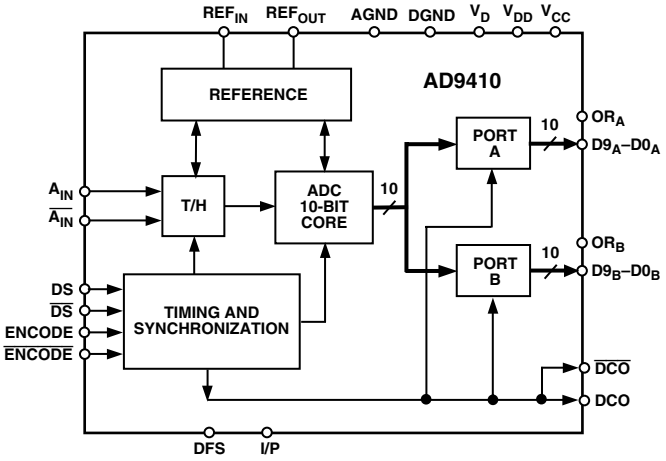
FEATURES

SNR = 54 dB with 99 MHz Analog Input
500 MHz Analog Bandwidth
On-Chip Reference and Track/Hold
1.5 V p-p Differential Analog Input Range
5.0 V and 3.3 V Supply Operation
3.3 V CMOS/TTL Outputs
Power: 2.1 W Typical at 210 MSPS
Demultiplexed Outputs Each at 105 MSPS
Output Data Format Option
Data Sync Input and Data Clock Output Provided
Interleaved or Parallel Data Output Option

APPLICATIONS

Communications and Radar
Local Multipoint Distribution Service (LMDS)
High-End Imaging Systems and Projectors
Cable Reverse Path
Point-to-Point Radio Link

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9410 is a 10-bit monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and is optimized for high-speed conversion and ease of use. The product operates at a 210 MSPS conversion rate, with outstanding dynamic performance over its full operating range.

The ADC requires a 5.0 V and 3.3 V power supply and up to a 210 MHz differential clock input for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS-compatible, and separate output power supply pins also support interfacing with 3.3 V logic.

The clock input is differential and TTL/CMOS-compatible. The 10-bit digital outputs can be operated from 3.3 V (2.5 V to 3.6 V) supplies. Two output buses support demultiplexed data up to 105 MSPS rates, and binary or two's complement output coding format is available. A data sync function is provided for timing-dependent applications. An output clock simplifies interfacing to external logic. The output data bus timing is selectable for parallel or interleaved mode, allowing for flexibility in latching output data.

Fabricated on an advanced BiCMOS process, the AD9410 is available in an 80-lead surface-mount plastic package (PowerQuad®2) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

High Resolution at High Speed—The architecture is specifically designed to support conversion up to 210 MSPS with outstanding dynamic performance.

Demultiplexed Output—Output data is decimated by two and provided on two data ports for ease of data transport.

Output Data Clock—The AD9410 provides an output data clock synchronous with the output data, simplifying the timing between data and other logic.

Data Synchronization—A DS input is provided to allow for synchronization of two or more AD9410s in a system, or to synchronize data to a specific output port in a single AD9410 system.

PowerQuad is a registered trademark of Amkor Electronics, Inc.

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AD9410–SPECIFICATIONS

DC SPECIFICATIONS (V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = –0.5 dBFS; Clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION				10		Bits
DC ACCURACY						
No Missing Codes[1]	Full	IV		Guaranteed		
Differential Nonlinearity	25°C	I	–1.0	±0.5	+1.25	LSB
	Full	VI	–1.0		+1.5	LSB
Integral Nonlinearity	25°C	I	–2.5	±1.65	+2.5	LSB
	Full	VI	–3.0		+3.0	LSB
Gain Error	25°C	I	–6.0	0	+6.0	% FS
Gain Tempco	Full	V		130		ppm/°C
ANALOG INPUT						
Input Voltage Range (With Respect to $\overline{A_{IN}}$)	Full	V		±768		mV p-p
Common-Mode Voltage	Full	V		3.0		V
Input Offset Voltage	25°C	I	–15	+3	+15	mV
	Full	VI	–20		+20	mV
Reference Voltage	Full	VI	2.4	2.5	2.6	V
Reference Tempco	Full	V		50		ppm/°C
Input Resistance	Full	VI	610	875	1250	Ω
Input Capacitance	25°C	V		3		pF
Analog Bandwidth, Full Power	25°C	V		500		MHz
POWER SUPPLY						
Power Dissipation AC[2]	25°C	V		2.1		W
Power Dissipation DC[3]	Full	VI		2.0	2.4	W
I_{VCC}[3]	Full	VI		128	145	mA
I_{VD}[3]	Full	VI		401	480	mA
Power Supply Rejection Ratio PSRR	25°C	I	–7.5	+0.5	+7.5	mV/V

NOTES
[1]Package heat slug should be attached when operating at greater than 70°C ambient temperature.
[2]Encode = 210 MSPS, A_{IN} = –0.5 dBFS 10 MHz sine wave, I_{VDD} = 31 mA typical at C_{LOAD} = 5 pF.
[3]Encode = 210 MSPS, A_{IN} = dc, outputs not switching.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = –0.5 dBFS; Clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	210			MSPS
Minimum Conversion Rate	Full	IV			100	MSPS
Encode Pulsewidth High (t_{EH})	25°C	IV	1.2	2.4		ns
Encode Pulsewidth Low (t_{EL})	25°C	IV	1.2	2.4		ns
Aperture Delay (t_A)	25°C	V		1.0		ns
Aperture Uncertainty (Jitter)	25°C	V		0.65		ps rms
Output Valid Time (t_V)	Full	VI	3.0			ns
Output Propagation Delay (t_{PD})	Full	VI			7.4	ns
Output Rise Time (t_R)	25°C	V		1.8		ns
Output Fall Time (t_F)	25°C	V		1.4		ns
CLKOUT Propagation Delay[1] (t_{CPD})	Full	VI	2.6	4.8	6.4	ns
Data to DCO Skew (t_{PD}–t_{CPD})	Full	IV	0	1	2	ns
DS Setup Time (t_{SDS})	Full	IV	0.5			ns
DS Hold Time (t_{HDS})	Full	IV	0			ns
Interleaved Mode (A, B Latency)	Full	VI		A = 6, B = 6		Cycles
Parallel Mode (A, B Latency)	Full	VI		A = 7, B = 6		Cycles

NOTES
[1]C_{LOAD} = 5 pF.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = –0.5 dBFS; Clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS						
DFS, Input Logic "1" Voltage	Full	IV	4			V
DFS, Input Logic "0" Voltage	Full	IV			1	V
DFS, Input Logic "1" Current	Full	V		50		µA
DFS, Input Logic "0" Current	Full	V		50		µA
I/P Input Logic "1" Current[1]	Full	V		400		µA
I/P Input Logic "0" Current[1]	Full	V		1		µA
ENCODE, $\overline{\text{ENCODE}}$ Differential Input Voltage	Full	IV	0.4			V
ENCODE, $\overline{\text{ENCODE}}$ Differential Input Resistance	Full	V		1.6		kΩ
ENCODE, $\overline{\text{ENCODE}}$ Common-Mode Input Voltage[2]	Full	V		1.5		V
DS, $\overline{\text{DS}}$ Differential Input Voltage	Full	IV	0.4			V
DS, $\overline{\text{DS}}$ Common-Mode Input Voltage	Full	V		1.5		V
Digital Input Pin Capacitance	25°C	V		3		pF
DIGITAL OUTPUTS						
Logic "1" Voltage (V_{DD} = 3.3 V)	Full	VI	V_{DD} – 0.05			V
Logic "0" Voltage (V_{DD} = 3.3 V)	Full	VI			0.05	V
Output Coding			Binary or Two's Complement			

NOTES
[1]I/P pin Logic "1" = 5 V, Logic "0" = GND. It is recommended to place a series 2.5 kΩ (±10%) resistor to V_{DD} when setting to Logic "1" to limit input current.
[2]See Encode Input section in Applications section.

Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = 3.3 V, V_D = 3.3 V, V_{CC} = 5.0 V; 2.5 V external reference; A_{IN} = –0.5 dBFS; Clock input = 210 MSPS; T_A = 25°C; unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Transient Response	25°C	V		2		ns
Overvoltage Recovery Time	25°C	V		2		ns
Signal-to-Noise Ratio (SNR)						
(Without Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	52.5	55		dB
f_{IN} = 82 MHz	25°C	I	52	54		dB
f_{IN} = 160 MHz	25°C	V		53		dB
Signal-to-Noise Ratio (SINAD)						
(With Harmonics)						
f_{IN} = 10.3 MHz	25°C	I	51	54		dB
f_{IN} = 82 MHz	25°C	I	50	53		dB
f_{IN} = 160 MHz	25°C	V		52		dB
Effective Number of Bits						
f_{IN} = 10.3 MHz	25°C	I	8.3	8.8		Bits
f_{IN} = 82 MHz	25°C	I	8.1	8.6		Bits
f_{IN} = 160 MHz	25°C	V		8.4		Bits
Second Harmonic Distortion						
f_{IN} = 10.3 MHz	25°C	I	–56	–65		dBc
f_{IN} = 82 MHz	25°C	I	–55	–63		dBc
f_{IN} = 160 MHz	25°C	V		–65		dBc
Third Harmonic Distortion						
f_{IN} = 10.3 MHz	25°C	I	–58	–69		dBc
f_{IN} = 82 MHz	25°C	I	–57	–67		dBc
f_{IN} = 160 MHz	25°C	V		–62		dBc
Spurious Free Dynamic Range (SFDR)						
f_{IN} = 10.3 MHz	25°C	I	56	61		dBc
f_{IN} = 82 MHz	25°C	I	54	60		dBc
f_{IN} = 160 MHz	25°C	V		58		dBc
Two-Tone Intermod Distortion IMD[1]						
f_{IN1} = 80.3 MHz, f_{IN2} = 81.3 MHz	25°C	V		58		dBFS

NOTES
[1]IN1, IN2 level = –7 dBFS.

Specifications subject to change without notice.

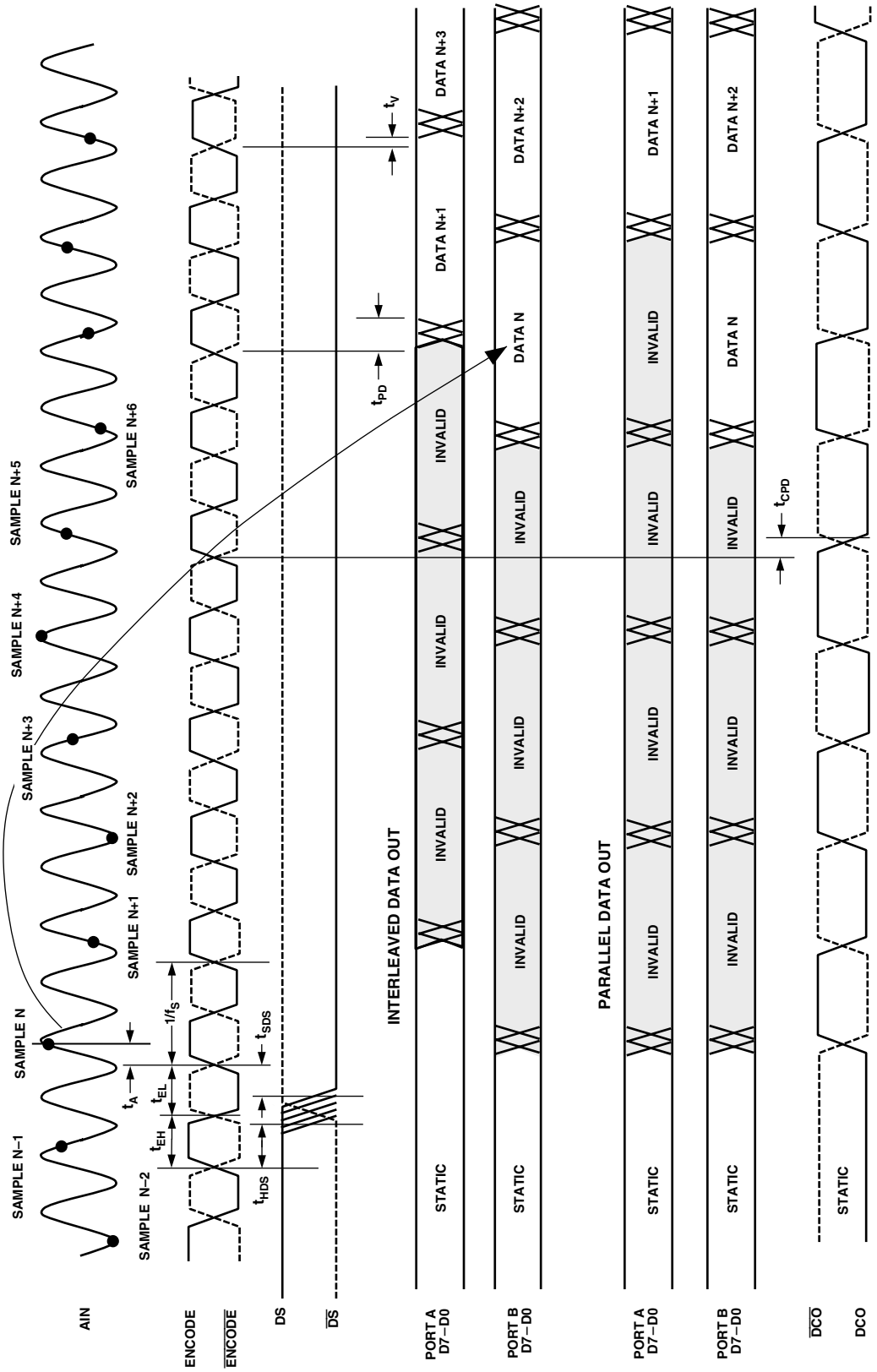


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_D, V_{CC}, V_{DD} . . . . . 6 V
Analog Inputs . . . . . 0 V to V_{CC} + 0.5 V
Digital Inputs . . . . . 0 V to V_{DD} + 0.5 V
VREF IN . . . . . 0 V to V_D + 0.5 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature[2] . . . . . 150°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied.

[2]Typical θ_{JA} = 22°C/W (heat slug not soldered), typical θ_{JA} = 16°C/W (heat slug soldered), for multilayer board in still air with solid ground plane.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9410BSQ	–40°C to +85°C	PowerQuad 2	SQ-80
AD9410/PCB	25°C	Evaluation Board	

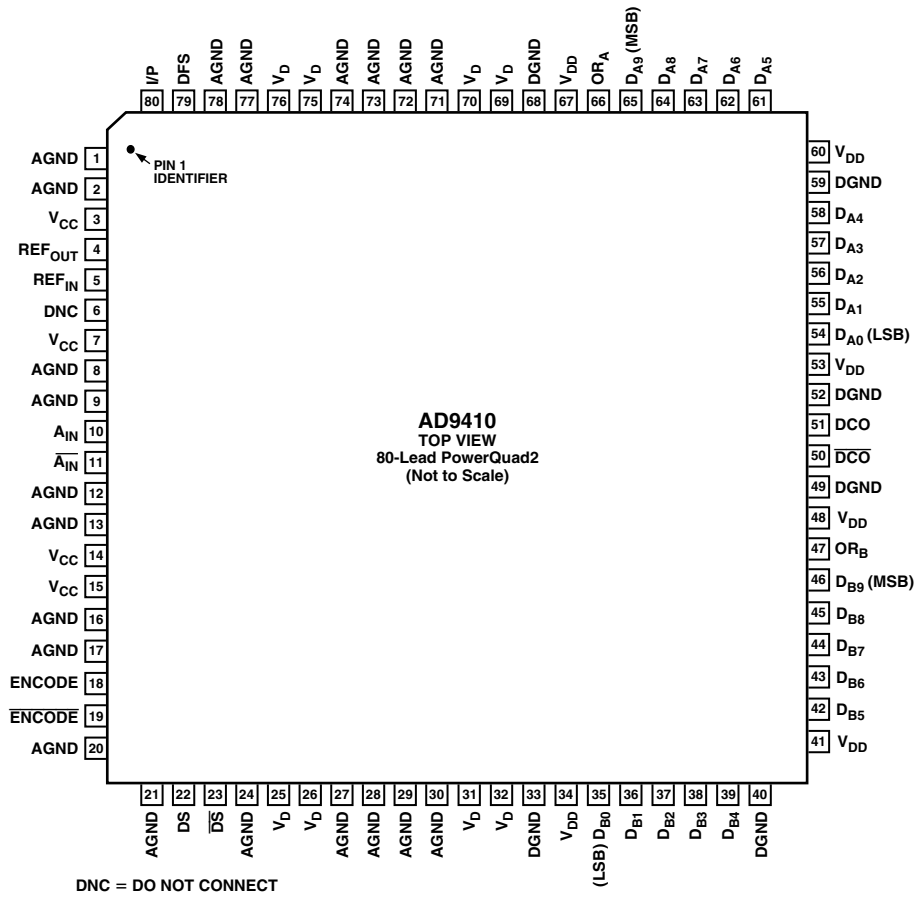
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9410 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1, 2, 8, 9, 12, 13, 16, 17, 20, 21, 24, 27, 28, 29, 30, 71, 72, 73, 74, 77, 78	AGND	Analog Ground.
3, 7, 14, 15	V_{CC}	5 V Supply. (Regulate to within ±5%.)
4	REF_{OUT}	Internal Reference Output.
5	REF_{IN}	Internal Reference Input.
6	DNC	Do Not Connect.
10	A_{IN}	Analog Input—True.
11	$\overline{A_{IN}}$	Analog Input—Complement.
18	ENCODE	Clock Input—True.
19	$\overline{\text{ENCODE}}$	Clock Input—Complement.
22	DS	Data Sync (Input)—True. Tie LOW if not used.
23	$\overline{\text{DS}}$	Data Sync (Input)—Complement. Float and decouple with 0.1 µF capacitor if not used.
25, 26, 31, 32, 69, 70, 75, 76	V_D	3.3 V Analog Supply. (Regulate to within ±5%.)
33, 40, 49, 52, 59, 68	DGND	Digital Ground.
34, 41, 48, 53, 60, 67	V_{DD}	3.3 V Digital Output Supply. (2.5 V to 3.6 V)
35–39	D_{B0}–D_{B4}	Digital Data Output for Channel B. (LSB = D_{B0}.)
42–46	D_{B5}–D_{B9}	Digital Data Output for Channel B. (MSB = D_{B9}.)
47	OR_B	Data Overrange for Channel B.
50	$\overline{\text{DCO}}$	Clock Output—Complement.
51	DCO	Clock Output—True.
54–58	D_{A0}–D_{A4}	Digital Data Output for Channel A. (LSB = D_{A0}.)
61–65	D_{A5}–D_{A9}	Digital Data Output for Channel A. (MSB = D_{A9}.)
66	OR_A	Data Overrange for Channel A.
79	DFS	Data Format Select. HIGH = Two's Complement, LOW = Binary.
80	I/P	Interleaved or Parallel Output Mode. Low = Parallel Mode, High = Interleaved Mode. If tying high, use a current limiting series resistor (2.5 kΩ) to the 5 V supply.

PIN CONFIGURATION



DNC = DO NOT CONNECT

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits
The effective number of bits (ENOB) is calculated from the measured SINAD based on the equation.

$$ENOB = \frac{SINAD_{MEASURED} - 1.76\ dB + 20\log\left(\frac{Full\ Scale\ Amplitude}{Input\ Amplitude}\right)}{6.02}$$

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specs define an acceptable ENCODE duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$POWER_{FULL\ SCALE} = 10\log\left[\frac{\frac{V^2{}_{FULL\ SCALE_{rms}}}{|Z|_{INPUT}}}{0.001}\right]$$

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least-square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Noise (For Any Range Within the ADC)

$$V_{NOISE} = \sqrt{|Z| \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SIGNAL_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value for the particular input level, and $SIGNAL$ is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set 0.5 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 0.5 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Transient Response Time
Transient response time is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Table I. Output Coding (V_{REF} = 2.5 V)

Step	A_{IN}–$\overline{A_{IN}}$	Digital Outputs Offset Binary	Digital Outputs Two's Complement	OR_A, OR_B
	> 0.768	11 1111 1111	01 1111 1111	1
1023	0.768	11 1111 1111	01 1111 1111	0
•	•	•	•	•
•	•	•	•	•
513	0.0015	10 0000 0001	00 0000 0001	0
512	0.0	10 0000 0000	00 0000 0000	0
511	–0.0015	01 1111 1111	11 1111 1111	0
•	•	•	•	•
•	•	•	•	•
0	–0.768	00 0000 0000	10 0000 0000	0
	< –0.768	00 0000 0000	10 0000 0000	1

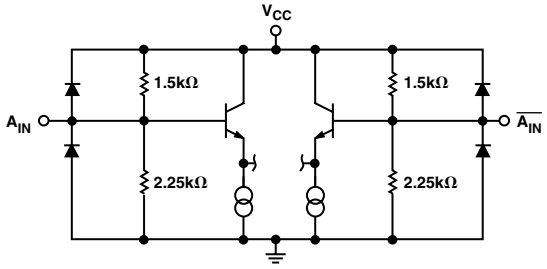


Figure 2. Equivalent Analog Input Circuit

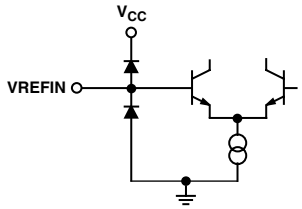


Figure 3. Equivalent Reference Input Circuit

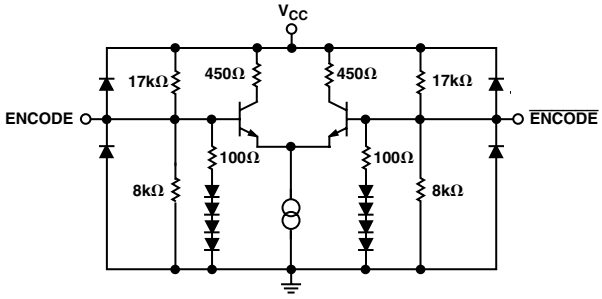


Figure 4 Equivalent Encode Input Circuit

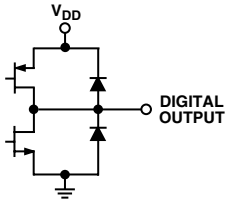


Figure 5. Equivalent Digital Output Circuit

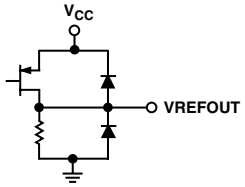


Figure 6. Equivalent Reference Output Circuit

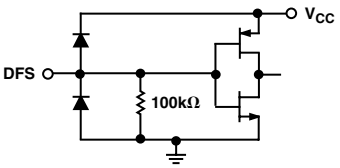


Figure 7. Equivalent DFS Input Circuit

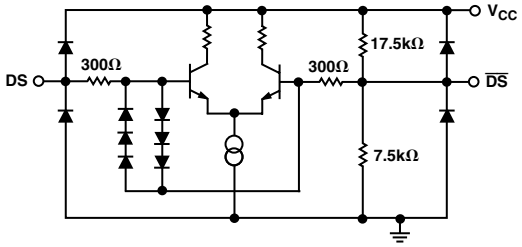


Figure 8. Equivalent DS Input Circuit

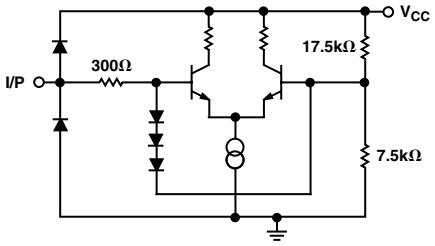
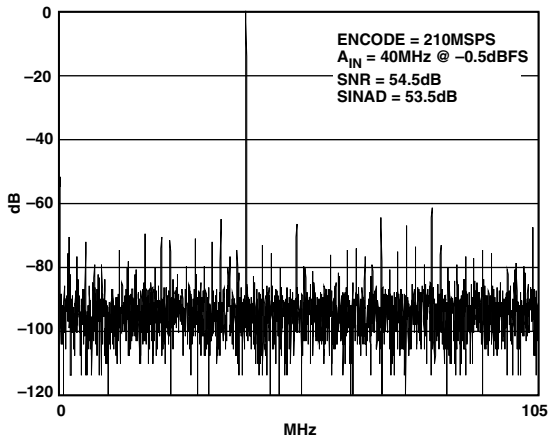
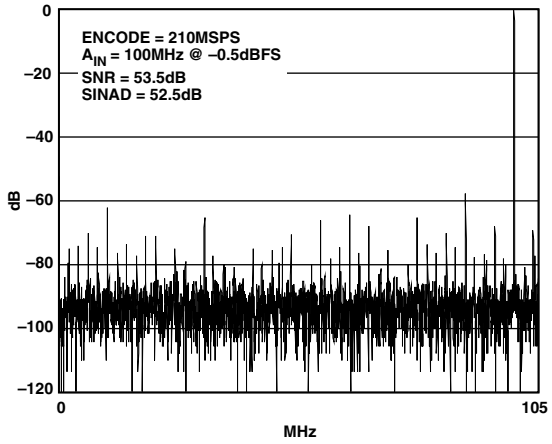


Figure 9. Equivalent I/P Input Circuit

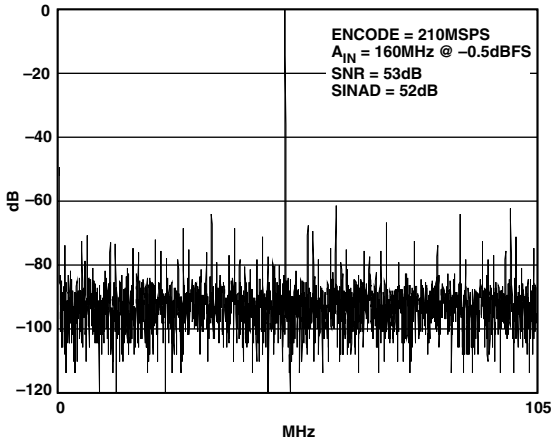
AD9410–Typical Performance Characteristics



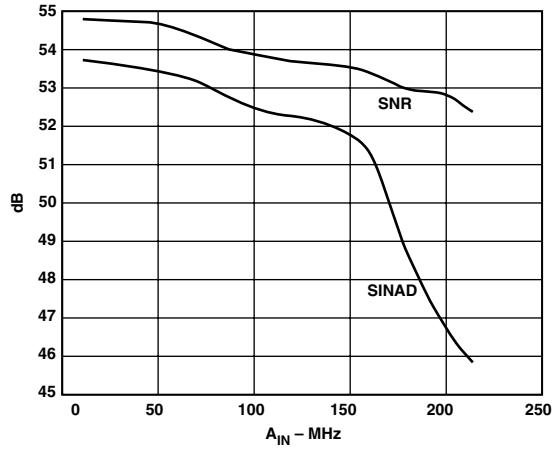
TPC 1. Single Tone at 40 MHz, Encode = 210 MSPS



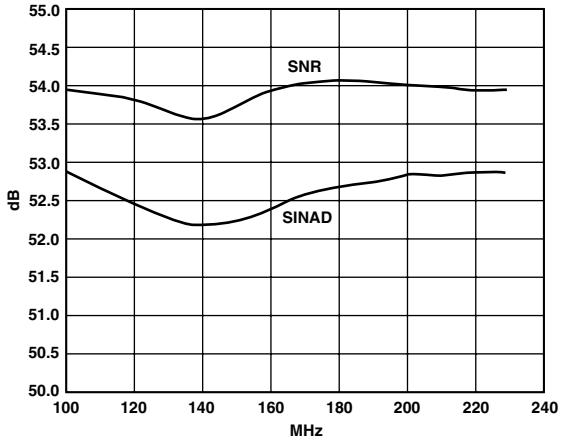
TPC 2. Single Tone at 100 MHz, Encode = 210 MSPS



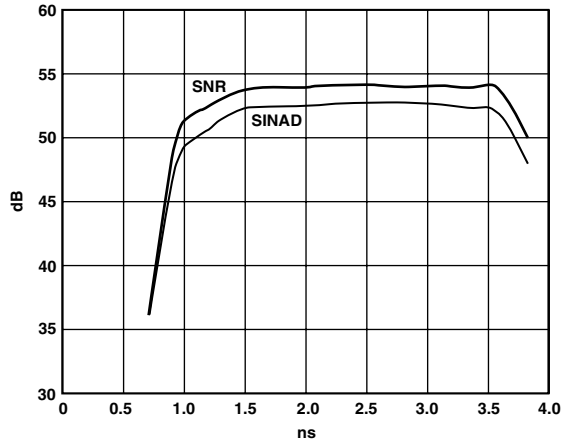
TPC 3. Single Tone at 160 MHz, Encode = 210 MSPS



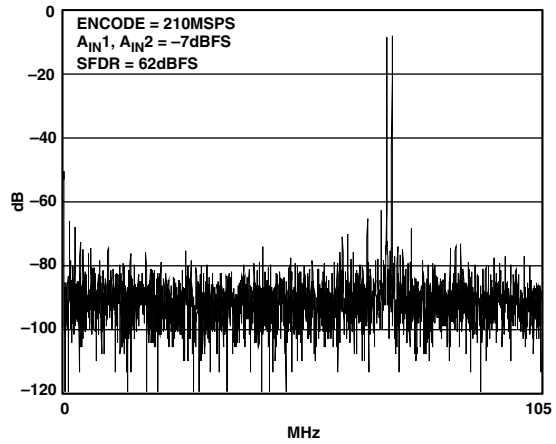
TPC 4. SNR/SINAD vs. A_{IN} Encode = 210 MSPS



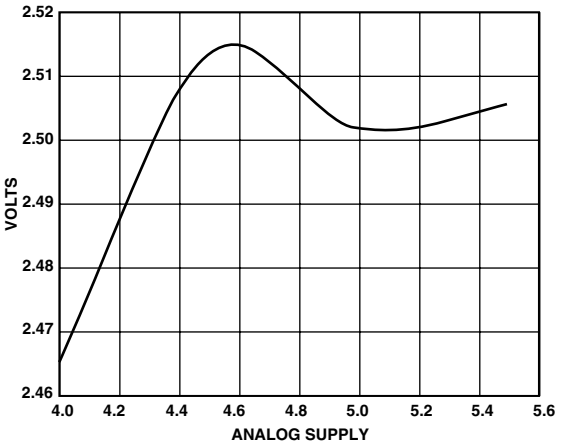
TPC 5. SNR/SINAD vs. F_S A_{IN} = 70 MHz



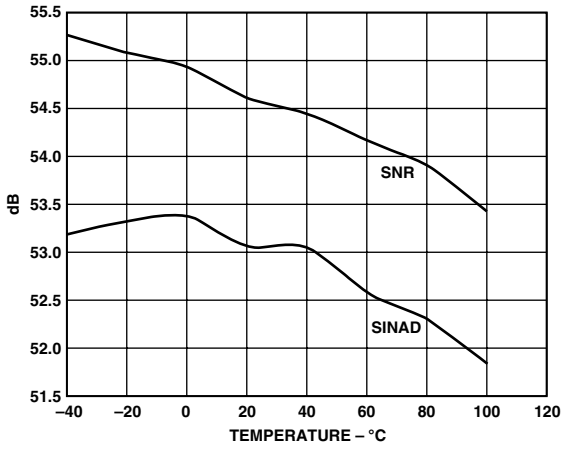
TPC 6. SNR/SINAD vs. Encode Positive Pulsewidth (F_S = 210 MSPS, A_{IN} = 70 MHz)



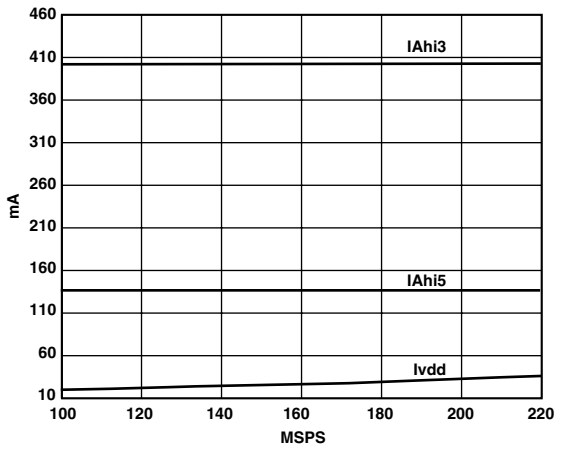
TPC 7. Two Tone Test A_{IN} 1 = 80.3 MHz, A_{IN} 2 = 81.3 MHz



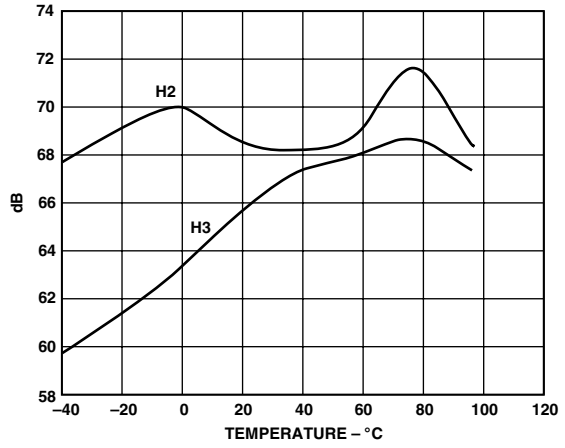
TPC 10. $VREF_{OUT}$ vs. Analog 5 V Supply



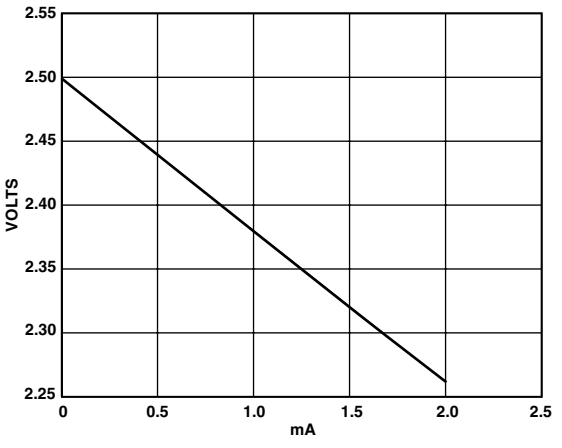
TPC 8. SNR/SINAD vs. Temperature, Encode = 210 MSPS, A_{IN} = 70 MHz



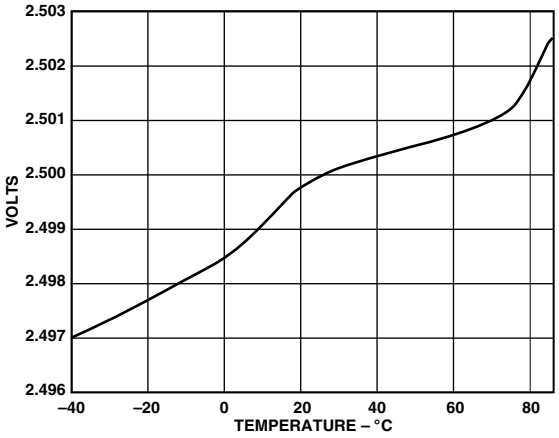
TPC 11. Power Supply Currents vs. Encode



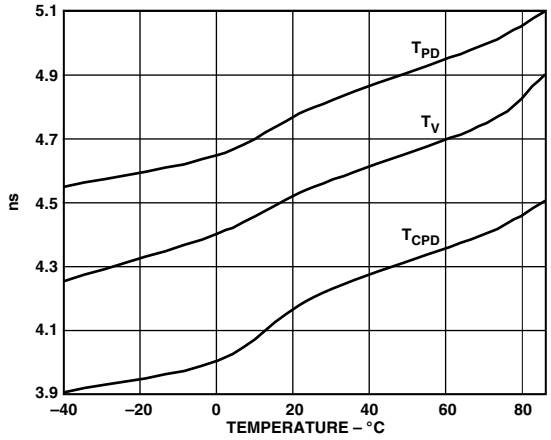
TPC 9. Second and Third Harmonics vs. Temperature; A_{IN} = 70 MHz, Encode = 210 MSPS



TPC 12. $VREF_{OUT}$ vs. I_{LOAD}



TPC 13. $VREF_{OUT}$ vs. Temperature



TPC 14. T_{PD}, T_V, T_{CPD} vs. Temperature

APPLICATION NOTES

THEORY OF OPERATION

The AD9410 architecture is optimized for high speed and ease of use. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the flash 10-bit core. For ease of use the part includes an onboard reference and input logic that accepts TTL, CMOS, or PECL levels.

USING THE AD9410

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/Hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9410, and the user is advised to give commensurate thought to the clock source. To limit SNR degradation to less than 1 dB, a clock source with less than 1.25 ps rms jitter is required for sampling at Nyquist. (Valpey Fisher VF561 is an example.) Note that required jitter accuracy is a function of input frequency and amplitude. Consult Analog Devices' application note AN-501, "Aperture Uncertainty and ADC System Performance," for more information.

The ENCODE input is fully TTL/CMOS-compatible. The clock input can be driven differentially or with a single-ended signal. Best performance will be obtained when driving the clock differentially. Both ENCODE inputs are self-biased to $1/3 \times V_{CC}$ by a high impedance resistor divider. (See Equivalent Circuits section.) Single-ended clocking, which may be appropriate for lower frequency or nondemanding applications, is accomplished by driving the ENCODE input directly and placing a 0.1 µF capacitor at $\overline{\text{ENCODE}}$.

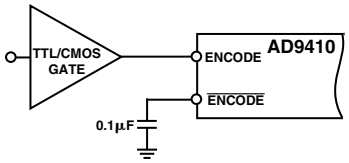


Figure 10. Driving Single-Ended Encode Input at TTL/CMOS Levels

An example where the clock is obtained from a PECL driver is shown in Figure 11. Note that the PECL driver is ac-coupled to the ENCODE inputs to minimize input current loading. The AD9410 can be dc-coupled to PECL logic levels resulting in the ENCODE input currents increasing to approximately 8 mA typically. This is due to the difference in dc bias between the ENCODE inputs and a PECL driver. (See Equivalent Circuits section.)

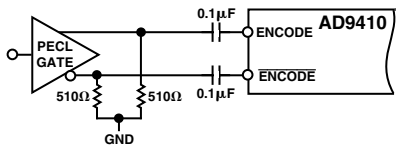


Figure 11. Driving the Encode Inputs Differentially

Analog Input

The analog input to the AD9410 is a differential buffer. For best dynamic performance, impedances at A_{IN} and $\overline{A_{IN}}$ should match. The analog input has been optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance will degrade significantly if the analog input is driven with a single-ended signal. A wideband transformer such as Minicircuits ADT1-1WT can be used to provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 3 V. (See Equivalent Circuits section.)

Special care was taken in the design of the Analog Input section of the AD9410 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.5 V diff p-p.

The nominal differential input range is 768 mV p-p × 2.

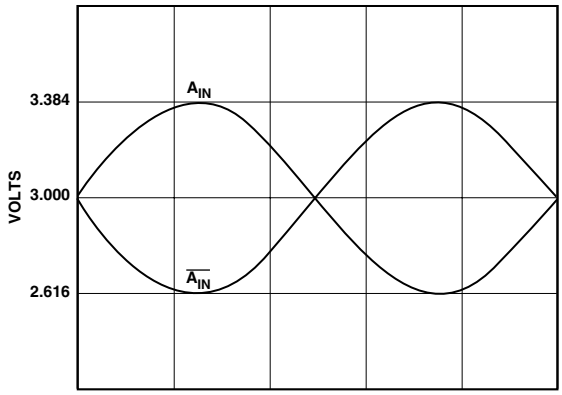


Figure 12. Typical Analog Input Levels

Digital Outputs

The digital outputs are TTL/CMOS-compatible for lower power consumption. The outputs are biased from a separate supply (V_{DD}), allowing easy interface to external logic. The outputs are CMOS devices which will swing from ground to V_{DD} (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total C_{LOAD} < 5 pF). It is also recommended to place low value (20 Ω) series damping resistors on the data lines to reduce switching transient effects on performance.

Clock Outputs (DCO, $\overline{\text{DCO}}$)

The input ENCODE is divided by two and available off-chip at DCO and $\overline{\text{DCO}}$. These clocks can facilitate latching off-chip, providing a low skew clocking solution (see timing diagram). These clocks can also be used in multiple AD9410 systems to synchronize the ADCs. Depending on application, DCO or $\overline{\text{DCO}}$ can be buffered and used to drive the DS inputs on a second AD9410, ensuring synchronization. The on-chip clock buffers should not drive more than 5 pF–7 pF of capacitance to limit switching transient effects on performance.

Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9410 (VREF OUT). The input range can be adjusted by varying the reference voltage. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly within the ±5% tolerance.

Timing
The AD9410 provides latched data outputs, with six pipeline delays in interleaved mode (see Figure 1). In parallel mode, the A Port has one additional cycle of latency added on-chip to line up transitions at the data ports—resulting in a latency of seven cycles for the A Port. The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9410; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9410 is 100 MSPS. At internal clock rates below 100 MSPS, dynamic performance may degrade. Note that lower effective sampling rates can be obtained simply by sampling just one output port—decimating the output by two. Lower sampling frequencies can also be accommodated by restricting the duty cycle of the clock such that the clock high pulsewidth is a maximum of 5 ns.

Data Sync (DS)
The Data Sync input, DS, can be used in applications requiring that a given sample will appear at a specific output Port A or B. *When DS is held high, the ADC data outputs and clock do not switch and are held static.* Synchronization is accomplished by the assertion (falling edge) of DS, within the timing constraints T_{SDS} and T_{HDS} relative to an encode rising edge. (On initial synchronization T_{HDS} is not relevant.) If DS falls within the required setup time (T_{SDS}) before a given encode rising edge N, the analog value at that point in time will be digitized and available at Port B six cycles later (interleaved mode). The very next sample, N+1, will be sampled by the next rising encode edge and available at Port A six cycles after that encode edge (interleaved mode). In dual parallel mode the A Port has a seven cycle latency, the B Port has a six cycle latency, but data is available at the same time.

EVALUATION BOARD
The AD9410 evaluation board offers an easy way to test the AD9410. The board requires an analog input, clock, and 3 V, 5 V power supplies. The digital outputs and output clocks are available at a standard 80-lead header P2, P3. The board has several different modes of operation, and is shipped in the following configuration:

- Output Timing = Parallel Mode
- Output Format = Offset Binary
- Internal Voltage Reference

Power Connector
Power is supplied to the board via detachable 4-pin power strips P1, P4, P5.

VDAC – Optional DAC Supply Input (3.3 V)
EXT REF – Optional External VREF Input (2.5 V)
V_{DD} – Logic Supply (3.3 V)
3.3 VA – Analog Supply (3.3 V)
5 V – Analog Supply (5 V)

Analog Inputs
The evaluation board accepts a 1.5 V p-p analog input signal centered at ground at SMB J8. This input is terminated to 50 Ω on the board at the transformer secondary, but can be terminated at the SMB if an alternative termination is desired. The input is ac-coupled prior to the transformer. The transformer is band limited to frequencies between approximately 1 MHz and 400 MHz.

Encode
The encode input to the board is at SMB connector J1. The input is terminated on the board with 50 Ω to ground. The (>0.5 V p-p) input is ac-coupled and drives a high-speed differential line receiver (MC10EL16). This receiver provides sub- nanosecond rise times at its outputs—a requirement for the ADC clock inputs for optimum performance. The EL16 outputs are PECL levels and are ac-coupled to meet the common-mode dc levels at the AD9410 encode inputs.

REFERENCE
The AD9410 has an on-chip reference of 2.5 V available at REF_{OUT} (Pin 4). Most applications will simply tie this output to the REF_{IN} input (Pin 5). This is accomplished by placing a jumper at E1, E6. An external reference can be used placing a jumper at E1, E3.

Output Timing
The chip has two timing modes (see timing diagram). Interleaved mode is selected by Jumper E11, E7. Parallel mode is selected by Jumper E11, E14.

Data Format Select
Data Format Select sets the output data format that the ADC outputs. Setting DFS (Pin 79) low at E12, E10 sets the output format to be offset binary; setting DFS high at E12, E16 sets the output to be two's complement.

DS Pin
The DS, $\overline{DS}$ inputs are available at SMB connectors J9X and J10X. The board is shipped with DS pulled to ground by R26. $\overline{DS}$ is floating (R25X is not placed).

DAC Outputs
Each channel is reconstructed by an on-board dual channel DAC, an AD9751 to assist in debug. The performance of the DAC has not been optimized and will not give an accurate measure of the full performance of the ADC. It is a current output DAC with on-board 50 Ω termination resistors. The outputs are available at J3 and J4.

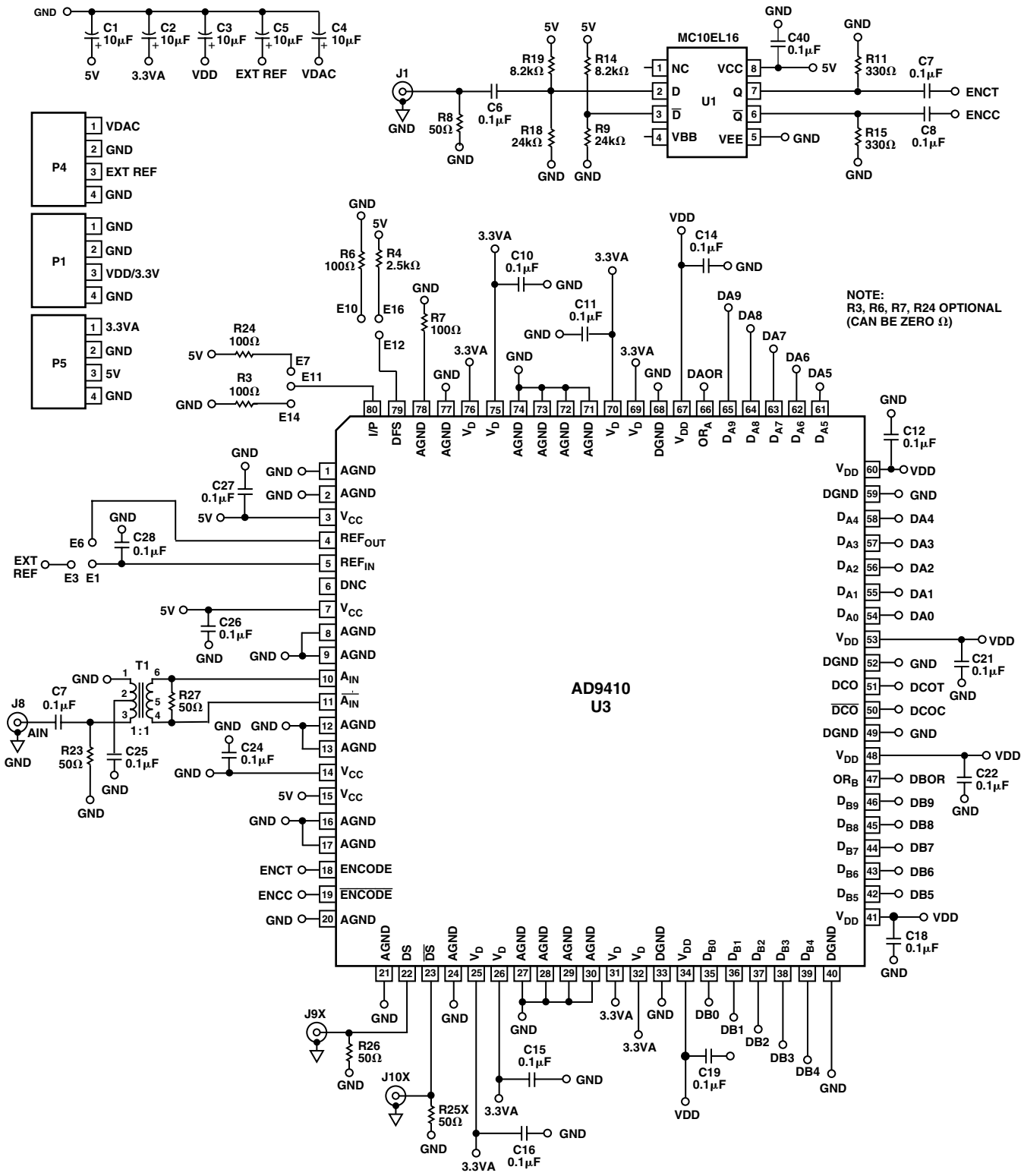


Figure 13a. PCB Schematic

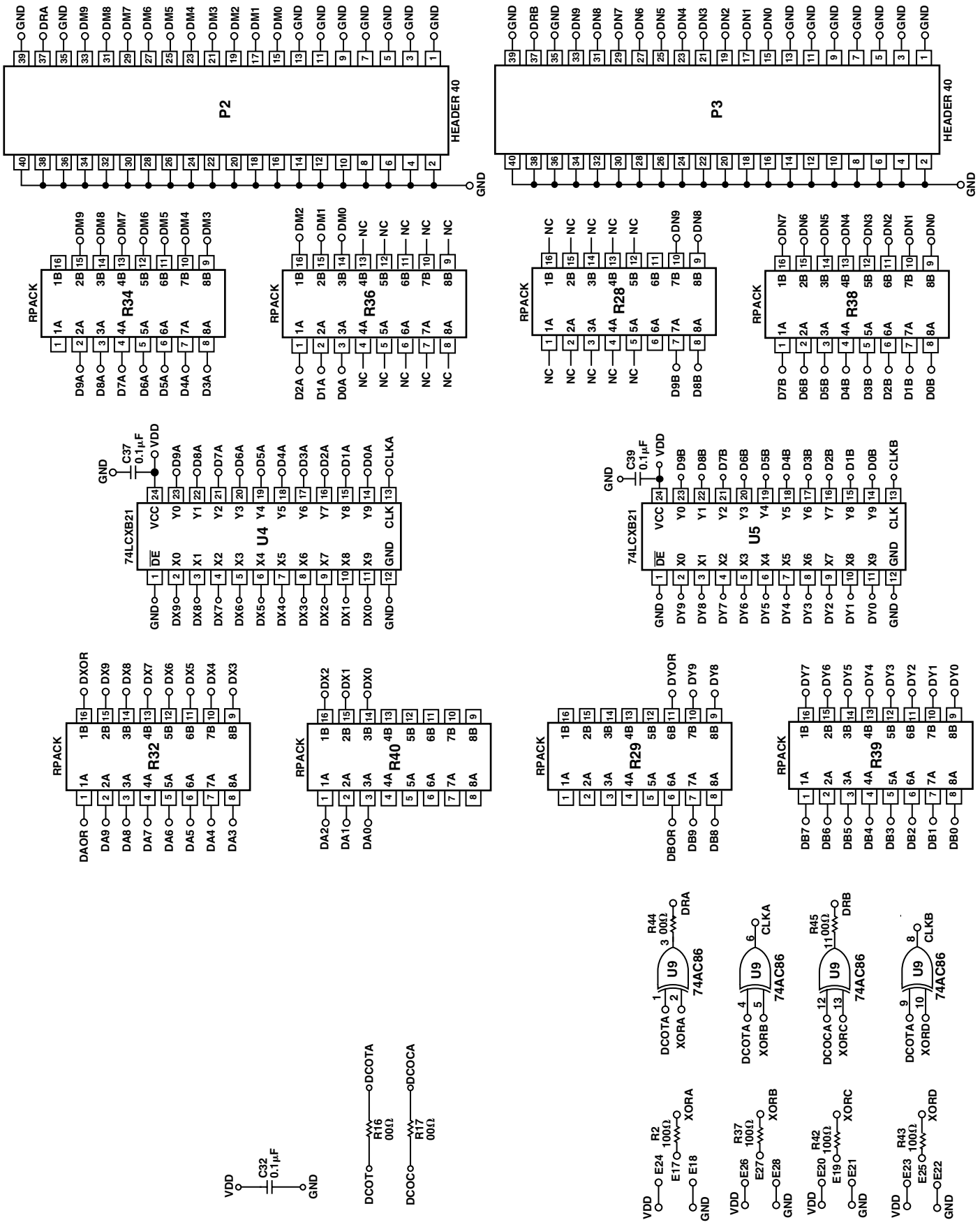


Figure 13b. PCB Schematic (Continued)

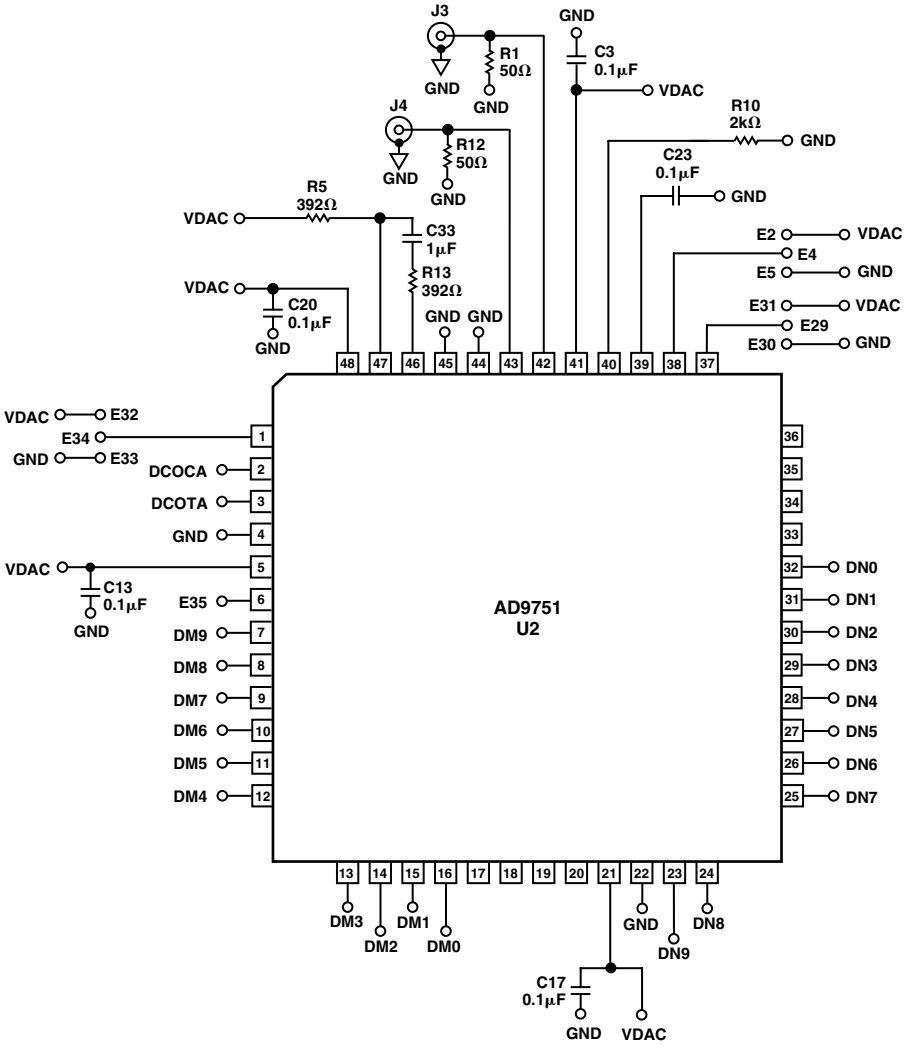


Figure 13c. PCB Schematic (Continued)

TROUBLESHOOTING

If the board does not seem to be working correctly, try the following:

- Verify power at IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify VREF is at 2.5 V.
- Try running encode clock and analog input at low speeds (*10 MSPS/1 MHz*) and monitor latch outputs, DAC outputs, and ADC outputs for toggling.

The AD9410 Evaluation Board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

EVALUATION BOARD LAYOUT

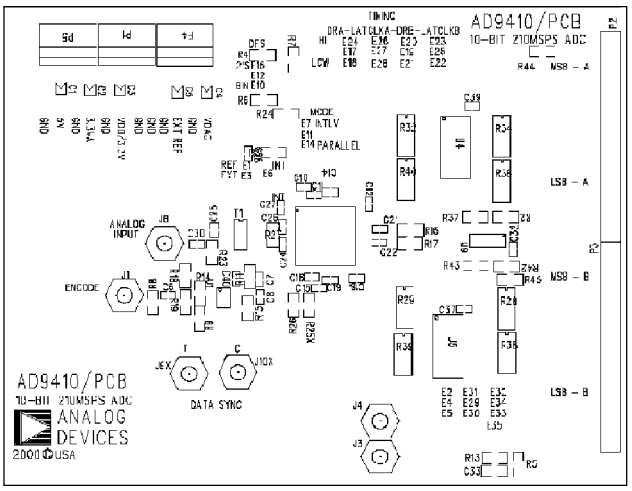


Figure 14. Top Silkscreen

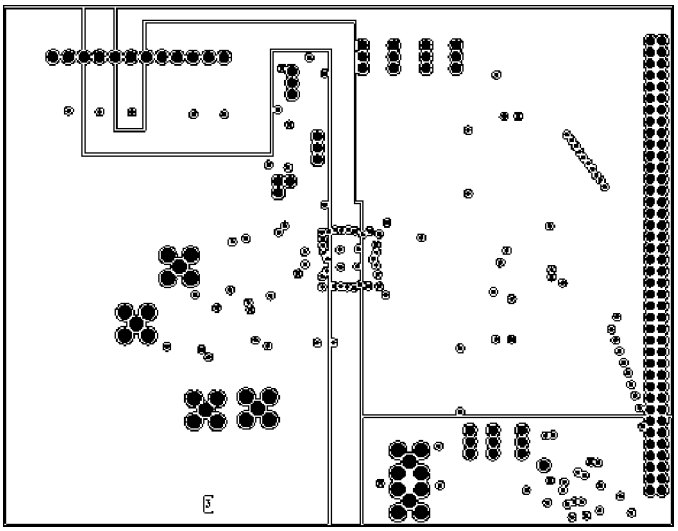


Figure 15. Split Power Plane

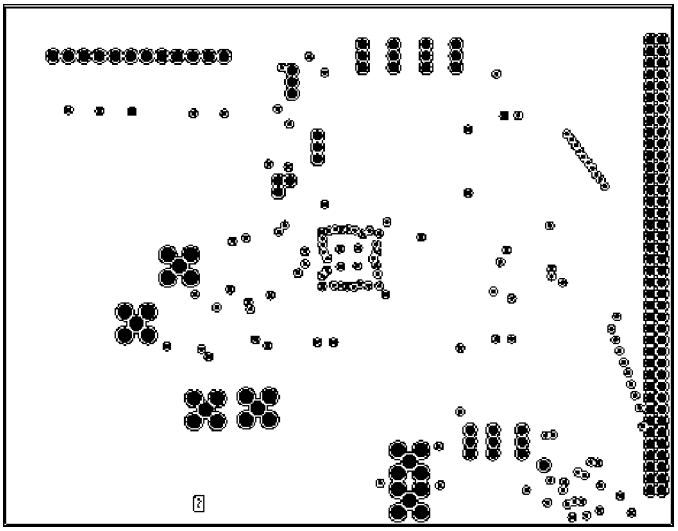


Figure 16. Ground Plane

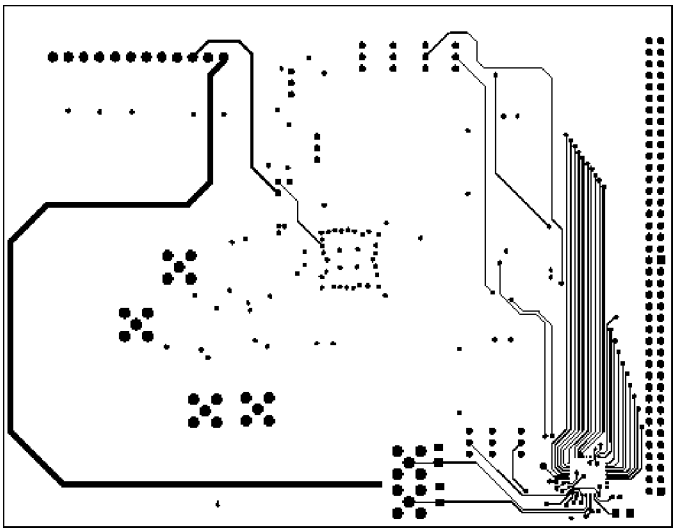


Figure 17. Bottom Components and Routing

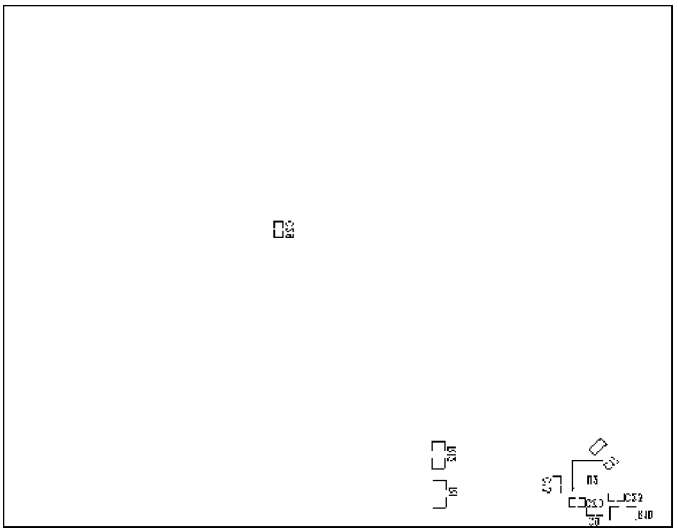


Figure 18. Bottom Silkscreen

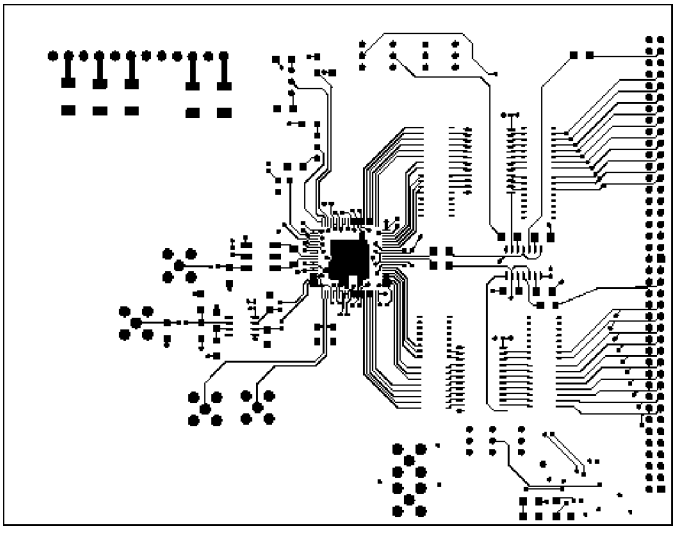


Figure 19. Top Components and Routing

AD9410 Evaluation Board Bill of Material

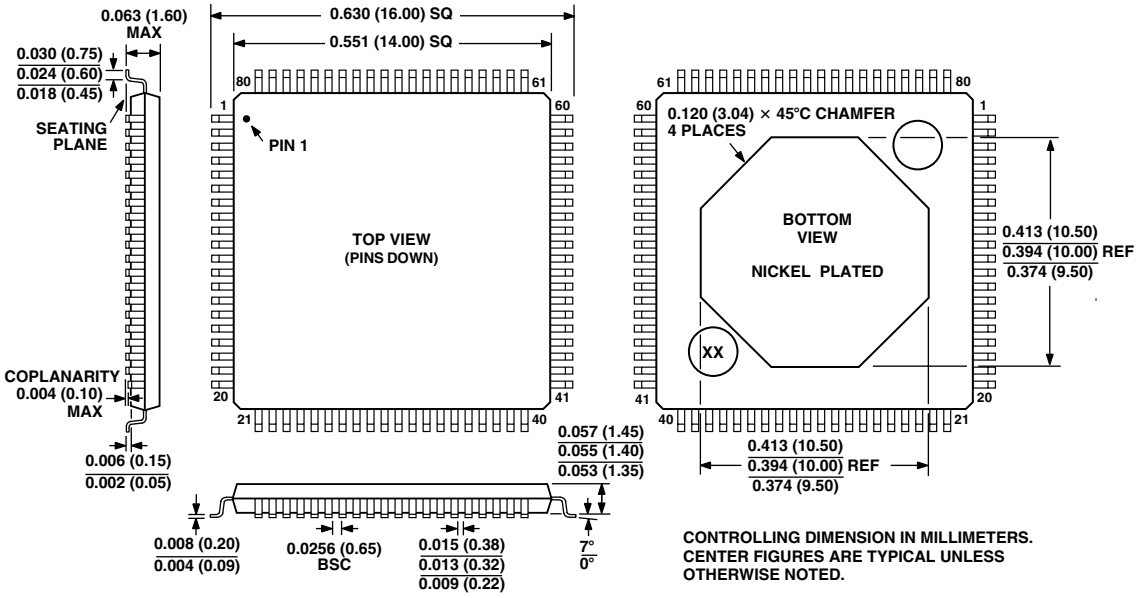
Quantity	Reference Description	Device	Package	Value
5	C1–C5	Capacitor	TAJD	10 µF
29	C6–C30, C32, C37, C39, C40	Capacitor	603	0.1 µF
1	C33	Capacitor	1206	1 µF
31	E1–E7, E10–E12, E14, E16–E35	Ehole		
6	J1, J3, J4, J8, J9X, J10X	SMB		
3	P1, P4, P5	4-Pin Power Connector	25.531.3425.0 25.602.5453.0	Wieland
2	P2, P3	40-Pin Header		
7	R1, R8, R12, R23*, R25X, R26, R27	Resistor	1206	50 Ω
8	R2, R3, R4, R6, R24, R37, R42, R43	Resistor	1206	100 Ω
1	R13	Resistor	1206	392 Ω
1	R7	Resistor	1206	100 Ω
2	R9, R18	Resistor	1206	24 kΩ
1	R10	Resistor	1206	2 kΩ
2	R11, R15	Resistor	1206	330 Ω
2	R14, R19	Resistor	1206	8.2 kΩ
5	R5, R16, R17, R44, R45	Resistor	1206	0 Ω
8	R28, R29, R32, R34, R36, R38–R40	RPACK	766163220G 22 Ω	CTS
1	T1	Transformer (1:1)	ADT1-1WT	Minicircuits
1	U1	MC10EL16	SOIC8	
1	U2	AD9751	LQFP48	
1	U3	AD9410	LQFP80	
2	U4, U5	74LCX821	SOIC24	
1	U9	74AC86	SOIC14	

*Optional R23 not placed on board (50 Ω termination resistor).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Lead PowerQuad 2 (LQFP_ED)
(SQ-80)



NOTE

The AD9410 has a conductive heat slug to help dissipate heat and ensure reliable operation of the device over the full industrial temperature range. The slug is exposed on the bottom of the package. It is recommended that no PCB traces or vias be located under the package that could come in contact with the conductive slug. Attaching the slug to a ground plane while not required in most applications will reduce the junction temperature of the device which may be beneficial in high temperature environments.

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