Mixed-Signal Front-End (MxFE™) Processor For Broadband Applications

Preliminary Technical Data **AD9861**

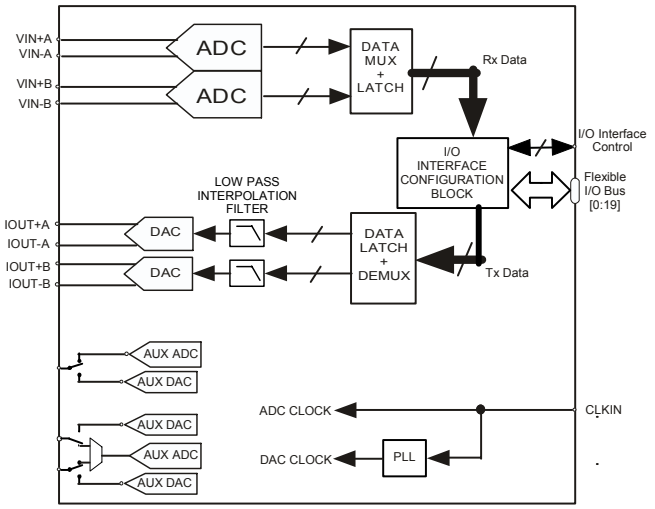
FEATURES

- Receive path includes Dual 10 Bit Analog to Digital Converters with Internal or External Reference, 50 and 80 MSPS versions
- Transmit path includes Dual 10 Bit, 200 MSPS Digital to Analog Converters with 1x, 2x, or 4x Interpolation and Programmable Gain Control
- Internal Clock Distribution Block includes a Programmable Phase-Locked-Loop and Timing Generation circuitry allowing single reference clock operation
- 20 bit flexible I/O data interface allow various interleaved or non-interleaved data transfers in half-duplex mode and interleaved data transfers in full-duplex mode
- Configurable through SPI compliant port or MODE selection pins
- Independent Rx and Tx power down control pins
- 64 Lead lfCSP package (9mmx9mm footprint)
- 3 configurable Auxiliary Converter pins

APPLICATIONS

- Broadband Access
- Broadband LAN
- Communications (modems)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9861 is a member of the MxFE™ family, a group of integrated converters for the communications market. The AD9861 includes dual 10 bit Analog to Digital Converters (ADCs) and dual 10 bit Digital to Analog Converters (TxDACs). Two speed grades are available, a -50 and -80. The -50 is optimized for ADC sampling of 50 MSPS and less, while the -80 is optimized for ADC sample rates between 50 MSPS and 80 MSPS. The dual TxDACs operate at speeds up to 200 MHz and includes a bypassable 2x or 4x interpolation filter. Three auxiliary converters are also available to provide required system level control voltages or monitor system signals. All devices are optimized for low power, small form factor and provide a cost effective solution for the broadband communication market.

The AD9861 uses a single input clock pin (CLKIN) to generate all system clocks. The ADCs and TxDACs clock are generated within a timing generation block which utilizes user programmable options such as divide circuits, PLL multiplier and switches.

A Flexible bi-directional 20 bit I/O bus is used to accommodate a variety of custom digital back ends or open market DSPs. In half duplex systems, the interface supports 20 bit parallel transfers or 10 bit interleaved transfers. In Full duplex systems, the interface supports an interleaved 10 bit ADC bus and an interleaved 10 bit Tx bus. The Flexible I/O bus reduces pin count and therefore required package size

The AD9861 can use either mode pins or a serial programmable interface (SPI) to configure the interface bus, operate the ADC in a low power mode, configure the TxDAC interpolation rate, control the ADC power down and TxDAC power down. The SPI allows for more programmable options for both the TxDAC path (for example, coarse and fine gain control, offset control for channel matching) and ADC path (for example, internal duty cycle stabilizer, 2's complement data format).

The AD9861 is packaged in a 64 pin lfCSP package (low profile, fine pitch chip scale package). The 64 pin lfCSP package footprint is only 9mm by 9mm and is less than 0.9 mm high fitting into tightly spaced applications such as PCMCIA cards.

Rev. PrA 03/6/2003

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REVISION HISTORY

Revision PrA: Initial Version

AD9861 SPECIFICATIONS

AD9861—Specifications[1] (Analog and digital supplies = 3.0V; F_{CLKIN} = 50 MHz; PLL 4x setting; Normal Timing Mode
TxDAC settings: F_{DAC} = 200 MSPS; 4x interpolation; RSET = ?? kOhms; Differential load resistance of ?? Ohms; TxPGA = 20 dB;
RxADC settings: F_{ADC} = 50 MSPS; INT ref; differential analog inputs; unless otherwise noted)

Tx Path Parameters		Temp	Test Level	Min	AD9861-50/-80 Typ	Max	Unit
Tx PATH GENERAL	Resolution	Full			10		Bits
	Maximum DAC Update Rate	Full		200			MHz
	Maximum Full Scale Output Current	Full		20			mA
	Gain Mismatch Error			-3		+3	% FS
	Offset Mismatch Error			-1		+1	% FS
	Update Timing Mismatch Error						ps
	Reference Voltage				1.23		V
	Output Capacitance				5		pF
	Phase Noise (1kHz offset, 6 MHz tone)						dBc/Hz
	Output Voltage Compliance Range			-1.0		1.0	V
Tx PATH DC ACCURACY	Integral Nonlinearity (INL)						Lsb
	Differential Nonlinearity (DNL)						Lsb
	TxPGA Gain Range				20		dB
	TxPGA Step Size				0.08		dB
Tx PATH DYNAMIC PERFORMANCE (Ioutfs = ?; Fout = ?)	SNR						dBc
	SINAD						dBc
	THD						dBc
	SFDR, Wideband (dc to Nyquist)						dBc
	SFDR, Narrowband (1 MHz Window)						dBc

Table 1

Rx Path Parameters		Temp	Test Level	Min	AD9861-50/-80 Typ	Max	Unit
Rx PATH GENERAL	Resolution	Full			10		Bits
	Maximum ADC Sample Rate	Full		50 / 80			MSPS
	Gain Mismatch Error				± 0.2		% FS
	Offset Mismatch Error				± 0.1		% FS
	Phase Mismatch Error						
	Reference Voltage				1		V
	Reference Voltage (REFT-REFB) Error				± 6		mV
	Input Resistance (differential)				2		kOhm
	Input Capacitance				5		pF
	Input Bandwidth				50		MHz
	Diiferential Analog Input Voltage Range				2		V
Rx PATH DC ACCURACY	Integral Nonlinearity (INL)				± 0.75		LSB
	Differential Nonlinearity (DNL)				± 0.75		LSB
	Aperature Delay				2.0		ns
	Aperature Uncertainty (Jitter)				1.2		ps RMS
	Input Refered Noise						
Rx PATH DYNAMIC PERFORMANCE (Vin = -0.5 dBFS; Fin = 6 MHz)	SNR				59		dBc
	SINAD				58		dBc
	THD (2^{nd} to 9^{th} harmonic)				-82		dBc
	SFDR, Wideband (dc to Nyquist)				86		dBc
	Crosstalk between ADC inputs				-80		dB

Table2

[1] Specifications subject to change without notice

AD9861—Specifications[1] (Analog and digital supplies = 3.0V; F_{CLKIN} = 50 MHz; PLL 4x setting; Normal Timing Mode
TxDAC settings: F_{DAC} = 200 MSPS; 4x interpolation; RSET = ?? kOhms; Differential load resistance of ?? Ohms; TxPGA = 20 dB
RxADC settings: F_{ADC} = 50 MSPS; INT ref; differential analog inputs; unless otherwise noted)

Power Parameters		**Temp**	**Test Level**	**Min**	**AD9861-50/-80 Typ**	**Max**	**Unit**
POWER SUPPLY RANGE	Analog Supply Voltage (AVDD)	Full	1	2.7		3.6	V
	Digital Supply Voltage (DVDD)	Full		2.7		3.6	V
	Driver Supply Voltage (DRVDD)	Full		2.7		3.6	V
ANALOG SUPPLY CURRENTS	TxPath (20 mA full scale outputs)	Full			65		mA
	TxPath (5mA full scale outputs)	Full			35		mA
	Rx Path (-80, at 80 MSPS)	Full			140		mA
	RxPath (-80, at 80 MSPS, Low Power Mode)	Full			80		mA
	Rx Path (-50, at 50 MSPS)				90		mA
	RxPath (-50, at 50 MSPS, Low Power Mode)				50		mA
	RxPath (-50, at 25 MSPS, Low Power Mode)				45		mA
	TxPath, Power Down Mode				5		mA
	RxPath, Power Down Mode				5		mA
	PLL				15		mA
DIGITAL SUPPLY CURRENTS	TxPath, 1x interpoaltion, 50 MSPS DAC update for both DACs				40		mA
	TxPath, 2x interpoaltion, 100 MSPS DAC update for both DACs				80		mA
	TxPath, 4x interpoaltion, 200 MSPS DAC update for both DACs				120		mA
	RxPath Digital				15		mA

Table 3: Specifications

Digital Parameters		**Temp**	**Test Level**	**Min**	**AD9861-50/-80 Typ**	**Max**	**Unit**
LOGIC LEVELS	Input Logic ‘1’ Voltage, Vih			DRVDD – 0.7			V
	Input Logic ‘0’ Voltage, Vil					0.4	V
	Output Logic ‘1’ Voltage, Voh (1mA load)			DRVDD – 0.6			V
	Output Logic ‘0’ Voltage, Vol (1mA load)					0.4	V
DIGITAL PIN	Input Leakage Current					12	uA
	Input Capacitance				3		pF
	Minimum RESET Low Pulsewidth			5			Input Clock Cycles
	Digital Output Rise/Fall Time			2.8		4	ns

Table 4: Specifications

[1] Specifications subject to change without notice

AD9861—Specifications[1] (Analog and digital supplies = 3.0V; F_{CLKIN} = 50 MHz; PLL 4x setting; Normal Timing Mode
TxDAC settings: F_{DAC} = 200 MSPS; 4x interpolation; RSET = ?? kOhms; Differential load resistance of ?? Ohms; TxPGA = 20 dB
RxADC settings: F_{ADC} = 50 MSPS; INT ref; differential analog inputs; unless otherwise noted)

TIMING SPECIFICATIONS

Timing Parameters		Temp	Test Level	Min	AD9861-50/-80 Typ	Max	Unit
INPUT CLOCK	CLKIN Clock Rate			1		200	MHz
	CLKIN Pulse Width High						ns
	CLKIN Pulse Width Low						ns
	PLL Input Frequnecy			16		200	MHz
	PLL Ouput Frequency			32		350	MHz
TxPATH DATA	Setup time (time required before data latching edge)				1.5		ns
	Hold time (time required after data latching edge)				2.1		ns
	Latency 1x interpolation						
	Latency 2x interpolation						
	Latency 4x interpolation						
	Wakeup Time from Power Down						
RxPATH DATA	Output Delay						
	Latency						
	Aperture Delay						
	Aperture Unceratinty						
	Wakeup Time from Power Down						

Table 5:Specifications

EXPLANATION OF TEST LEVELS

TEST LEVEL

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

[1] Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating
Electrical	AVDD Voltage	3.9 V max
	DRVDD Voltage	3.9 V max
	Analog Input Voltage	-0.3 V to AVDD + 0.3 V
	Digital Input Voltage	-0.3 V to DVDD – 0.3 V
	Digital Output Current	5 mA max
Environmental	Operating Temperature Range (Ambient)	-40°C to +85°C
	Maximum Junction Temperature	150°C
	Lead Temperature (Soldering, 10 sec)	300°C
	Storage Temperature Range (Ambient)	-65°C to +150°C

Table 6: Absolute Maximum Ratings

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Description
AD9861	-40°C to +85°C (Ambient)	64-pin lfCSP
AD9861/PCB	25°C (Ambient)	Evaluation Board

Table 7: Ordering Guide

DEFINITIONS

Input Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the CLKIN and the instant at which the analog input is actually sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Crosstalk

Coupling onto one channel being driven by a -0.5 dBFS signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range

The peak to peak differential voltage that must be applied to the converter to generate a full scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak to peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits

The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76dB}{6.02}$$

Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that a signal should be left in logic "1" state to achieve rated performance; pulse width low is the minimum time a signal should be left in a low state, logic "0".

Full Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10\log\left(\frac{\frac{V^2_{Fullscale_{rms}}}{Z_{Input}}}{.001}\right)$$

Gain Error

Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Noise (for any range within the ADC)

$$V_{noise} = \sqrt{Z * .001 * 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value for the particular input level and Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Output Propagation Delay

The delay between a differential crossing of CLK+ and CLK- and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (i.e., always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (i.e., always relates back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time

Transient response time is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time

Out of range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

DESCRIPTION

SYSTEM BLOCK DESCRIPTION

The AD9861 is targeted to cover the mixed signal front end needs of multiple wireless communication systems. It features a receive path that consists of dual 10 bit receive ADCs and a transmit path that consists of dual 10 bit transmit DACs (TxDAC™). The AD9861 integrates additional functionality typically required in most systems, such as additional auxiliary converters, Tx gain control and clock multiplication circuitry.

The AD9861 minimizes both size and power consumption to address the need of the portable market. The package is a 64 pin low profile, fine pitched chip scale package (lfCSP) that has a footprint of only 9 mm by 9mm. Power consumption is optimized to suit the particular application with power down controls, a low power ADC mode, a sub-50 MHz speed grade (AD9861-50) and half duplex mode which automatically disable the unused digital path.

The following sections discuss the four main blocks of the AD9861: Rx Block, Tx Block, Digital Block (contains Clock Generation Block) and the Auxiliary Converters.

AD9861 RX PATH BLOCK DESCRIPTION

The AD9861 Rx path consists of two 10 bit, 50 MSPS (for the AD9861-50) or 80 MSPS (for the AD9861-80) analog-to-digital converters (ADCs). The dual ADC paths share the same clocking and reference circuitry to provide optimal matching characteristics. Each of the ADC's consists of a 9 stage differential pipelined switched capacitor architecture with output error correction logic.

The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the falling edge of the input clock. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The differential input stage is dc self biased and allows differential or single-ended inputs. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers.

The latency of the Rx path is about 5 clock cycles.

Analog Input Equivalent Circuit

The Rx Path analog inputs of the AD9861 incorporate a novel structure that merges the function of the input sample-and-hold amplifiers (SHA) and the first pipeline residue amplifiers into a single, compact switched capacitor circuit. This structure achieves considerable noise and power savings over a conventional implementation that uses separate amplifiers by eliminating one amplifier in the pipeline.

The figure below illustrates the equivalent analog inputs of the AD9861 (a switched capacitor input). Bringing CLK to a logic high opens Switch S3 and closes Switches S1 and S2. The input source is connected to AIN and must charge capacitor CH during this time. Bringing CLK to a logic low opens S2, and then Switch S1 opens followed by closing S3. This puts the input in the hold mode.

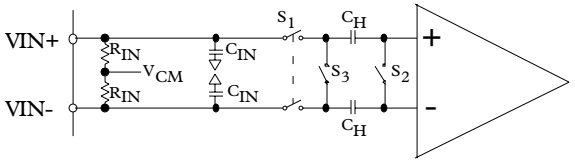


Figure #. Differential Input Architecture

The structure of the input SHA places certain requirements on the input drive source. The differential input resistors are typically 2k ohms each. The combination of the pin capacitance, C_{IN}, and the hold capacitance, C_H, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to its 10-bit accuracy in one-half of a clock cycle. When the SHA goes into track mode, the input source must charge or discharge capacitor C_H from the voltage already stored on C_H to the new voltage. In the worst case, a full-scale voltage step on the input source must provide the charging current through the R_{ON} (typically 100 ohms) of Switch S1 and quickly (within 1/2 CLK period) settle. This situation corresponds to driving a low input impedance. On the other hand, when the source voltage equals the value previously stored on CH, the hold capacitor requires no input current and the equivalent input impedance is extremely high. Adding series resistance between the output of the signal source and the VIN pins reduce the drive requirements placed on the signal source. The figure below shows this configuration.

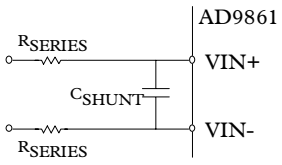


Figure #. Typical Input

The bandwidth of the particular application limits the size of this resistor. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to XX ohms or less. For applications with signal bandwidths less than 10 MHz, the user may proportionally increase the size of the series resistor.

Alternatively, adding a shunt capacitance between the AIN pins can lower the ac load impedance. The value of this capacitance will depend on the source resistance and the required signal bandwidth. In systems that must use dc-coupling, use an op amp to comply with the input requirements of the AD9861.

The ADCs in the AD9861 are designed to sample differential input signals. The differential input provides the benefit of improved noise immunity and better THD and SFDR performance for the Rx path. In systems that use single ended signals, these inputs can be digitized, but it is recommended that a single ended to differential conversion is performed. A single ended to differential conversion can be performed by using a transformer coupling circuit or using an operational amplifier such as the AD8131, which can perform the conversion.

The inputs accept a signal with a 2v pkpk differential input swing, centered about one half of the supply voltage (AVDD/2). The Rx input pins are self biased to provide this mid supply, common mode bias voltage, so it is recommended to ac couple the signal to the inputs.

ADC Voltage References

The AD9861 10 bit ADCs use internal references that are designed to provide a 2 V p-p input (differential or 1V p-p single ended) range. The internal bandgap reference generates a stable 1 V reference level and is decoupled through the Vref pin. REFT and REFB are the differential references generated based on the voltage level of Vref. Figure 2 shows the proper decoupling of the reference pins REFT and REFB when using the internal reference. An external reference may be used for systems that require high accuracy gain matching between multiple devices or improvements in temperature drift and noise characteristics. External references REFT and REFB will be centered at AVDD/2 with a differential offset voltage corresponding to half the desired input span. For example, for a 2V p-p differential input swing, the offset voltage should be:

REFT: AVDD/2 + 0.5 V,

REFB: AVDD/2 – 0.5 V

The internal Rx bandgap reference can be bypassed and an external reference used to drive the Vref voltage level. This is desirable for example to accommodate a different fullscale input swing, an extremely low temperature drift reference or to improve matching across multiple converters. To supply an external reference, the internal bandgap reference can be powered down through the SPI and the external reference can be used to drive the Vref pin. The resulting can be driven to the new voltages should be:

REFT: AVDD/2 +Vref/2 V,

REFB: AVDD/2 – Vref/2 V

If an external reference is used, it is not recommended to exceed a differential offset voltage for the reference of greater than 1V. The full scale, differential input voltage is 2x Vref voltage.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9861 contains two clock duty cycle stabilizers (DCS), one for each ADC in the Rx path that re-times the non-sampling edge, providing an internal clock with a nominal 50% duty cycle. Input clock rates of over 40 MHz can use the DCS so that a wide range of input clock duty cycles can be accommodated (conversely, DCS should not be used for Rx sampling below 40 MSPS). Maintaining a 50% duty cycle clock is particularly important in high speed applications, when proper track-and-hold times for the converter are required to maintain high performance. The DCS can be enabled by writing a high to the appropriate bits in registers 6 and 7.

The duty cycle stabilizer utilizes a delay locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency will require approximately 2 to 3 microseconds to allow the DLL to acquire and settle to the new rate. High speed, high resolution ADCs converters are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (fINPUT) due only to aperture jitter (t_A) can be calculated with the following equation:

$$\text{SNR degradation} = 20 \times \log [\tfrac{1}{2} (pi) \times F_{IN} \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum-square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter. The clock input is a digital signal that should be treated as an analog signal with logic level threshold voltages, especially in cases where aperture jitter may affect the dynamic range of the AD9861. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated of the AD9861 Rx path is proportional to its sampling rates. The Rx path portion of the digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by:

$$I_{DRVDD} = V_{DRVDD} \, x \, C_{LOAD} \, x \, f_{CLOCK} \, x \, N$$

where *N* is the number of bits changing and *CLOAD* is the average

load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases with clock frequency. The baseline power dissipation for either speed grade can be reduced by asserting the ADC_LO_PWR pin, which reduces internal ADC bias currents by half at the sake of degraded performance.

Either of the ADCs in the AD9861 Rx path can be placed in standby mode independently by writing to the appropriate SPI register bits in Registers 3, 4 and 5. The minimum standby power is achieved when both channels are placed in full power down mode using the appropriate SPI register bits in Registers 3, 4 and 5. Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time will be directly related to the recharging of the REFT and REFB decoupling capacitors and the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 uF and 10 uF decoupling capacitors on REFT and REFB.

AD9861 TX PATH BLOCK DESCRIPTION

The AD9861 Transmit (Tx) path includes dual interpolating 10- bit current output DACs that can be operated independently or coupled to form a complex spectrum in an image reject transmit architecture. Each channel includes two FIR filters, making the AD9861 capable of 1x, 2x, or 4xinterpolation. High speed input and output data rates can be achieved within the following limitations:

Interpolation Rate	20 bit Interface Mode	Input Data Rate (MSPS) per channel	DAC Sampling Rate (MSPS)
1x	FD, HD10, Clone	80	80
	HD20	160	160
2x	FD, HD10, Clone	80	160
	HD20	80	160
4x	FD, HD10, Clone	50	200
	HD20	50	200

By using the dual DAC outputs to form a complex signal, an external analog quadrature modulator, such as the Analog Devices AD8349, can enable an image rejection architecture. To optimize the image rejection capability, as well as LO feed-through suppression in this architecture, the AD9861 offers programmable (via the SPI port) fine (trim) gain and offset adjust for each DAC.

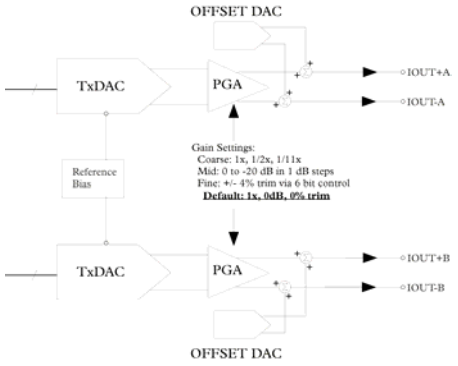
Also included in the AD9861 are a phase-locked loop (PLL) clock multiplier and a 1.2 V band gap voltage reference. With the PLL enabled, a clock applied to the CLKIN input is multiplied internally and generates all necessary internal synchronization clocks. Each 10-bit DAC provides two complementary current outputs whose full-scale currents can be determined from a single external resistor.

An external pin, TxPwrDwn, can be used to power down the Tx path when not used to optimize system power consumption. Using the TxPwrDwn pin disables clocks and some analog circuitry saving both digital and analog power. The power down mode leaves the biases enabled to facilitate a quick recovery time (typically < 10 us). Additional a SLEEP mode is available that turns off the DAC output current, but leaves all other circuits active, for a modest power savings. A SPI-compliant serial port is used to program the many features of the AD9861. Note that in power-down mode, the SPI port is still active.

DAC Equivalent Circuits

The AD9861 Tx Path consisting of dual 10-bit DACs is shown below. The DACs integrates a high performance TxDAC core, a programmable gain control through a Programmable Gain Amplifier (TxPGA), coarse gain control, and offset adjustment and fine gain control to compensate for system mismatches. Coarse gain applies a gross scaling to either DAC by 1x, 1/2 x or 1/11x. The TxPGA provides gain control from 0 dB to -20 dB in steps of 0.1 dB and is control via the 8 bit TxPGA setting. And a fine gain adjustment of +/- 4% for each channel is controlled through a 6 bit Fine Gain register. By default, coarse gain is 1x, the TxPGA is set to 0 dB and the fine gain is set to 0%.

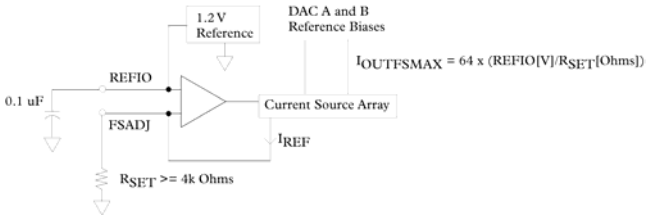
The TxDAC core of the AD9861 provides dual, differential, complementary current outputs generated from the 10-bit data. The 10-bit Dual DACs support update rates up to 200 MSPS. The differential outputs (i.e., IOUT+ and IOUT–) of each dual DAC are complementary, meaning they always sum to the full-scale current output of the DAC, IOUTFS. Optimum ac performance is achieved with the differential current interface drives balanced loads or a transformer.



The fine gain control allows for improved balance of QAM modulated signals, resulting in improved modulation accuracy and image rejection.

The independent DAC A and DAC B offset control adds a small dc current to either IOUT+ or IOUT- (not both). The selection of which IOUT this offset current is directed toward is programmable via Register setting. Offset control can be used for suppression of an LO leakage signal that typically results at the output of the modulator. If the AD9861 is dc-coupled to an external modulator, this feature can be used to cancel the output offset on the AD9861 as well as the input offset on the modulator.

The reference circuitry is shown in the Figure below.



Referring to the transfer functions in the Equation below, $I_{OUTFSMAX}$ is the maximum current output of the DAC with the default gain setting (0 dB) and is based on a reference current, I_{REF}. IREF is set by the internal 1.2 V reference and the external R_{SET} resistor.

$$I_{OUTFSMAX} = 64 \times (REFIO[V] / R_{SET}[Ohms])$$

Typically, R_{SET} is 4 kohms, which sets $I_{OUTFSMAX}$ to 20 mA, the optimal dynamic setting for the TxDACs. Increasing RSET by a factor of 2 will proportionally decrease $I_{OUTFSMAX}$ by a factor of 2. $I_{OUTFSMAX}$ of each DAC can be re-scaled either simultaneously with the TxPGA Gain register or independently with DAC A/B Coarse Gain registers.

The TxPGA function provides 20 dB of simultaneous gain range for both DACs and is controlled by writing to SPI register TxPGA Gain for a programmable full-scale output of 10% to 100% $I_{OUTFSMAX}$. The gain curve is linear in dB, with steps of about 0.1 dB. Internally, the gain is controlled by changing the main DAC bias currents with an internal TxPGA DAC whose output is heavily filtered via an on-chip R-C filter to provide continuous gain transitions. Note, the settling time and bandwidth of the TxPGA DAC can be improved by a factor of 2 by writing to the TxPGA Fast register.

Each DAC has independent coarse gain control. Coarse gain control can be used to accommodate different IOUTFS from the dual DACs. The coarse full-scale output control can be adjusted using the DAC A/B Coarse Gain registers to 1/2 or 1/11th of the nominal full scale current.

Fine Gain controls and dc offset controls can be used to compensate for mismatches (for system level calibration), allowing improved matching characteristics of the two Tx channels and aiding in suppressing LO feedthrough. This is especially useful in image rejection architectures. The 10-bit dc offset control of each DAC can be used independently to provide a +/-12% $I_{OUTFSMAX}$ of offset to either differential pin, thus allowing calibration of any system offsets. The fine gain control with 5-bit resolution allows the $I_{OUTFSMAX}$ of each DAC to be varied over a +/-4% range, thus allowing compensation of any DAC or system gain mismatches. Fine gain control is set through the DAC A/B Fine Gain registers and the offset control of each DAC is accomplished using DAC A/B Offset registers.

CLOCK INPUT CONFIGURATION

The quality of the clock and data input signals is important in achieving optimum performance. The external clock driver circuitry should provide the AD9861 with a low jitter clock input that meets the min/max logic levels while providing fast edges.. When a driver is used to buffer the clock input, it should be placed very close to the AD9861 clock input, thereby negating any transmission line effects such as reflections due to mismatch.

PROGRAMMABLE PLL

CLKIN can function either as an input data rate clock (PLL enabled) or as a DAC data rate clock (PLL disabled).

The PLL clock multiplier and distribution circuitry produce the necessary internal timing to synchronize the rising edge triggered latches for the enabled interpolation filters and DACs. This circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO) and clock distribution block, all under SPI port control. The charge pump, phase detector and VCO are powered from PLLVDD while the clock distribution circuits are powered from the DVDD supply.

To ensure optimum phase noise performance from the PLL clock multiplier circuits PLLVDD should

originate from a clean analog supply. The speed of the VCO within the PLL also has an effect on phase noise.

The PLL will lock with a VCO speeds as low as 32 MHz up to 350 MHz, but optimal phase noise with respect to VCO speed is achieved by running it in the range of 64 to 200 MHz.

POWER DISSIPATION

The AD9861 Tx Path power is derived from four voltage supplies: AVDD, DVDD and DRVDD.

IDRVDD and IDVDD is very dependent on the input data rate, the interpolation rate, and the activation of the internal digital modulator. IAVDD has the same type of sensitivity to data, interpolation rate, and the modulator function but to a much lesser degree (<10%).

SLEEP/POWER-DOWN MODES

The AD9861 provides multiple methods for programmable power saving modes. The externally controlled TxPwrDwn or SPI programmed SLEEP mode and full power down mode are the main options.

TxPwrDwn is used to disable all clocks and much of the analog circuitry in the Tx path when asserted. In the mode, the biases remain active therefore reducing the time required for re-enabling the Tx path. Recovery from power down time for this mode is typically less than 10 us.

The sleep mode, when activated, turns off the DAC output currents but the rest of the chip remains functioning. When coming out of sleep mode, the AD9861 will immediately return to full operation.

A full power-down mode can be enabled through the SPI register, which turns off all Tx path related analog and digital circuitry in the AD9861. When returning from full power-down mode, enough clock cycles must be allowed to flush the digital filters of random data acquired during the power-down cycle.

Interpolation Stage

Interpolation filters are available for use in the AD9861 transmit path, providing 1x(bypassed), 2x, or 4x interpolation.

The interpolation filters effectively increase the Tx data rate while suppressing the original images. The interpolation filters digitally shift the worst case image further away from the desired signal, thus reducing the requirements on the analog output reconstruction filter.

There are two 2x interpolation filters available in the Tx path. An interpolation rate of 4x is achieved using both interpolation filters; an interpolation rate of 2x is achieved by enabling only the first 2x interpolation filter.

The first interpolation filter provides 2x interpolation using a 39 tap filter. It suppresses out-of-band signals by 60 dB or more and has a flat passband response (less than 0.1 dB ripple) extending to 38% of the AD9861 input Tx data rate (19% of the DAC update rate, fDAC). The maximum input data rate is 80 MSPS per channel when using 2x interpolation.

The second interpolation filter will provide an additional 2x interpolation for an overall 4x interpolation. The second filter is a 15 tap filter. It suppresses out-of-band signals by 60 dB or more.

The flat passband response (less than 0.1 dB attenuation) is 38% of the Tx input data rate (9.5% of fDAC). The maximum input data rate per channel is 50 MSPS per channel when using 4x interpolation.

Latch/Demultiplexer

Data for the dual channel Tx path can be latched in parallel through 2 ports in half duplex operations (HD20 mode) or through a single port by interleaving the data (FD, HD10 and Clone modes). See the Flexible Interface section for further description of each mode.

AD9861 AUXILIARY CONVERTERS

Aux DAC

The AD9861 has three 8-bit integrated voltage output Auxiliary Digital to Analog Converters (AuxDACs) which can be used for supplying various control voltages throughout the system such as a VCXO voltage control or external VGA gain control. The AuxDACs are based on a resistor divider network and have independent programmable full scale output of 2.5V, 2.7V, 3.0V or 3.3V. The AuxDAC outputs have an I to V driver that produces a voltage output which settles to +/-1 lsb within 0.5 us. The output driver is capable of sinking or sourcing up to 6 mA. Utilizing this feature requires the SPI to be operational.

The AuxDACs output level is proportional to the straight binary input codes from the appropriate SPI registers. If the Slave Mode register bit is high, slave mode enabled, the AUX DAC(s) update will occur when the appropriate update register is written to. Otherwise, the update will occur at the conclusion of the data being written to the register. Typical maximum settling time for the auxiliary DAC is less than 0.5 us, but is somewhat dependent on load. Other optional controls include an invert register control and a power down option.

Auxiliary ADC

Two auxiliary 10-bit SAR ADCs (AuxADCs) are available for various external signals throughout the system, such as a Receive Signal Strength Indicator (RSSI) function or Temperature Indicator. The AuxADCs can convert at rates up to 5.33 MSPS (0.1875 us maximum conversion time) and have a bandwidth of around 200 kHz. The Aux ADC full scale reference is configurable as PLL_AVDD (supply dependent) or as a supply independent 3.0V or 2.5V based on a internal reference. Additionally, an external reference can be used to drive the full scale level through the AuxADC_Ref pin. On-chip averaging of 2, 4, 8, 16, 32 or 64 samples can be enabled. Utilizing any of these feature requires the SPI to be operational.

The two auxiliary ADCs (AUX ADC A and AUX ADC B) can monitor up to 3 system signals. AuxADCA has multiplexed inputs that controls whether pin AUX_ADCA1 or pin AUX_ADCA2 is connected to the input of Auxiliary ADC A. The multiplexer is programmed through Register xx, SelectA. By default, the register is low, which connects the AUX_ADC_A2 Pin to the input.

The full scale AuxADC reference can be generated from the analog supply (supply dependent), an internal reference or to an external reference. By default, an internal reference buffer provides a full-scale reference for both of the auxiliary ADCs that is equal to the supply voltage for the auxiliary ADCs (PLL_AVDD). For a supply independent internal reference, the Aux ADC Ref Enable and Aux ADC Ref FS registers in 0x17 can be used to enable a 2.5V or 3.0 V reference generator. An external full-scale reference can also be applied to either or both of the AUX ADCs by setting the appropriate bit(s), RefselB for the AUX ADC B and Refsel A for the AUX ADC B in the Register Map. Setting either or both of these bits high will disconnect the internal reference buffer and enable the externally applied reference from the AuxADC_Ref pin to the respective channel(s).

Timing for the auxiliary ADCs is generated from a divided down Rx ADC clock. The divide down ratio is controlled by register 0x23, AuxADC CLK Div register and is used to maintain a maximum clock rate of 64 MHz. By default, the Rx ADC clock is divided by 4. At Rx ADC rate greater than 64 MHz, the AuxADC Clock Div register must be set to divide by 2 or divide by 4. The conversion time, including setup, takes 16 clock cycles.

There are four mode of operating the AuxADC: SPI Operation Mode (default), SPI with External Start Convert Operation Mode, Aux_SPI Operation Mode.
In the default SPI Operation Mode, a conversion is initiated by writing a logic high to one or both of the Start register bits, Register 0xXX (StartA) and (StartB). When the conversion is complete, the straight binary, 10-bit output data of the AUX ADC is written to one of three reserved locations in the register map depending on which auxiliary ADC and which multiplexed input is selected. Because the auxiliary ADCs output 10 bits, two register addresses are needed for each data location.

In the optional SPI with External Start Convert Operation Mode, the conversion is initiated by asserting the AuxSPI_csb and data retrieval is accomplished through the SPI interface (data retrieval is similar to the default operation). The AusSPI_csb can be configured to initiate the conversion of either one of the auxiliary ADCs.

In the optional Aux_SPI Operation Mode, initiating a conversion and retrieving data is accomplished through the a dedicated Auxiliary Serial Port Interface (AUX SPI). The AUX SPI can be configured to allow dedicated access and control of either one of the auxiliary ADCs and is available so that the SPI is not tied up retrieving AuxADC data.

The AUX SPI can be enabled and configured by setting register AUX ADC CTRL. Setting the appropriate Select bit selects which of the multiplexed input is connected to the auxiliary ADC. The AUX SPI consists of a chip select pin (AUX_SPI_csb), a clock pin (AUX_SPI_clk), and a data output pin (AUX_SPI_do). A conversion is initiated by pulsing the AUX_SPI_csb pin low. When the conversion is complete, the data pin, AUX_SPI_do, previously a logic low, will go high. At this point, the user supplies an external clock, previously tied low, no data is present on the first rising edge. The data output bit is updated on the falling edge of the clock pulse and is settled and can be latched on the

next clock rising edge. The data arrives serially, MSB first. The AUX SPI runs up to a rate of 16 MHz.

A summary of the three AuxADC modes of operation are :

1. SPI Operation Mode (default)
2. SPI with External Start Convert Operation Mode
3. Aux_SPI Operation Mode

SPI Operation Mode (default)

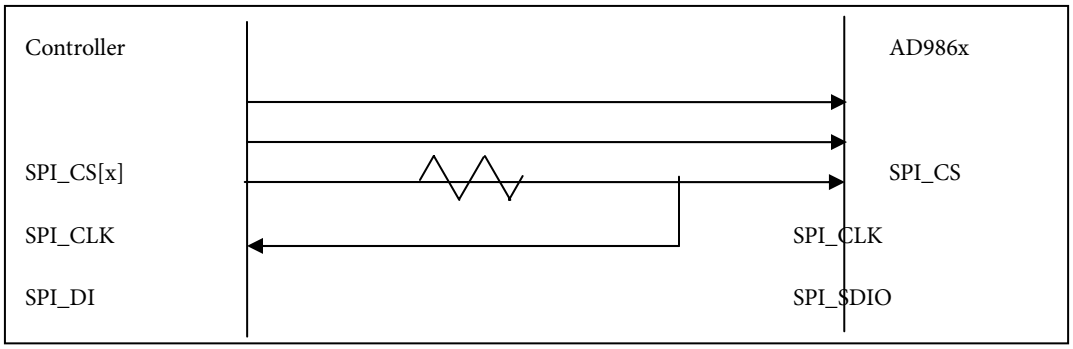
- A number of readings can be averaged by setting the appropriate, Number of Aux ADC Samples register. A maximum of 64 readings can be averaged; the default is 1.
- Setting the appropriate register bit, Start Average Aux ADC, high will initiate the conversion
- Aux_ADC output data will be stored in the appropriate register, Aux ADC

SPI with External Start Convert Operation Mode

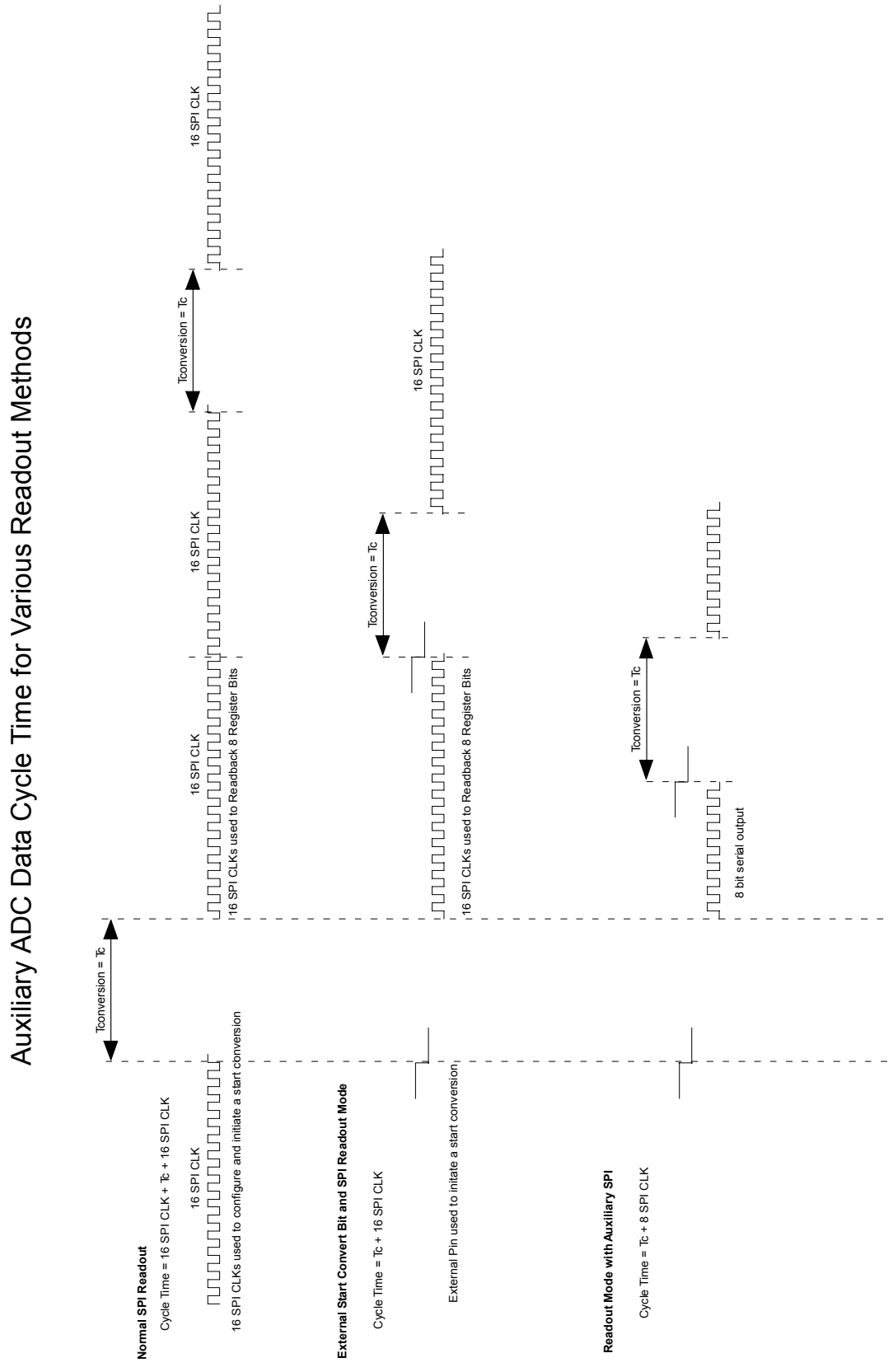
- A number of readings can be averaged by setting the appropriate, Number of Aux ADC Samples register. A maximum of 64 readings can be averaged; the default is 1.
- Setting the appropriate register bit, ???, high will allow an external pin, Aux_SPI_CS, to initiate the conversion.
- The start convert is initiated by applying a rising edge to the Aux_SPI_CS pin (formerly, the ADC_LP pin during the power up cycle)
- Aux_ADC output data will be stored in the appropriate register, Aux_ADC_DATA

Aux_SPI Operation Mode

- For the 64 pin packages, operation of the Aux_SPI requires 3 wire SPI mode to be used (disabling SDO pin). If the Controller is a 4 wire interface, a method of connecting the 3 wire AD986x interface to the 4 wire controller is suggested below.
- The start convert is initiated by applying a rising edge to the Aux_SPI_CS pin (formerly, the ADC_LP pin during the power up cycle)
- A rising edge on the Aux_SPI_DO pin (formerly the SDO pin) indicates a conversion done.
- Supplying a clock to the Aux_SPI_CLK then outputs data on the Aux_SPI_DO pin, MSB first



The timing for each of the 4 Aux_ADC modes of operation are shown below.


Auxiliary ADC Data Cycle Time for Various Readout Methods
Tconversion = Tc
Normal SPI Readout
Cycle Time = 16 SPI CLK + Tc + 16 SPI CLK
16 SPI CLK
16 SPI CLKs used to configure and initiate a start conversion
16 SPI CLK
16 SPI CLKs used to Readback 8 Register Bits
Tconversion = Tc
16 SPI CLK
External Start Convert Bit and SPI Readout Mode
Cycle Time = Tc + 16 SPI CLK
External Pin used to initate a start conversion
16 SPI CLK
16 SPI CLKs used to Readback 8 Register Bits
Tconversion = Tc
Readout Mode with Auxiliary SPI
Cycle Time = Tc + 8 SPI CLK
8 bit serial output

AD9861 DIGITAL BLOCK DESCRIPTION

The AD9861 digital block allows the device to be configured in various timing and operation modes. The following sections discuss the flexible I/O interfaces, the clock distribution block and programming of the device through Mode pins or SPI Registers.

AD9861 FLEXIBLE I/O INTERFACE OPTIONS

The AD9861 can accommodate various data interface transfer options (Flexible I/O). The AD9861 use two 10 bit buses, an upper bus (U10) and a Lower bus (L10) to transfer the dual channel 10 bit ADCs and dual channel 10 bit DACs data by means of interleaved data, parallel data or a mix of both. Below is a graphical look up table that shows the different I/O configurations between the modes depending on half duplex or full duplex operation. After that a table summarizing the pin configuration and a summary of the mode is given.

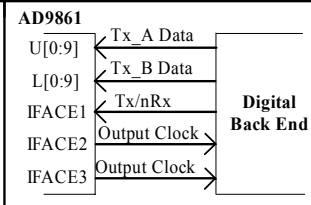
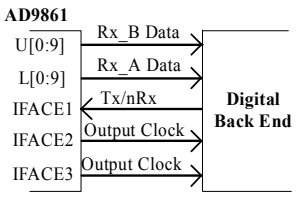
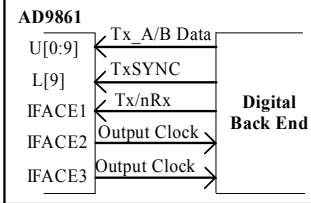
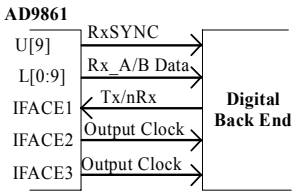
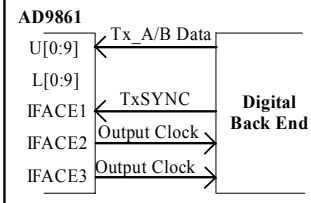
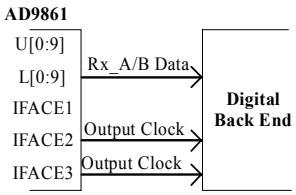
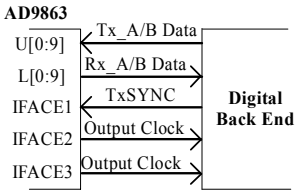
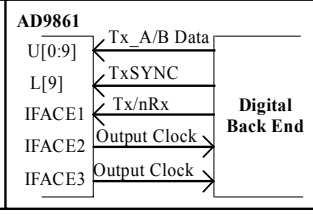
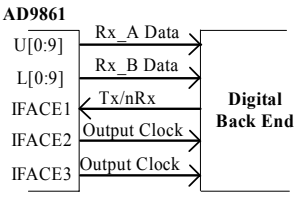
Mode Name	Tx Only Mode (Half Duplex)	Rx Only Mode (Half Duplex)	Concurrent Tx+Rx Mode (Full Duplex)	General Notes
HD20			N/A	Mode Name: HD20 Rx Data Rate = 1 x ADC Sample Rate Two 10 bit Parallel Rx Data Buses Tx Data Rate = 1 x ADC Sample Rate Two 10 bit Parallel Tx Data Buses
HD10			N/A	Mode Name: HD10 Rx Data Rate = 2 x ADC Sample Rate One 10 bit Interleaved Rx Data Bus Tx Data Rate = 2 x ADC Sample Rate One 10 bit Interleaved Rx Data Bus
FD				Mode Name: FD Rx Data Rate = 2 x ADC Sample Rate One 10 bit Interleaved Rx Data Bus Tx Data Rate = 2 x ADC Sample Rate One 10 bit Interleaved Tx Data Bus
Clone			N/A	Mode Name: Clone Rx Data Rate = 1 x ADC Sample Rate Two 10 bit Parallel Rx Data Buses Tx Data Rate = 2 x ADC Sample Rate One 10 bit Interleaved Rx Data Bus Requires SPI interface to configure; similar to AD9860 data interface

Figure #. Graphical illustration of the flexible data interface modes.

	AD9861 Pin Function vs. interface mode [No SPI cases]				
Mode Name	U10	L10	IFACE1	IFACE2	IFACE3
FD	Interleaved Tx Data	Interleaved Rx Data	TxSYNC	Buffered Rx Clock	Buffered Tx Clock
HD10 (Tx/nRx=HI)	Interleaved Tx Data	MSB=TxSYNC Others=Tri-state	Tx/nRx = Tied HI	10/n20 pin control Tied HIGH	Buffered Tx Clock
HD10 (Tx/nRx=LO)	MSB=RxSYNC Other=Tri-state	Interleaved Tx Data	Tx/nRx = Tied LO	10/n20 pin control Tied HIGH	Buffered Rx Clock
HD20 (Tx/nRx=HI)	Tx_A Data	Tx_B Data	Tx/nRx = Tied HI	10/n20 pin control Tied LO	Buffered Tx Clock
HD20 (Tx/nRx=LO)	Rx_B Data	Rx_A Data	Tx/nRx = Tied LO	10/n20 pin control Tied LO	Buffered Rx Clock
Clone Mode (Tx/nRx=HI)	CLONE MODE NOT AVAILABLE WITHOUT SPI				
Clone Mode (Tx/nRx=LO)					

Table #. AD9861 Pin function (when Mode pins are used) relative to I/O mode, and for half duplex modes whether Transmitting or Receiving

	AD9861 Pin Function vs. interface mode [configured through the SPI registers]				
Mode Name	U10	L10	IFACE1	IFACE2	IFACE3
FD	Interleaved Tx Data	Interleaved Rx Data	TxSYNC	Buffered System Clock	Buffered Tx Clock
HD10 (Tx/nRx=HI)	Interleaved Tx Data	MSB=TxSYNC Others=Tri-state	Tx/nRx = Tied HI	Buffered System Clock	Buffered Tx Clock
HD10 (Tx/nRx=LO)	MSB=RxSYNC Other=Tri-state	Interleaved Tx Data	Tx/nRx = Tied LO	Buffered System Clock	Buffered Rx Clock
HD20 (Tx/nRx=HI)	Tx_A Data	Tx_B Data	Tx/nRx = Tied HI	Buffered System Clock	Buffered Tx Clock
HD20 (Tx/nRx=LO)	Rx_B Data	Rx_A Data	Tx/nRx = Tied LO	Buffered System Clock	Buffered Rx Clock
Clone Mode (Tx/nRx=HI)	Interleaved Tx Data	MSB=TxSYNC Others=Tri-state	Tx/nRx = Tied HI	Buffered System Clock	Buffered Tx Clock
Clone Mode (Tx/nRx=LO)	Rx_B Data	Rx_A Data	Tx/nRx = Tied LO	Buffered System Clock	Buffered Rx Clock

Table #. AD9861 Pin function (when SPI programming is used) relative to Flexible I/O mode, and for half duplex modes whether Transmitting or Receiving

Summary of Flexible I/O Modes

FD Mode (using Mode pins, additional flexibility available with SPI capability)

FD mode is the only mode that supports full duplex, receive and transmit concurrent operation. The Upper 10- bit bus (U10) is used to accept Interleaved Tx Data and the Lower 10- bit bus (L10) is used to output Interleaved Rx data. Either the Rx path or the Tx path (or both paths) can be independently powered down using either (or both) the RxPwrDwn and the TxPwrDwn pins. Below are some general notes regarding the FD mode configuration, for more information see the FD Mode description in the next section.

General Tx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
Interpolation Rate (and PLL clock multiplication factor) of 2x or 4x programmed with Mode pins or SPI
Max DAC Update Rate = 200 MSPS, Max Tx Input Data Rate = 80 MSPS/channel (160 MSPS interleaved)
TxSYNC is used to direct Tx Input Data; TxSYNC=HI indicates channel Tx_A data, LO indicates Tx_B data
Buffered Tx Clock Output (from IFACE3 pin) equals 2 times the DAC update rate; 1 rising edge per interleaved Tx sample.

General Rx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
ADC CLK Div Register can be used to divide down the Clock input (CLKIN) before the ADC, which accepts 1 MHz to 50 MHz input (AD9861-50) or 1 MHz to 80 MHz (AD9861-80)
Max ADC sampling rate = 50 MSPS (AD9861-50) OR 80 MSPS (AD9861-80)
Output Data rate = 2 times ADC sample rate = 2 x CLKIN
Buffered Rx Clock Output (from IFACE2 pin) equal phase delayed CLKIN1 and is aligned with Rx output data
Rx path data output at 2 time CLKIN; 2 Rx path data outputs per 1 Buffered Rx Clock Output cycle
Rx_A output while IFACE2 logic level = HI; Rx_B output when IFACE2 logic level = LO

HD10 Mode (using Mode pins, additional flexibility available with SPI capability)

HD10 mode supports half duplex only operations and can interface to a single 10 bit data bus with independent Rx and Tx synchronization pins (RxSYNC and TxSYNC). Both the U10 and L10 buses are used on the AD9861, but the logic level of the Tx/nRx selector (controlled through IFACE1 pin) is used to disable and tri-state the unused bus allowing U10 and L10 to be tied together. The MSB of the unused bus acts as the RxSYNC (during Rx operation) or TxSYNC (during Tx operation). A single pin is used to output the clocks for Rx and Tx data latching (from the IFACE3 pin) switching depending which path is enabled. Below are some general notes regarding the HD10 mode configuration, for more information see the HD10 Mode description in the next section.

General Tx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
Interpolation Rate (and PLL clock multiplication factor) of 2x or 4x programmed with Mode pins or SPI
Interleaved Tx Data accepted on U10 bus, L10 bus MSB acts as TxSYNC
Max DAC Update Rate = 200 MSPS, Max Tx Input Data Rate = 80 MSPS/channel (160 MSPS interleaved)
TxSYNC is used to direct Tx Input Data; TxSYNC=HI indicates channel Tx_A data, LO indicates Tx_B data
Buffered Tx Clock Output (from IFACE3 pin) equals 2 times CLKIN2; 1 rising edge per interleaved Tx sample.

General Rx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
ADC CLK Div Register can be used to divide down the Clock input (CLKIN) before the ADC, which accepts 1 MHz to 50 MHz input (AD9861-50) or 1 MHz to 80 MHz (AD9861-80)
Max ADC sampling rate = 50 MSPS (AD9861-50) OR 80 MSPS (AD9861-80)
Output Data rate = 2 times ADC sample rate = 2 x CLKIN
Interleaved Rx data output from L10 bus
Buffered Rx Clock Output (from IFACE3 pin) equal phase delayed CLKIN
Rx path data output at 2 time CLKIN1; 2 Rx path data outputs per 1 Buffered Rx Clock Output cycle
Rx_A output while IFACE3 logic level = HI; Rx_B output when IFACE2 logic level = LO

HD20 Mode (using Mode pins, additional flexibility available with SPI capability)

HD20 mode supports half duplex only operations and can interface to a single 20 bit data bus (two parallel 10 bit buses). Both the U10 and L10 buses are used on the AD9861, but the logic level of the Tx/nRx selector (controlled through IFACE1 pin) is used to configure the buses as Rx outputs (during Rx operation) or as Tx inputs (during Tx operation). A single pin is used to output the clocks for Rx and Tx data latching (from the IFACE3 pin) switching depending which path is enabled. Below are some general notes regarding the HD20 mode configuration, for more information see the HD20 Mode description in the next section.

General Tx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
Interpolation Rate (and PLL clock multiplication factor) of 1x, 2x or 4x programmed with Mode pins
Max DAC Update Rate = 200 MSPS, Max Tx Input Data Rate = 200 MSPS/channel, bypassed interpolation filters; 80 MSPS for 2x or 4x interpolation
Buffered Tx Clock Output (from IFACE3 pin) is a buffered version of CLKIN
Tx_A output on U10 bus; Tx_B output on L10 bus

General Rx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
ADC CLK Div Register can be used to divide down the Clock input (CLKIN) before the ADC, which accepts 1 MHz to 50 MHz input (AD9861-50) or 1 MHz to 80 MHz (AD9861-80)
Max ADC sampling rate = 50 MSPS (AD9861-50) OR 80 MSPS (AD9861-80)
Output Data rate = ADC sample rate (= CLKIN1); two 10 bit parallel outputs per 1 Buffer Rx Clock Output cycle
Rx_A output on L10 bus; Rx_B output on U10 bus

Clone Mode (requires SPI programming)

Clone mode enables a half duplex interface similar to the AD9860 data interface. It provide parallel Rx data output (20 bits) while in Rx mode, and accepts interleaved Tx data (10 bit) while in Tx mode. Both the U10 and L10 buses are used on the AD9861, but the logic level of the Tx/nRx selector (controlled through IFACE1 pin) is used to configure the buses for Rx outputs (during Rx operation) or as Tx inputs (during Tx operation). A single pin is used to output the clocks for Rx and Tx data latching (from the IFACE3 pin) depending upon which path is enabled. Below are some general notes regarding the Clone mode configuration, for more information see the Clone Mode description in the next section.

General Tx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
Interpolation Rate (and PLL clock multiplication factor) of 2x or 4x programmed with Mode pins
Max DAC Update Rate = 200 MSPS, Max Tx Input Data Rate = 80 MSPS/channel (160 MSPS interleaved)
TxSYNC is used to direct Tx Input Data; TxSYNC=HI indicates channel Tx_A data, LO indicates Tx_B data
Buffered Tx Clock Output (from IFACE3 pin) equals 2 times CLKIN; 1 rising edge per interleaved Tx sample.

General Rx Path Notes:

Clock input (CLKIN) accepts 16 MHz to 80 MHz (2x interpolation) OR 8 MHz to 50 MHz (4x interpolation)
With SPI the PLL can be bypassed, in which case CLKIN accepts a master clock between 1 MHz to 200 MHz
ADC CLK Div Register can be used to divide down the Clock input (CLKIN) before the ADC, which accepts 1 MHz to 50 MHz input (AD9861-50) or 1 MHz to 80 MHz (AD9861-80)
Max ADC sampling rate = 50 MSPS (AD9861-50) OR 80 MSPS (AD9861-80)
Output Data rate = ADC sample rate (= CLKIN); two 10 bit parallel outputs per 1 Buffer Rx Clock Output cycle
Rx_A output on L10 bus; Rx_B output on U10 bus

CONFIGURING WITH MODE PINS

The Flexible interface can be configured with or without the SPI, although more options and flexibility are available when using the SPI to program the AD9861. Mode pins can be used to power down sections of the device, reduce overall power consumption, configure the flexible I/O interface and program the interpolation setting. The SPI register map which provides many more options is discussed in the SPI Register section.

Mode Pins / Power Up Configuration options:

There are various options that are configurable at power up through mode pins and also control pins for power down modes. The logic value of the configuration mode pins are latched when the device is brought out of reset (rising edge of RESETb). The mode pin names and there function are shown in the table below.

Pin Name	Duration	Function
RxPwrDwn	Permanent	When high, digital clocks to Rx block are disabled. Analog Blocks that require <10 us to power up are powered off.
TxPwrDwn	Permanent	When high, digital clocks to Tx block are disabled (PLL remains powered to maintain output clock with an optional SPI shut off). Analog Blocks that require <10 us to power up are powered off.
Tx/nRx	Permanent only for HD Flex I/O interface	When high, digital clocks to Tx block are disabled (PLL remains powered to maintain output clock with an optional SPI shut off). Tx Analog Blocks remain powered up unless Tx_PwrDwn is asserted. When low, digital clocks to Rx block are disabled. Rx Analog Blocks remain powered up unless Rx_PwrDwn is asserted.
ADC_LoPwr	Defined at RESET or Power Up	When enabled, this bit scales the ADC power down by 40%.
SPI_Bus_Enable	Defined at RESET or Power Up	This pin must remain low to maintain Mode pin functionality (the SPI port remains nonfunctional).
FD/nHD	Defined at RESET or Power Up	Configures the Flex I/O for FD or HD mode
10/n20 only valid for HD mode	Defined at RESET or Power Up	If the Flex I/O bus is in HD mode, this bit is used to configure parallel or interleaved data mode.
Interp0 and Interp1	Defined at RESET or Power Up	These bits configure the PLL and interpolation rate to 1x, 2x or 4x

Configuring Using Mode Pins

ADC Low Power Mode Option

- ADC_LP is latched during the rising edge of RESET
  - A logic low setting results in ADC operation at nominal power mode
  - A logic high setting results in ADC consuming 40% less power than the nominal power mode

Flex I/O Configuration

- FD/nHD (SDO) is latched during the rising edge of RESET

- A logic low setting identifies that the DUT Flex I/O port will be configured for Half Duplex operation
  - 10/n20 (IFACE2) is also latched during the rising edge of RESET to identify interleaved data mode or parallel data modes
    - A logic low indicates that the Flex I/O will configure itself for parallel data mode
    - A logic high indicates that the Flex I/O will configure itself for interleaved data mode

Interpolation/PLL Factor Configuration

- SPI_CS is latched during the rising edge of RESET
  - A logic low setting results in the SPI being disabled and SPI_DIO, SPI_CLK and SPI_SDO will be acting as mode pins controlling Tx Interpolation rate and PLL setting
    - SPI_DIO and SPI_CLK config the Tx path for 1x, 2x or 4x interpolation (also enabling the PLL of the same multiplication factor)
  - A logic high setting results in the SPI being fully operational

Power Down Controls

- RxPwrDwn logic level controls the power down function of the Rx Path
  - A logic low setting will result in the Rx path operating at normal power levels
  - A logic high setting disables the ADC clock and disable some bias circuitry to reduce power consumption
- TxPwrDwn logic level controls the power down function of the Tx Path
  - A logic low setting will result in the Tx path operating at normal power levels
  - A logic high setting disables the DAC clocks and disable some bias circuitry to reduce power consumption
- Tx/nRx pin enables the appropriate Tx or Rx path in the Half Duplex modes
  - A logic low disables the Tx digital clock and the I/O port will be outputs
  - A logic high disables the Rx digital clocks and the I/O port will be a high impedance input

AD9861 CLOCK DISTRIBUTION BLOCK

The AD9861 utilizes a PLL clock multiplier circuit and an internal distribution block to generate all required clocks for various timing configurations. The AD9861 has 2 independent clock paths, one primarily used to drive the Rx ADCs and the other primarily used to drive the TxDACs and Tx digital processing blocks. There are 2 options to generate the needed clocks for the AD9861, the "Normal Timing Operation" Mode and the "Alternative Timing Operation" Mode. A block diagram of the Clock Tree and the Data Path are shown in the figures below. Many of the options require SPI programmability. Some features of the AD9861 Clock Tree:

- The PLL has 2 controllable variables to configure a multiplication factor. One setting controls a divide by 1 or 5, and the other controls a multiply by 1, 2, 4, 8 or 16.
- The Rx path has an independent divide by 1, 2 or 4 control for flexibility purposes.
- In the alternative timing mode, the PLL can be used to drive the Rx ADCs (expecting lower performance due to clock jitter).

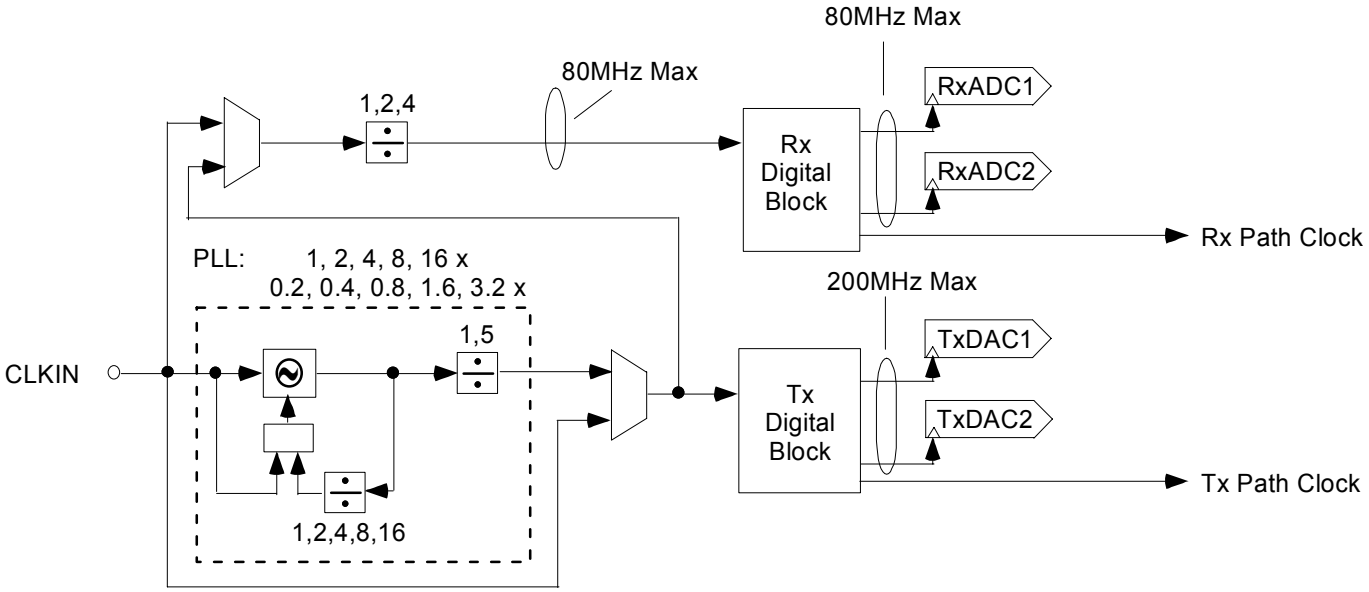


Figure ##. Clock Distribution Block Diagram

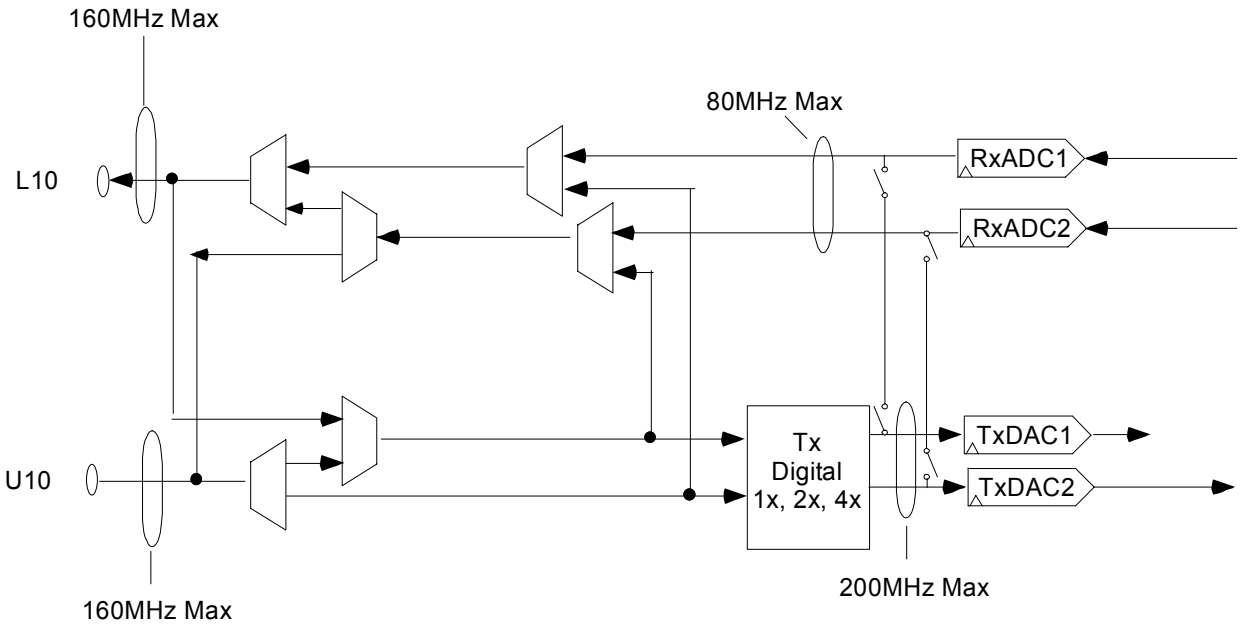


Figure ##. Data Path Block Diagram

TIMING DIAGRAMS

SPI REGISTER MAP

The Registers for the AD9861 are used to control a number of features to provide flexible operation of the device. The SPI allows access to many configurable options and information, including:

- SPI Setup: 3 wire mode, LSB First Mode, Soft Reset
- Rx Path Setup: Power Down of various Rx path blocks/channels, 2's Complement, Clock Duty Stabilizer
- Tx Path Setup: Power Down of various Tx path blocks/channels, Tx Offset Control, Fine Gain Control, Coarse Gain Control, PGA Control, Gain update slaved to Tx power down, Q/I order, 2's Compl, Inverse Sample
- Clock setup: PLL multiply factor, Rx CLKOUT divide factor, Tx CLKOUT divide factor, Invert Rx CLKOUT, Inv Tx CLKOUT, single clock input mode, Input clock control? (crystal or source),
- Aux ADC: start convert signal, mux position, Data values (10 bit), number of samples to average, enable Aux SPI, allow external start convert, slow Aux ADC clock
-Aux DAC: Update slaved to Tx Power Down, data values (10 bit)

A Register map consist of register from 0x00 to 0x29 and can be seen below:

Register Name	Reg Add	7	6	5	4	3	2	1	0
General	0	SDIO BiDir	LSB first	Soft reset					
Clock Mode	1	clk_mode[2:0]						Inv clkout (IFACE3)	
Power Down	2	Tx Analog			TxDigital	RxDigital	PLL Power Down	PLL Output Disable	
RxA Power Down	3	Rx_A Analog	Rx_A DC Bias						
RxB Power Down	4	Rx_B Analog	Rx_B DC Bias						
Rx Power Down	5	Rx Analog Bias	VREF1	VREF, DIFF	VREF2				
	6			Rx_A Twos Compliment	Rx_A Clk Duty				
	7			Rx_B Twos Compliment	Rx_B Clk Duty				
	0B	DAC A Offset [9:2]							
	0C	DAC A Offset [1:0]							DAC A Offset Direction
	0D	DAC A Coarse Gain Control		DAC A Fine Gain [5:0]					
	0E	DAC B Offset [9:2]							
	0F	DAC B Offset [1:0]							DAC B Offset Direction
	10	DAC B Coarse Gain Control		DAC B Fine Gain [5:0]					
	11	TxPGA Gain [7:0]							
Tx Misc	12		TxPGA Slave Enable		TxPGA Fast Update				
	13	Tx Twos Compliment	Rx Twos Compliment	Tx Inverse Sample	Rx Data Interleaved	Tx Data Interleaved		Interpolation Control [1:0]	
	14			Dig Loop On	SpiFDnHD	SpiTxnRx	SpiB10n20	SPI IO Control	SpiClone
	15	PLL Bypass	ADC Clock Div[1:0]		Alt Timing Mode	PLL Div5	PLL Multiplier [2:0]		
	16	PLL Lock Bypass	PLL Lock Force	PLL User Detect			PLL Slow		
	17	Aux DAC A FS [1:0]		Aux DAC B FS [1:0]		Aux DAC C FS [1:0]		Aux ADC Ref Enable	Aux ADC Ref FS
	18	Start Average Aux ADC A					Number of Aux ADC A Samples [2:0]		
	19	Start Average Aux ADC B					Number of Aux ADC B Samples [2:0]		
	1A	Aux ADC A2 [1:0]							
	1B	Aux ADC A2 [9:2]							
	1C	Aux ADC A1 [1:0]							
	1D	Aux ADC A1 [9:2]							

	20	Aux ADC B [1:0]							
	21	Aux ADC B [9:2]							
	22	Aux SPI Enable	Sel BnotA	Refsel B		Start B	Refsel A	Select A	Start A
	23							AuxADC Clock Div[1:0]	
	24	Aux DAC A[7:0]							
	25	Aux DAC B[7:0]							
	26	Aux DAC C[7:0]							
	28	Slave Enable					Update C	Update B	Update A
	29						Power Up C	Power Up B	Power Up A

REGISTER BIT DEFINITIONS

REGISTER 0: GENERAL

BIT 7: SDIO BiDir (Bidirectional)

Default setting is low, which indicates SPI serial port uses dedicated input and output lines (i.e., 4-wire interface), SDIO and SDO Pins, respectively. Setting this bit high configures the serial port to use the SDIO Pin as a bidirectional data pin.

BIT 6: LSB First

Default setting is low, which indicates MSB first SPI Port Access Mode. Setting this bit high configures the SPI port access to LSB first mode.

BIT 5: Soft Reset

Writing a high to this register resets all the registers to their default values and forces the PLL to relock to the input clock. The Soft Reset Bit is a one shot register and is cleared immediately after the register write is completed.

REGISTER 1: ???

BIT 7-5: Clk Mode

These bits represent the clocking interface for the various modes. Setting 000 is default. Setting 111 is used for Clone mode (see Flex IO section for definition of Clone Mode).

	Modes
000	Standard FD, HD10, HD20 Clock modes
001	Optional FD timing
010	Not Used
011	Optional HD10 timing
100	Not Used
101	Optional HD20 timing
110	Not Used
111	Clone Mode

Bit 1: Inv clkout (IFACE3)

Invert the output clock on IFACE3

REGISTER 2: ???

BIT 7-5: Tx Analog (Power-Down)

Three options are available to reduce analog power consumption for the Tx channels. The first two options disable the analog output from Tx channel A or B independently, and the third option disables the output of both channels and reduces the power consumption of some of the additional analog support circuitry for maximum power savings. With all three options, the DAC bias current is not powered d own so recovery times are fast (typically a few clock cycles). The list below explains the different modes and settings used to configure them.

Power-Down Option Bits Setting [7:5]

Power-Down Tx A Channel Analog Output [1 0 0]
Power-Down Tx B Channel Analog Output [0 1 0]
Power-Down Tx A and Tx B Analog Outputs [1 1 1]

BIT 4: Tx Digital (Power-Down)

By default this bit is low, enabling the transmit path digital to operate as programmed through other registers. By setting this bit high, the digital blocks are not clocked to reduce power consumption. When enabled, the Tx outputs will be static, holding their last update values.

BIT 3: Rx Digital (Power-Down)
Setting this bit high will power down the digital section of the receive path of the chip. Typically, any unused digital blocks are automatically powered down.
BIT 2: PLL Power-Down
Setting this register bit high forces the CLKIN multiplier to a power-down state. This mode can be used to conserve power or to bypass the internal PLL. To operate the AD9861 when the PLL is bypassed, an external clock equal to the fastest on-chip clock is supplied to the CLKIN.
BIT 1: PLL Output Disable
Setting this register bit high disconnects the PLL output from the clock path. If the PLL is enabled it will lock or stay locked as normal.

REGISTER 3/4: ???
BIT 7/7: Rx_A Analog/Rx_B Analog (Power-Down)
Either ADC or both ADCs can be powered down by setting the appropriate register bit high. The entire Rx channel is powered down, including the differential references, input buffer, and the internal digital block. The bandgap reference remains active for quick recovery.
BIT 6/6: Rx_A DC Bias/Rx_B DC Bias (Power-Down)
Setting either of these bits high will power down the dc bias network for the respective channel and requires an input signal to be properly dc biased. By default, these bits are low and the Rx inputs are self biased and accept an AC coupled input.

REGISTER 5: ???
BIT 7: Rx Analog Bias (Power-Down)
Setting this bit high powers down all analog bias circuits related to the receive path (including the differential reference buffer). Since bias circuits are powered down, an additional power saving, but also a longer recovery time relative to other Rx power down options will result.
BIT 6: VREF1 (Power-Down)
Setting this register bit high, along with VREF2 bit, will power down the ADC reference circuit (i.e., VREF). Powering down the Rx Bandgap reference will allow an external reference to drive the Vref pin setting full scale range of the Rx paths.
BIT 5: VREF, DIFF(Power-Down)
Setting this bit high will power down the ADC's differential references (i.e., REFT and REFB). Recovery time will depend on REFT and REFB decoupling caps size and amount of
BIT 4: VREF2 (Power-Down)
Setting this register bit high, along with VREF1 bit, will power down the ADC reference circuit (i.e., VREF). Powering down the Rx Bandgap reference will allow an external reference to drive the Vref pin setting full scale range of the Rx paths.

REGISTER 6/7: ???
BIT 5: Rx_A Twos Complement/ Rx_B Twos Complement
Default data format for the Rx data is straight binary. Setting this bit high will generate two's complement data.
BIT 4: Rx_A Clk Duty/ Rx_B Clk Duty
Setting either of these bits high enables the respective channels on-chip duty cycle stabilizer (DCS) circuit to generate the internal clock for the Rx block. This option is useful for adjusting for high speed input clocks with skewed duty cycle. The DCS Mode can be used with ADC sampling frequencies over 40 MHz.

REGISTER 0B/0C/0E/0F: DAC OFFSET A/B
DAC A/DAC B Offset
These 10-bit, twos complement registers control a dc current offset that is combined with the Tx A or Tx B output signal. An offset current of up to ±12% IOUTFS (2.4 mA for a 20 mA fullscale output) can be applied to either differential pin on each channel. The offset current can be used to compensate for offsets that are present in an external mixer stage, reducing LO leakage at its output. Default setting is hex00, no offset current. The offset current magnitude is set using the lower nine bits. Setting the MSB high will add the offset current to the selected differential pin, while an MSB low setting will subtract the offset value.
DAC A/DAC B Offset Direction
This bit determines to which of the differential output pins for the selected channel the offset current will be applied. Setting this bit low will apply the offset to the negative differential pin. Setting this bit high will apply the offset to the positive differential pin.

REGISTER 0D/10: ????
BIT 7, 6: DAC A/DAC B Coarse Gain Control
These register bits will scale the full-scale output current (IOUTFS) of either Tx channel independently. IOUT of the Tx channels is a function of the RSET resistor, the TxPGA setting, and the Coarse Gain Control setting.

00	Output current scaling by 1/11
01	Output current scaling by ½
10	No output current scaling
11	No output current scaling

BIT 5–0: DAC A/DAC B Fine Gain
The DAC output curve can be adjusted fractionally through the Gain Trim Control. Gain trim of up to ±4% can be achieved on each channel individually. The Gain Trim register bits are a twos complement attention control word.
MSB, LSB
100000 Maximum positive gain adjustment
111111 Minimum positive gain adjustment
000000 No adjustment (default)
000001 Minimum negative gain adjustment
011111 Maximum negative gain adjustment

REGISTER 11: TxPGA GAIN
BIT 0–7: TxPGA Gain
This 8 bit, straight binary (Bit 0 is the LSB, Bit 7 is the MSB) register controls for the Tx programmable gain amplifier (TxPGA). The TxPGA provides a 20 dB continuous gain range with 0.1 dB steps (linear in dB) simultaneously to both Tx channels. By default, this register setting is hex00.
MSB, LSB
000000 Minimum gain scaling –20 dB
111111 Maximum gain scaling 0 dB

REGISTER 12: Tx MISC
BIT 6: TxPGA Slave Enable
The TxPGA Gain is controlled through register TxPGA Gain setting and by default is updated immediately after the register write. If this bit is set, the TxPGA Gain update is synchronized with the falling edge of a signal applied to the TxPwrDwn pin and is enabled during the wakeup from Power Down.
BIT 4: TxPGA Fast Update (Mode)
The TxPGA Fast bit controls the update speed of the TxPGA. When Fast Update mode is enabled, the TxPGA provides fast gain settling within a few clock cycles (which may introduce spurious signals at the output of the Tx Path). Default setting for this bit is low and the TxPGA gives a smooth transition between gain settings. Fast mode is enabled when this bit is set high.

REGISTER 13: ????
BIT 7: Tx Twos Complement
The default data format for Tx data is straight binary. Set this bit high when providing twos complement Tx data.
BIT 6: Rx Twos Complement
The default data format for Rx data is straight binary. Set this bit high when providing twos complement Rx data.
BIT 5: Tx Inverse Sample
By default, the transmit data is sampled on the rising edge of the CLKOUT. Setting this bit high will change this, and the transmit data will be sampled on the falling edge.
BIT 4: Rx Data Interleaved
This bit can be used to configure the Rx data port to output interleaved data, overriding the I/O configuration setup through the Mode pins.
BIT 3: Tx Data Interleaved
This bit can be used to configure the Tx data port to accept interleaved data, overriding the I/O configuration setup through the Mode pins.
BIT 1,0: Interpolation Control
These register bits control the interpolation rate of the transmit path. Default settings are both bits low, indicating that both interpolation filters are bypassed. The MSB and LSB are address Bits 1 and 0, respectively. Setting binary 01 provides an interpolation rate of 2x; binary 10 provides an interpolation rate of 4x.

REGISTER 14: ????
BIT 5: Dig Loop On
When enabled this bit enables a digital loop back mode. The digital loop back mode provides a means of testing digital interfaces and functionality at the system level. In digital loop back mode, the full duplex interface must be enabled (see Flexible I/O

section). The device will accept digital input bus according to the FD mode timing and exercise the Tx digital path (with enabled interpolation and other digital settings); the processed data will then be output from the Rx path bus.

BIT 4: SPI_FDnHD

Control bit to configure full duplex (high) or half duplex (low) interface mode. This register setting requires a SPI IO Control register to be enabled.

BIT 3: SpiTxnRx

Control bit for transmit or receive mode. HIGH represents TX and LOW represents RX

Bit 2: SpiB10n20

Control bit for 10 or 20 bit mode. HIGH represents 10 bit and LOW represents 20 bit

Bit 1: SPI IO Control

Use this bit in conjunction with **SpiTxnRx** to overide external TxnRx pin operation.

Bit 0: SpiClone

Set HIGH when in clone mode (see Flexible IO section for definition of Clone mode). Clk_mode should also be set to binary 111 (ie: Reg01[7:5] = 111)

REGISTER 15: ???

BIT 7: PLL_Bypass

Setting this bit high will bypass the PLL. When bypassed, the PLL will remain active.

BIT 6,5: ADC Clock Div [1:0]

For the AD9861, by default the ADCs are driven directly from CLKIN in Normal Timing Operation or from the PLL output clock in the Alternative Timing Operation. These bits are used to divide the source of the ADC clock prior to the ADCs. A [00] setting performs no division, the [01] setting divides the clock by 2, the [10] setting divides the clock by 4 and the [11] setting is not used.

BIT 4: Alt Timing Mode

The timing section in the data sheet describes two timing modes, the "Normal Timing Operation" and the "Alternative Timing Operation" modes. The default configuration is Normal timing mode and for the AD9861, the CLKIN drives the Rx path. In the Alternative Timing Mode the PLL output is used to drive the Rx path. The Alternative Operation mode is configured by setting this bit high.

BIT 3: PLL Div5

The output of the PLL can be divided by 5 by setting this bit high. By default, the PLL directly drives the Tx Digital path with no division of its output.

BIT 2-0: PLL Multiplier

These bits control the PLL multiplication factor. A default setting is binary 000 which will configure the PLL to 1x multiplication factor. This register, in combination with the PLL Div10 register, sets the PLL output frequency. The programmable multiplication factors are:

000 > 1 x
001 > 2 x
010 > 4 x
011 > 8x
100 > 16 x
101 > 32 x
110 and 111 >> not used

REGISTER 16: ???

BIT 7: PLL Lock Bypass

In the Alternative Timing mode, a PLL lock detect signal is used to gate an output clock (IFACE2 pin). Setting this bit high will force the PLL lock detect signal high after the 32 input clock cycles. This is required when configuring the PLL near its min or maximum frequency when PLL Lock detect signal may become intermittent.

BIT 6: PLL Lock Force

In the Alternative Timing mode, a PLL lock detect signal is used to gate an output clock (IFACE2 pin). Setting this bit high will force the PLL lock detect signal high with no delay. This may be required when configuring the PLL near its min or maximum frequency when PLL Lock detect signal may become intermittent.

BIT 5: PLL User Detect

Flipping this bit HIGH will manually tell the PLL to switch between fast and slow clocks in IPW mode. Only valid if Register 16, bit 6 is HIGH.

BIT 2: PLL Slow

For low input clocks (< 32 MHz) to the PLL, this bit will decrease the bandwidth helping the PLL remain locked.

REGISTER 17: ???

BIT 7-2: Aux DAC A FS / Aux DAC B FS / Aux DAC C FS

These register bits will scale the full-scale output voltage for the Aux DACs independently. If the Full scale voltage is programmed to a value greater than PLL_VDD – 0.2 V, the Aux DAC will become non-linear in this region.

MSB, LSB	Aux DAC Full Scale output voltage
00	3.0 V
01	3.3 V
10	2.5 V
11	2.7 V

BIT 1: Aux ADC Ref Enable

This bit enables the Aux ADC on chip, supply independent reference generator. By default, the Aux ADC uses the PLL_AVDD supply for its full scale voltage level.

BIT 0: Aux ADC Ref FS

When the Aux ADC Ref Enable bit is set high, this bit allows the user to select the full scale value of the Aux ADC. A low setting sets the full scale value to 3.0 V; a high setting sets the full scale value to 2.5 V. If the Full scale voltage is programmed to a value greater than PLL_VDD – 0.2 V, the Aux ADC will not be linear in this region.

REGISTER 18/19 : ???

BIT 7: Start Average Aux ADC A / Start Average Aux ADC B

These registers are used to initiate a conversion cycle of the Aux ADCs for a number of consecutive samples and than report the average result. This is a one shot register, meaning it will always reset itself to a logic low and will wait and use a logic high setting as a trigger. The number of consecutive samples are programmed in the Number of Aux ADC A/B Samples register. The external pin Aux_SPI_CS can be configured to allow it to initiate the Start Average conversion cycle. The result will be placed in the appropriate register corresponding to the Aux ADC output (register 0x1A to 0x21).

BIT 7: Number of Aux ADC A / B Samples

These bits control the number of samples the Aux ADC will collect and use to calculate an average value. This register is used in conjunction with the Start Average Aux ADC register.

MSB, LSB	Number of samples to average
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	Not Used

REGISTER 1A-21: AUX ADC A2, A1, B Data

These 10-bit, offset binary registers are read only and store the last corresponding Aux ADC output values. The AD9861 has two auxiliary ADC SAR converters., called Aux ADC A and Aux ADC B. Aux ADC A has a multiplexed input which allows the user to select either input using the Sel 2not1 register. The 10 bits are broken into two registers, one containing the upper eight bits and the other containing the lower two bits.

REGISTER 22: AUX ADC CONTROL

BIT 7: Aux SPI (Enable)

Enables the Auxiliary SPI which can be used to initiate a conversion and read back one of the Aux ADCs. To use the Aux_SPI to access the AuxADC, it is required to configure the standard SPI as a 3 wire interface by setting Register 0x00 bit 7.

BIT 6: Sel BnotA

If the auxiliary Serial port is used, this bit selects which Auxiliary ADC, A or B, will be using the dedicated Auxiliary Serial port. The Auxiliary Serial port by default (low setting) controls Auxiliary ADC A. Setting this bit high will allow the Auxiliary Serial Port to control Auxiliary ADC B.

BIT 5, 2: Refsel B/A

By default, the auxiliary ADCs use an external reference applied to the AUX_REF pin. This voltage will act as the full-scale reference for the selected auxiliary ADC. Either auxiliary ADC can use an internally generated reference, which can be a buffered version of the analog supply voltage or a supply independent, 3.0 V or 2.5 V internal reference. To enable use of the internal reference for either of the auxiliary ADCs, the respective Refsel register should be set high. For internal reference configuration, see register 17.

BIT 1: Select A

This bit is used to select which of the two inputs will be connected to the auxiliary ADC. By default (setting low), the AUX_ADC_A2 pin is connected to Auxiliary ADC A. Setting the respective bit high will connect the AUX_ADC_A1 pin to Auxiliary ADC A.

BIT 3, 0: Start B/A

Setting a high bit to either of these registers initiates a conversion of the respective auxiliary ADC, A or B. The register bit always reads back a low.

REGISTER 23: ???
BIT 1,0: AuxADC Clock Div
The auxiliary ADCs clock can be based on either the clock driving the Rx ADC or it can be driven from the SPI_CLK. The conversion rate of the auxiliary ADCs should be less than 40 MHz. In order to facilitate a slower speed clock for the Aux ADC these bits are used to divide down the Rx ADC clock prior to driving the Aux ADC. These following options are programmable through this register:

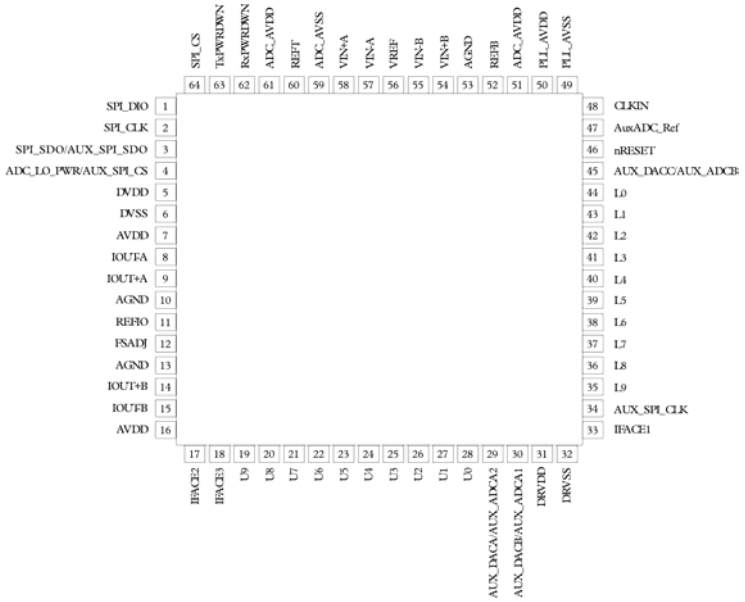
MSB, LSB	Aux ADC sampling rate
00	Rx ADC Clock / 4
01	Rx ADC Clock / 2
10	Rx ADC Clock
11	SPI_CLK drives Aux ADC

REGISTER 24, 25, 26: AUX DAC A/B/C
Auxiliary DAC A, B, and C Output Control Word
Three 8-bit, straight binary words are used to control the output of three on-chip auxiliary DACs. The auxiliary DAC output changes take effect immediately after any of the serial write is completed. The DAC output control words have default values of 0. The smaller programmed output controlled words correspond to lower DAC output levels.

REGISTER 28: ???
BIT 7: Slave Enable
A low setting (default) updates the auxiliary DACs after the respective register is written to. To synchronize the auxiliary DAC outputs to each other, a slave mode can be enabled by setting this bit high and then setting a high to the appropriate update registers.
BIT 2/1/0: Update C, B, and A
Setting a high bit to any of these registers initiates an update of the respective Auxiliary DAC, A, B, or C, when Slave mode is enabled using the Slave Enable register. The register bit is a one shot and always reads back a low. Note: be sure to keep the Slave Enable bit high when using the auxiliary DAC synchronization option.

REGISTER 29: AUX DAC POWER-DOWN
BIT 2/1/0: Power Up C, B, and A
Setting any of these bits high will power up the appropriate auxiliary DAC. By default, these bits are low and the auxiliary DACs are disabled.

AD9861 PIN CONFIGURATION



Pin #	Pin Name	Description
1	SPI_DIO (Interp1)	Serial Port Data Input (OR if no SPI: Tx Interpolation bit MSB)
2	SPI_CLK (Interp0)	Serial Port Shift Clock (OR if no SPI: Tx Interpolation bit LSB)
3	SPI_SDO / AuxSPI_SDO (FD/nHD)	4 wire Serial Port Output / SDO for AuxSPI (OR if no SPI Full or Half Duplex Config)
4	ADC_LO_PWR / Aux_SPI_CS	ADC Low Power Mode enable defined at power up / CS for AuxSPI
5, 31	DVDD	Digital Supply
6, 32	DVSS	Digital Ground
7, 16, 50, 51, 61	AVDD	Analog Supply
8, 9	IOUT-A, IOUT+A	DAC A differential output
10, 13, 49, 53, 59	AGND	Analog Ground
11	REFIO	TxDAC bandgap reference decoupling pin
12	FSADJ	Tx DAC Full scale adjust pin
14, 15	IOUT+B, IOUT-B	DAC B differential output
17	IFACE2	**SPI** : Buffered CLKIN (can be configured to be system clock output) **No SPI** : ***FD*** >> Buffered CLKIN; ***HD20*** or ***HD10*** >> 10/n20 Configuration Pin
18	IFACE3	Clock Output
19 - 28	U9 – U0	UPPER DATA BIT 9 to UPPER DATA BIT 0
29	AUX1	Configurable as either AuxADC_A2 or AuxDAC_A
30	AUX2	Configurable as either AuxADC_A1 or AuxDAC_B
33	IFACE1	**SPI** : ***FD*** >> TxSYNC; ***HD24*** >> Tx/nRx; ***HD12*** >> Tx/nRx; ***Clone*** >> Tx/nRx **No SPI** : ***FD*** >> TxSYNC; ***HD24*** >> Tx/nRx; ***HD12*** >> Tx/nRx
34	Aux_SPI_CLK	CLK for AuxSPI
35 - 44	L9 – L0	LOWER DATA BIT 9 to LOWER DATA BIT 0
45	AUX3	Configurable as either AuxADC_B or AuxDAC_C
46	RESETb	Chip reset when low
47	AuxADC_Ref	Decoupling for AuxADC on-chip reference
48	CLKIN	Clock Input
52	REFB	ADC bottom reference
54, 55	VIN+B, VIN-B	ADC B differential input
56	VREF	ADC band gap reference
57, 58	VIN-A, VIN+A	ADC A differential input
60	REFT	ADC top reference
62	RxPwrDwn	Rx analog power down control
63	TxPwrDwn	Tx analog power down control
64	SPI_CS	Serial Port Chip Select (At Power Up: Tie high to enable SPI OR tie low to disable SPI and use Mode pins)

TIMING DIAGRAM

Figure 1: Timing Diagrams

Outline Dimensions

Figure 2:

Figure 3: