CMOS 8-BIT A/D CONVERTERS — ADC0801/2/3/4/5-1

Preliminary

DESCRIPTION

The ADC0801 family is a series of five CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor controlled buses using a minimum of external circuitry. The three-state output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

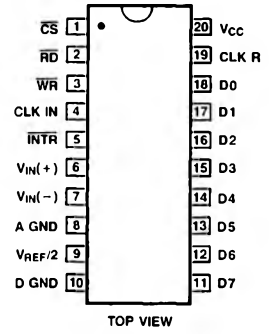
- **Compatible with most microprocessors**
- **Differential inputs**
- **Three-state outputs**
- **Logic levels TTL and MOS compatible**
- **Can be used with internal or external clock**
- **Analog input range 0V to V_{CC}**
- **Single 5V supply**
- **Guaranteed specification with 1MHz clock**

APPLICATIONS

- **Transducer to microprocessor interface**
- **Digital thermometer**
- **Digitally-controlled thermostat**
- **Microprocessor-based monitoring and control systems**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

ORDER NUMBERS

ADC0801/02-1F
ADC0801/02/03-1 LCF
ADC081/02/03/04/05-1 LCN
ADC0804-1 CN

ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage	6.5	V
	Logic Control Input Voltages	−0.3 to + 16	V
	All Other Input Voltages	−0.3 to (V_{CC} +0.3)	V
T_A	Operating Temperature Range ADC0801/02-1 F	−55 to +125	°C
	ADC0801/02/03-1 LCF	−40 to +85	°C
	ADC0801/02/03/04/05-1 LCN	−40 to +85	°C
	ADC0804-1 CN	0 to +70	°C
T_{STG}	Storage Temperature	−65 to +150	°C
T_{SOLD}	Lead Soldering Temperature (10 seconds)	300	°C
P_D	Package Power Dissipation at T_A = 25°C	875	mW

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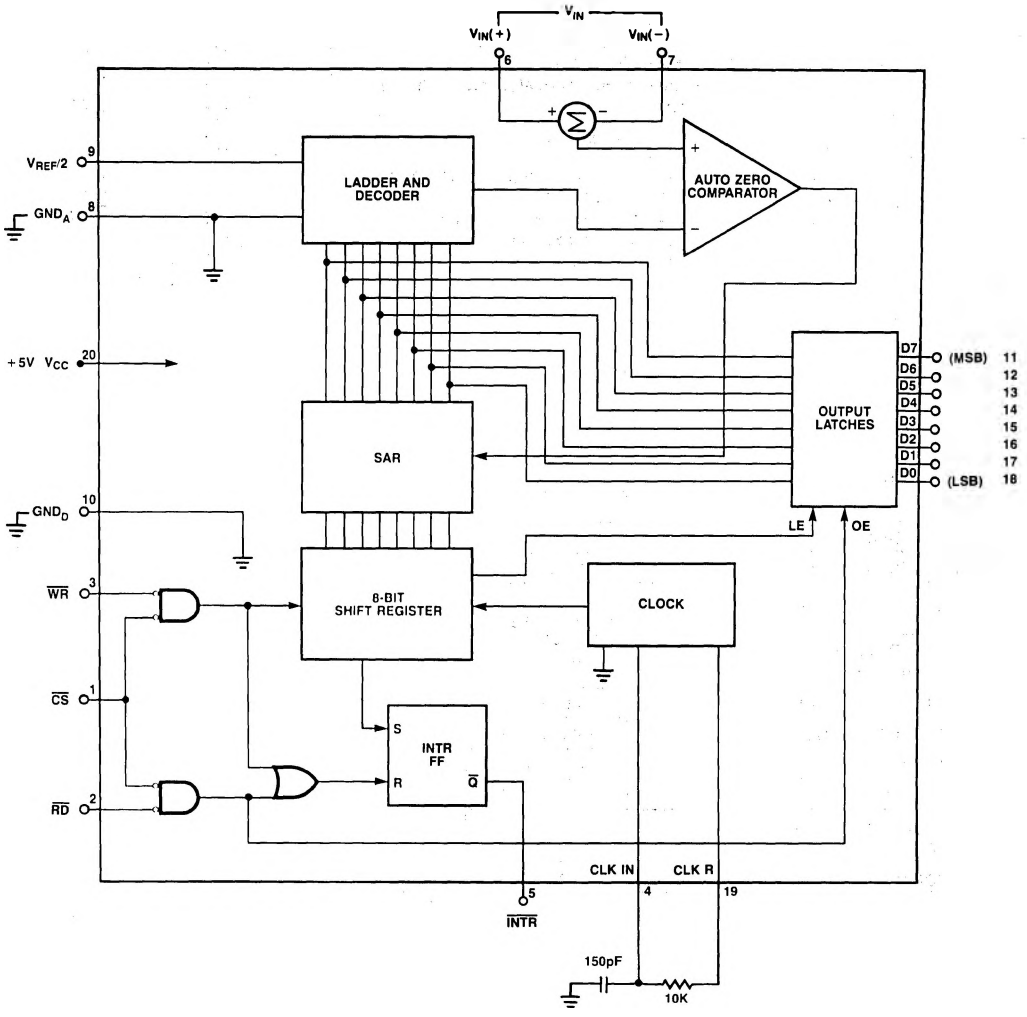
BLOCK DIAGRAMS



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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, f_{CLK} = 1MHz, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

SYMBOL & PARAMETER	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
		Min	Typ	Max	
ADC0801 Relative Accuracy Error (Adjusted)	Full Scale Adjusted			0.25	LSB
ADC0802 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2}$ = 2.500 V_{DC}			0.50	LSB
ADC0803 Relative Accuracy Error (Adjusted)	Full Scale Adjusted			0.50	LSB
ADC0804 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2}$ = 2.500 V_{DC}			1	LSB
ADC0805 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2}$ = has no connection			1	LSB
$\frac{V_{REF}}{2}$ Input Resistance		400	640		Ω
Analog Input Voltage Range		−0.05		V_{CC} +0.05	V
DC Common Mode Error	Over Analog Input Voltage Range		1/16	1/8	LSB
Power Supply Sensitivity	V_{CC} = 5V ± 10%[1]				
CONTROL INPUTS					
V_{IH} Logical "1" Input Voltage	V_{CC} = 5.25V_{DC}	2.0		15	V_{DC}
V_{IL} Logical "0" Input Voltage	V_{CC} = 4.75V_{DC}			0.8	V_{DC}
I_{IH} Logical "1" Input Current	V_{IN} = 5V_{DC}		0.005	1	μA_{DC}
I_{IL} Logical "0" Input Current	V_{IN} = 0V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R					
V_T+ Clk In Positive-Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T- Clk In Negative-Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H Clk In Hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OL} Logical "0" Clk R Output Voltage	I_{OL} = 360μA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OH} Logical "1" Clk R Output Voltage	I_{OH} = −360μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUT AND $\overline{INTR}$					
V_{OL} Logical "0" Output Voltage					
Data Outputs	I_{OL} = 1.6mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
$\overline{INTR}$ Outputs	I_{OL} = 1.0mA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OH} Logical "1" Output Voltage	I_{OH} = −360μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
	I_{OH} = −10μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OZL} 3-State Output Leakage	V_{OUT} = 0V_{DC}, $\overline{CS}$ = Logical "1"	−3			μA_{DC}
I_{OZH} 3-State Output Leakage	V_{OUT} = 5V_{DC}, $\overline{CS}$= Logical "1"			3	μA_{DC}
I_{SC} + Output Short Circuit Current	V_{OUT} = 0$_V$, T_A = 25°C	4.5	6		mA_{DC}
I_{SC} − Output Short Circuit Current	V_{OUT} = V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
I_{CC} Power Supply Current	f_{CLK} =1MHz, $V_{REF/2}$ = Open $\overline{CS}$ = Logical "1", T_A = 25°C		3.0	3.5	mA

NOTE:
1. Analog inputs must remain within the range: $-0.05 \leq V_{IN} \leq V_{CC} + 0.05V$.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER		TO	FROM	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
					Min	Typ	Max	
Conversion Time				f_{CLK} = 1MHz[1]	66		73	µs
f_{CLK}	Clock Frequency			See Note 1.	0.1	1.0	3.0	MHz
	Clock Duty Cycle			See Note 1.	40		60	%
CR	Free-Running Conversion Rate			$\overline{CS}$ = 0, f_{CLK} = 1MHz $\overline{INTR}$ Tied To $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start Pulse Width			$\overline{CS}$ = 0	30			ns
t_{ACC}	Access Time	Output	$\overline{RD}$	$\overline{CS}$ = 0, C_L = 100 pF		75	100	ns
t_{1H}, t_{OH}	Three-State Control	Output	$\overline{RD}$	CL = 10 pF, RL = 10K See Three-State Test Circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ Delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic Input =Capacitance					5	7.5	pF
C_{OUT}	Three-State Output Capacitance					5	7.5	pF

NOTE:
1. Accuracy is guaranteed at f_{CLK} = 1MHz. Accuracy may degrade at higher clock frequencies.

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FUNCTIONAL DESCRIPTION

The ADC0801 through ADC0805 series of A/D converters are successive approximation devices with 8-bit resolution and no missing codes. The most significant bit is tested first and after 64 clock cycles a digital 8-bit binary word is transferred to an output latch and the $\overline{INTR}$ pin goes low, indicating that conversion is complete. A conversion in progress can be interrupted by issuing another start command. The device may be operated in a continuous conversion mode by connecting the $\overline{INTR}$ and $\overline{WR}$ pins together and holding the $\overline{CS}$ pin low. To insure start-up when connected this way, an external $\overline{WR}$ pulse is required at power-up.

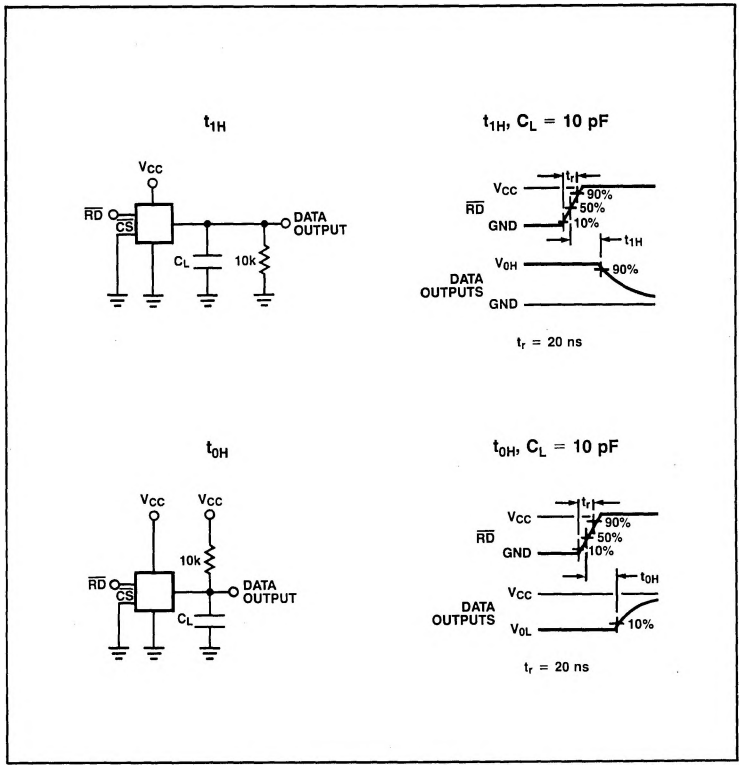
As the $\overline{WR}$ input goes low, when $\overline{CS}$ is low, the SAR is cleared and remains so as long as these two inputs are low. Conversion begins between 1 and 8 clock periods after at least one of these inputs goes high. As the conversion begins, the $\overline{INTR}$ line goes high. Note that the $\overline{INTR}$ line will remain low until 1 to 8 clock cycles after either the $\overline{WR}$ or the $\overline{CS}$ input (or both) goes high.

When the $\overline{CS}$ and $\overline{RD}$ inputs are both brought low to read the data, the $\overline{INTR}$ line will go low and the three-state output latches are enabled.

The digital control lines ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) operate with standard TTL levels and have been renamed when compared with standard A/D Start and Output Enable labels. For non-microprocessor based applications, the $\overline{CS}$ pin can be grounded, the $\overline{WR}$ pin can be interpreted as a $\overline{START}$ pulse pin, and the $\overline{RD}$ pin performs the OE (Output Enable) function.

The $V_{IN}(-)$ input can be used to subtract a fixed voltage from the input voltage. Because there is a time interval between sampling the $V_{IN}(+)$ and the $V(-)$ inputs, it is important that these inputs remain constant, during the entire conversion cycle.

THREE-STATE TEST CIRCUITS AND WAVEFORMS



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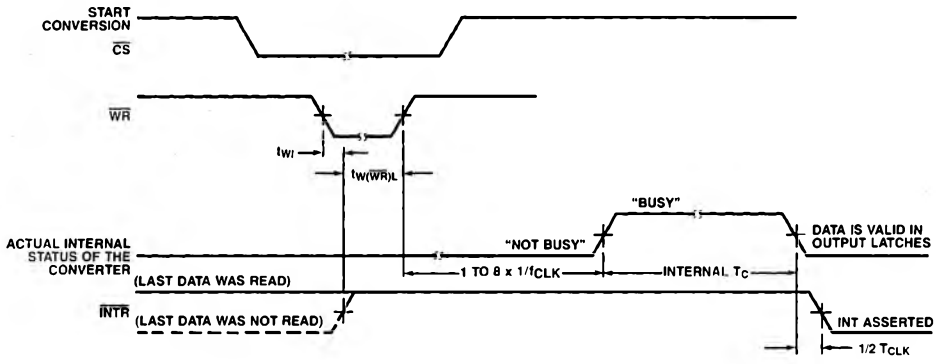
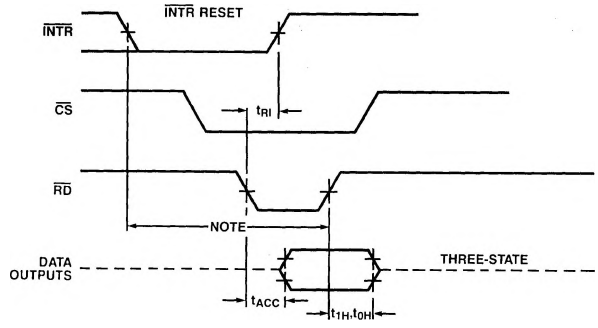
TIMING DIAGRAMS (All timing is measured from the 50% voltage points)



OUTPUT ENABLE AND RESET INTR



Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.